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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	384
Number of Logic Elements/Cells	-
Total RAM Bits	442368
Number of I/O	92
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-TFBGA, CSPBGA
Supplier Device Package	144-LCSBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v250-5csg144c

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
11/07/00	1.0	Early access draft.
12/06/00	1.1	Initial release.
01/15/01	1.2	Added values to the tables in the Virtex-II Performance Characteristics and Virtex-II Switching Characteristics sections.
01/25/01	1.3	The data sheet was divided into four modules (per the current style standard).
04/02/01	1.5	Skipped v1.4 to sync up modules. Reverted to traditional double-column format.
07/30/01	1.6	Made minor changes to items listed under Summary of Virtex-II™ Features.
10/02/01	1.7	Minor edits.
07/16/02	1.8	Updated Virtex-II Device/Package Combinations shown in Table 6.
09/26/02	1.9	Updated Table 2 and Table 6 to reflect supported Virtex-II Device/Package Combinations.
08/01/03	2.0	All Virtex-II devices and speed grades now Production. See Table 13, Module 3.
03/29/04	2.0.1	Recompiled for backward compatibility with Acrobat 4 and above. No content changes.
06/24/04	3.3	Added references to available Pb-free wire-bond packages. (Revision number advanced to level of complete data sheet.)
03/01/05	3.4	*No changes in Module 1 for this revision.*
11/05/07	3.5	Updated copyright notice and legal disclaimer.

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Virtex-II Data Sheet

The Virtex-II Data Sheet contains the following modules:

- Virtex-II Platform FPGAs: Introduction and Overview (Module 1)
- Virtex-II Platform FPGAs: Functional Description (Module 2)
- Virtex-II Platform FPGAs: DC and Switching Characteristics (Module 3)
- Virtex-II Platform FPGAs: Pinout Information (Module 4)

Table 5: **Minimum Power On Current Required for Virtex-II Devices**

	Device (mA)							
	XC2V40, XC2V80, XC2V250, XC2V500	XC2V1000	XC2V1500	XC2V2000	XC2V3000	XC2V4000	XC2V6000	XC2V8000
$I_{CCINTMIN}$	200	250	350	400	500	650	800	1100
$I_{CCAUXMIN}$	100	100	100	100	100	100	100	100
I_{CCOMIN}	50	50	100	100	100	100	100	100

Notes:
1. Values specified for power on current parameters are Commercial Grade. For Industrial Grade values, multiply Commercial Grade values by 1.25.
2. I_{CCOMIN} values listed here apply to the entire device (all banks).

General Power Supply Requirements

Proper decoupling of all FPGA power supplies is sessential. Consult Xilinx Application Note **XAPP623** for detailed information on power distribution system design.

V_{CCAUX} powers critical resources in the FPGA. Thus, V_{CCAUX} is especially susceptible to power supply noise.

Changes in V_{CCAUX} voltage outside of 200 mV peak to peak should take place at a rate no faster than 10 mV per millisecond. Techniques to help reduce jitter and period distortion are provided in Xilinx Answer Record 13756, available at **www.support.xilinx.com**.

V_{CCAUX} can share a power plane with 3.3V V_{CCO}, but only if V_{CCO} does not have excessive noise. Using simultaneously switching output (SSO) limits are essential for keeping power supply noise to a minimum. Refer to **XAPP689**, "Managing Ground Bounce in Large FPGAs," to determine the number of simultaneously switching outputs allowed per bank at the package level.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 6: **DC Input and Output Levels**

Input/Output	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
Standard	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTL(1)	– 0.5	0.8	2.0	3.6	0.4	2.4	24	– 24
LVCMOS33	– 0.5	0.8	2.0	3.6	0.4	V_{CCO} – 0.4	24	– 24
LVCMOS25	– 0.5	0.7	1.7	2.7	0.4	V_{CCO} – 0.4	24	– 24
LVCMOS18	– 0.5	35% V_{CCO}	65% V_{CCO}	1.95	0.4	V_{CCO} – 0.4	16	– 16
LVCMOS15	– 0.5	35% V_{CCO}	65% V_{CCO}	1.7	0.4	V_{CCO} – 0.4	16	– 16
PCI33_3	– 0.5	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
PCI66_3	– 0.5	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
PCI–X	– 0.5	Note 2	Note 2	Note 2	Note 2	Note 2	Note 2	Note 2
GTLP	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.5	0.6	n/a	36	n/a
GTL	– 0.5	V_{REF} – 0.05	V_{REF} + 0.05	V_{CCO} + 0.5	0.4	n/a	40	n/a
HSTL I	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.5	0.4	V_{CCO} – 0.4	8	– 8
HSTL II	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.5	0.4	V_{CCO} – 0.4	16	– 16
HSTL III	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.5	0.4	V_{CCO} – 0.4	24	– 8
HSTL IV	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.5	0.4	V_{CCO} – 0.4	48	– 8

Clock Distribution Switching Characteristics

Table 20: **Clock Distribution Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Global Clock Buffer I input to O output	T_{GIO}	0.47	0.52	0.59	ns, Max
Global Clock Buffer S input Setup/Hold to I1 an I2 inputs	T_{GSI}/T_{GIS}	0.55/ 0	0.61/ 0	0.70/ 0	ns, Max

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used (see Figure 16 in Module 2). The values listed below are worst-case. Precise values are provided by the timing analyzer.

Table 21: **CLB Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Combinatorial Delays					
4-input function: F/G inputs to X/Y outputs	T_{ILO}	0.35	0.39	0.44	ns, Max
5-input function: F/G inputs to F5 output	T_{IF5}	0.57	0.63	0.72	ns, Max
5-input function: F/G inputs to X output	T_{IF5X}	0.76	0.83	0.95	ns, Max
FXINA or FXINB inputs to Y output via MUXFX	T_{IFXY}	0.36	0.39	0.45	ns, Max
FXINA input to FX output via MUXFX	T_{INAFX}	0.26	0.28	0.32	ns, Max
FXINB input to FX output via MUXFX	T_{INBFX}	0.26	0.28	0.32	ns, Max
SOPIN input to SOPOUT output via ORCY	T_{SOPSOP}	0.35	0.38	0.44	ns, Max
Incremental delay routing through transparent latch to XQ/YQ outputs	T_{IFNCTL}	0.41	0.45	0.51	ns, Max
Sequential Delays					
FF Clock CLK to XQ/YQ outputs	T_{CKO}	0.45	0.50	0.57	ns, Max
Latch Clock CLK to XQ/YQ outputs	T_{CKLO}	0.54	0.59	0.68	ns, Max
Setup and Hold Times Before/After Clock CLK					
BX/BY inputs	T_{DICK}/T_{CKDI}	0.30/–0.07	0.33/–0.08	0.37/–0.09	ns, Min
DY inputs	T_{DYCK}/T_{CKDY}	0.30/–0.07	0.33/–0.08	0.37/–0.09	ns, Min
DX inputs	T_{DXCK}/T_{CKDX}	0.30/–0.07	0.33/–0.08	0.37/–0.09	ns, Min
CE input	T_{CECK}/T_{CKCE}	0.19/–0.06	0.21/–0.07	0.24/–0.08	ns, Min
SR/BY inputs (synchronous)	T_{SRCK}/T_{SCKR}	0.21/–0.02	0.23/–0.03	0.26/–0.03	ns, Min
Clock CLK					
Minimum Pulse Width, High	T_{CH}	0.61	0.67	0.77	ns, Min
Minimum Pulse Width, Low	T_{CL}	0.61	0.67	0.77	ns, Min
Set/Reset					
Minimum Pulse Width, SR/BY inputs (asynchronous)	T_{RPW}	0.61	0.67	0.77	ns, Min
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	T_{RQ}	1.06	1.17	1.34	ns, Max
Toggle Frequency (MHz) (for export control)	F_{TOG}	820	750	650	MHz

CLB Distributed RAM Switching Characteristics

Table 22: **CLB Distributed RAM Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Sequential Delays					
Clock CLK to X/Y outputs (WE active) in 16 x 1 mode	$T_{SHCKO16}$	1.63	1.79	2.05	ns, Max
Clock CLK to X/Y outputs (WE active) in 32 x 1 mode	$T_{SHCKO32}$	1.97	2.17	2.49	ns, Max
Clock CLK to F5 output	$T_{SHCKOF5}$	1.77	1.94	2.23	ns, Max
Setup and Hold Times Before/After Clock CLK					
BX/BY data inputs (DIN)	T_{DS}/T_{DH}	0.53/–0.09	0.58/–0.10	0.67/–0.11	ns, Min
F/G address inputs	T_{AS}/T_{AH}	0.40/ 0.00	0.44/ 0.00	0.50/ 0.00	ns, Min
SR input (WS)	T_{WES}/T_{WEH}	0.42/–0.01	0.46/–0.01	0.53/–0.01	ns, Min
Clock CLK					
Minimum Pulse Width, High	T_{WPH}	0.57	0.63	0.72	ns, Min
Minimum Pulse Width, Low	T_{WPL}	0.57	0.63	0.72	ns, Min
Minimum clock period to meet address write cycle time	T_{WC}	1.14	1.25	1.44	ns, Min

CLB Shift Register Switching Characteristics

Table 23: **CLB Shift Register Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Sequential Delays					
Clock CLK to X/Y outputs	T_{REG}	2.31	2.54	2.92	ns, Max
Clock CLK to X/Y outputs	T_{REG32}	2.65	2.92	3.35	ns, Max
Clock CLK to XB output via MC15 LUT output	T_{REGXB}	2.23	2.46	2.82	ns, Max
Clock CLK to YB output via MC15 LUT output	T_{REGYB}	2.18	2.40	2.75	ns, Max
Clock CLK to Shiftout	T_{CKSH}	1.92	2.11	2.43	ns, Max
Clock CLK to F5 output	T_{REGF5}	2.45	2.69	3.09	ns, Max
Setup and Hold Times Before/After Clock CLK					
BX/BY data inputs (DIN)	T_{SRLDS}/T_{SRLDH}	0.53/–0.07	0.58/–0.08	0.67/–0.09	ns, Min
SR input (WS)	T_{WSS}/T_{WSH}	0.19/–0.06	0.21/–0.07	0.24/–0.08	ns, Min
Clock CLK					
Minimum Pulse Width, High	T_{SRPH}	0.57	0.63	0.72	ns, Min
Minimum Pulse Width, Low	T_{SRPL}	0.57	0.63	0.72	ns, Min

Source-Synchronous Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-II source-synchronous transmitter and receiver data-valid windows.

Table 45: **Duty Cycle Distortion and Clock-Tree Skew**

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
Duty Cycle Distortion(1)	T_{DCD_CLK0}	All	140	140	140	ps
	T_{DCD_CLK180}	All	50	50	50	ps
Clock Tree Skew(2)	T_{CKSKEW}	XC2V40	50	50	60	ps
		XC2V80	50	50	60	ps
		XC2V250	50	50	60	ps
		XC2V500	50	50	60	ps
		XC2V1000	80	80	90	ps
		XC2V1500	80	80	90	ps
		XC2V2000	100	100	110	ps
		XC2V3000	100	100	110	ps
		XC2V4000	400	400	450	ps
		XC2V6000	500	500	550	ps
		XC2V8000		600	650	ps

Notes:

1. These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
   T_{DCD_CLK0} applies to cases where local (IOB) inversion is used to provide the negative-edge clock to the DDR element in the I/O.
   T_{DCD_CLK180} applies to cases where the CLK180 output of the DCM is used to provide the negative-edge clock to the DDR element in the I/O.
2. This value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

Table 46: **Package Skew**

Description	Symbol	Device/Package	Value	Units
Package Skew(1)	$T_{PKGSKEW}$	XC2V1000 / FF896	130	ps
		XC2V3000 / FF1152	115	ps
		XC2V3000 / BF957	130	ps
		XC2V4000 / FF1152	130	ps
		XC2V4000 / FF1517	200	ps
		XC2V4000 / BF957	140	ps
		XC2V6000 / FF1152	90	ps
		XC2V6000 / FF1517	105	ps
		XC2V6000 / BF957	105	ps

Notes:

1. These values represent the worst-case skew between any two balls of the package: shortest flight time to longest flight time from Pad to Ball (7.1ps per mm).
2. Package trace length information is available for these device/package combinations. This information can be used to deskew the package.

Table 3: **Virtex-II Device/Package Combinations and Maximum Number of Available I/Os**

Package	Available I/Os										
	XC2V 40	XC2V 80	XC2V 250	XC2V 500	XC2V 1000	XC2V 1500	XC2V 2000	XC2V 3000	XC2V 4000	XC2V 6000	XC2V 8000
CS144	88	92	92	-	-	-	-	-	-	-	-
FG256	88	120	172	172	172	-	-	-	-	-	-
FG456	-	-	200	264	324	-	-	-	-	-	-
FG676	-	-	-	-	-	392	456	484	-	-	-
FF896	-	-	-	-	432	528	624	-	-	-	-
FF1152	-	-	-	-	-	-	-	720	824	824	824
FF1517	-	-	-	-	-	-	-	-	912	1,104	1,108
BG575	-	-	-	-	328	392	408	-	-	-	-
BG728	-	-	-	-	-	-	-	516	-	-	-
BF957	-	-	-	-	-	-	624	684	684	684	-

Virtex-II Pin Definitions

This section describes the pinouts for Virtex-II devices in the following packages:

- CS144: wire-bond chip-scale ball grid array (BGA) of 0.80 mm pitch
- FG256, FG456, and FG676: wire-bond fine-pitch BGA of 1.00 mm pitch
- FF896, FF1152, FF1517: flip-chip fine-pitch BGA of 1.00 mm pitch
- BG575 and BG728: wire-bond BGA of 1.27 mm pitch
- BF957: flip-chip BGA of 1.27 mm pitch

All of the devices supported in a particular package are pinout compatible and are listed in the same table (one table per package). In addition, the FG456 and FG676 packages are compatible, as are the FF896 and FF1152 packages. Pins that are not available for the smallest devices are listed in right-hand columns.

Each device is split into eight I/O banks to allow for flexibility in the choice of I/O standards (see the Virtex-II *Data Sheet*). Global pins, including JTAG, configuration, and power/ground pins, are listed at the end of each table. Table 4 provides definitions for all pin types.

The FG256 pinouts (Table 6) is included as an example. All Virtex-II pinout tables are available on the distribution CD-ROM, or on the web (at **http://www.xilinx.com**).

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
NA	VCCINT	R16		
NA	VCCINT	R7		
NA	VCCINT	H16		
NA	VCCINT	H7		
NA	VCCINT	G16		
NA	VCCINT	G15		
NA	VCCINT	G8		
NA	VCCINT	G7		
NA	VCCINT	F17		
NA	VCCINT	F6		
NA	GND	AB22		
NA	GND	AB1		
NA	GND	AA21		
NA	GND	AA2		
NA	GND	Y20		
NA	GND	Y3		
NA	GND	W19		
NA	GND	W4		
NA	GND	P14		
NA	GND	P13		
NA	GND	P12		
NA	GND	P11		
NA	GND	P10		
NA	GND	P9		
NA	GND	N14		
NA	GND	N13		
NA	GND	N12		
NA	GND	N11		
NA	GND	N10		
NA	GND	N9		
NA	GND	M14		
NA	GND	M13		
NA	GND	M12		
NA	GND	M11		

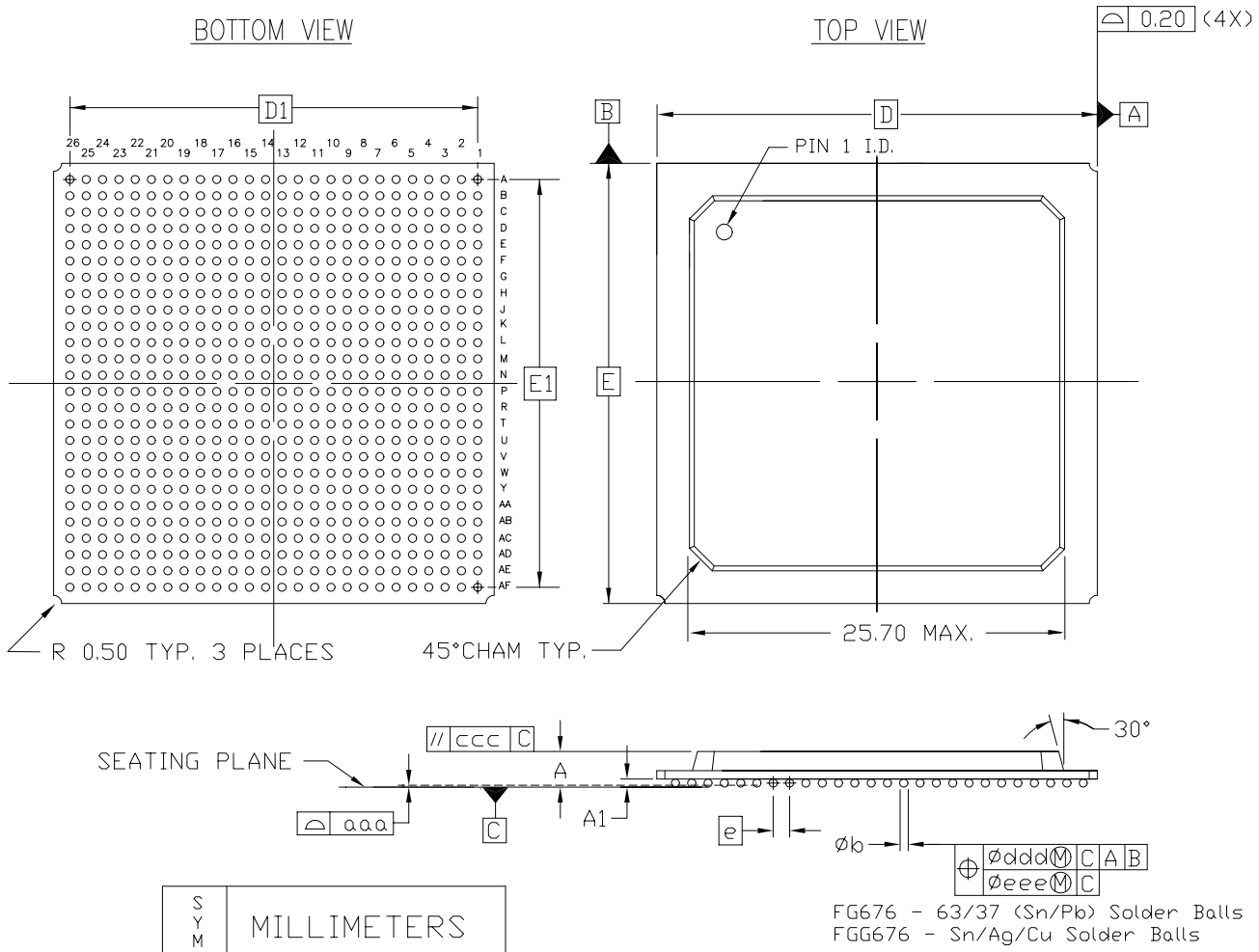
Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
4	IO_L06P_4	Y21		
4	IO_L19N_4	AE24		
4	IO_L19P_4	AF24		
4	IO_L21N_4	AE23		
4	IO_L21P_4/VREF_4	AF23		
4	IO_L22N_4	AE22		
4	IO_L22P_4	AF22		
4	IO_L24N_4	AF21		
4	IO_L24P_4	AF20		
4	IO_L25N_4	AA19	NC	NC
4	IO_L25P_4	AB19	NC	NC
4	IO_L27N_4	AD20	NC	NC
4	IO_L27P_4/VREF_4	AC20	NC	NC
4	IO_L28N_4	AC19	NC	NC
4	IO_L28P_4	AD19	NC	NC
4	IO_L49N_4	AE19		
4	IO_L49P_4	AF19		
4	IO_L51N_4	AA18		
4	IO_L51P_4/VREF_4	AB18		
4	IO_L52N_4	Y18		
4	IO_L52P_4	Y17		
4	IO_L54N_4	AC18		
4	IO_L54P_4	AD18		
4	IO_L67N_4	AE18		
4	IO_L67P_4	AF18		
4	IO_L69N_4	AA17		
4	IO_L69P_4/VREF_4	AB17		
4	IO_L70N_4	AC17		
4	IO_L70P_4	AD17		
4	IO_L72N_4	AF17		
4	IO_L72P_4	AF16		
4	IO_L73N_4	AB16	NC	
4	IO_L73P_4	AC16	NC	
4	IO_L75N_4	AA16	NC	
4	IO_L75P_4/VREF_4	Y16	NC	
4	IO_L76N_4	AD16	NC	
4	IO_L76P_4	AE16	NC	

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
3	VCCO_3	V19		
3	VCCO_3	U25		
3	VCCO_3	U19		
3	VCCO_3	T18		
3	VCCO_3	R18		
3	VCCO_3	P18		
4	VCCO_4	AE20		
4	VCCO_4	AE17		
4	VCCO_4	W18		
4	VCCO_4	W17		
4	VCCO_4	V16		
4	VCCO_4	V15		
4	VCCO_4	V14		
5	VCCO_5	AE10		
5	VCCO_5	AE7		
5	VCCO_5	W10		
5	VCCO_5	W9		
5	VCCO_5	V13		
5	VCCO_5	V12		
5	VCCO_5	V11		
6	VCCO_6	Y2		
6	VCCO_6	V8		
6	VCCO_6	U8		
6	VCCO_6	U2		
6	VCCO_6	T9		
6	VCCO_6	R9		
6	VCCO_6	P9		
7	VCCO_7	N9		
7	VCCO_7	M9		
7	VCCO_7	L9		
7	VCCO_7	K8		
7	VCCO_7	K2		
7	VCCO_7	J8		
7	VCCO_7	G2		
NA	CCLK	AB21		
NA	PROG_B	C4		

FG676/FGG676 Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A		2.25	2.60
A_1	0.40	0.50	0.60
D/E	27.00 BSC		
D_1/E_1	25.00 REF		
e	1.00 BSC		
øb	0.50	0.60	0.70
aaa			0.20
ccc			0.35
ddd			0.30
eee			0.10
M	26		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-AAL-1

676-BALL FINE PITCH BGA (FG676/FGG676)

Figure 4: **FG676/FGG676 Fine-Pitch BGA Package Specifications**

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
2	IO_L01P_2	D23		
2	IO_L02N_2/VRP_2	E21		
2	IO_L02P_2/VRN_2	E22		
2	IO_L03N_2	F21		
2	IO_L03P_2/VREF_2	F20		
2	IO_L04N_2	G20		
2	IO_L04P_2	G19		
2	IO_L06N_2	H18		
2	IO_L06P_2	J17		
2	IO_L19N_2	D24		
2	IO_L19P_2	E23		
2	IO_L21N_2	E24		
2	IO_L21P_2/VREF_2	F24		
2	IO_L22N_2	F23		
2	IO_L22P_2	G23		
2	IO_L24N_2	G21		
2	IO_L24P_2	G22		
2	IO_L43N_2	H19		
2	IO_L43P_2	H20		
2	IO_L45N_2	J18		
2	IO_L45P_2/VREF_2	J19		
2	IO_L46N_2	K17		
2	IO_L46P_2	K18		
2	IO_L48N_2	H23		
2	IO_L48P_2	H24		
2	IO_L49N_2	H21		
2	IO_L49P_2	H22		
2	IO_L51N_2	J24		
2	IO_L51P_2/VREF_2	K24		
2	IO_L52N_2	J22		
2	IO_L52P_2	J23		
2	IO_L54N_2	J20		
2	IO_L54P_2	J21		
2	IO_L67N_2	K19	NC	
2	IO_L67P_2	K20	NC	
2	IO_L69N_2	L17	NC	

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
3	IO_L52N_3	T21		
3	IO_L52P_3	T20		
3	IO_L51N_3/VREF_3	R20		
3	IO_L51P_3	R19		
3	IO_L49N_3	W24		
3	IO_L49P_3	W23		
3	IO_L48N_3	U23		
3	IO_L48P_3	V23		
3	IO_L46N_3	U22		
3	IO_L46P_3	U21		
3	IO_L45N_3/VREF_3	V22		
3	IO_L45P_3	V21		
3	IO_L43N_3	U19		
3	IO_L43P_3	U20		
3	IO_L24N_3	T19		
3	IO_L24P_3	T18		
3	IO_L22N_3	R18		
3	IO_L22P_3	R17		
3	IO_L21N_3/VREF_3	Y24		
3	IO_L21P_3	Y23		
3	IO_L19N_3	AA24		
3	IO_L19P_3	AB24		
3	IO_L06N_3	AA23		
3	IO_L06P_3	AA22		
3	IO_L04N_3	Y22		
3	IO_L04P_3	Y21		
3	IO_L03N_3/VREF_3	W21		
3	IO_L03P_3	W20		
3	IO_L02N_3/VRP_3	V20		
3	IO_L02P_3/VRN_3	V19		
3	IO_L01N_3	U18		
3	IO_L01P_3	T17		
4	IO_L01N_4/BUSY/DOUT(1)	AD22		
4	IO_L01P_4/INIT_B	AD21		
4	IO_L02N_4/D0/DIN(1)	AA20		

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
NA	VCCINT	R10		
NA	VCCINT	P15		
NA	VCCINT	P10		
NA	VCCINT	N15		
NA	VCCINT	N10		
NA	VCCINT	M15		
NA	VCCINT	M10		
NA	VCCINT	L15		
NA	VCCINT	L10		
NA	VCCINT	K15		
NA	VCCINT	K14		
NA	VCCINT	K13		
NA	VCCINT	K12		
NA	VCCINT	K11		
NA	VCCINT	K10		
NA	VCCINT	J16		
NA	VCCINT	J9		
NA	VCCINT	H17		
NA	VCCINT	H8		
NA	GND	AD24		
NA	GND	AD23		
NA	GND	AD18		
NA	GND	AD7		
NA	GND	AD2		
NA	GND	AD1		
NA	GND	AC24		
NA	GND	AC23		
NA	GND	AC2		
NA	GND	AC1		
NA	GND	AB22		
NA	GND	AB3		
NA	GND	AA21		
NA	GND	AA15		
NA	GND	AA10		
NA	GND	AA4		
NA	GND	Y20		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
5	IO_L23N_5	AD20		
5	IO_L23P_5	AD21		
5	IO_L22N_5	AK25		
5	IO_L22P_5	AK24		
5	IO_L21N_5/VREF_5	AH24		
5	IO_L21P_5	AH25		
5	IO_L20N_5	AE21		
5	IO_L20P_5	AD22		
5	IO_L19N_5	AJ25		
5	IO_L19P_5	AJ24		
5	IO_L06N_5	AG25		
5	IO_L06P_5	AG24		
5	IO_L05N_5/VRP_5	AC20		
5	IO_L05P_5/VRN_5	AC21		
5	IO_L04N_5	AK26		
5	IO_L04P_5/VREF_5	AK27		
5	IO_L03N_5/D4/ALT_VRP_5	AH26		
5	IO_L03P_5/D5/ALT_VRN_5	AJ27		
5	IO_L02N_5/D6	AE22		
5	IO_L02P_5/D7	AE23		
5	IO_L01N_5/RDWR_B	AJ28		
5	IO_L01P_5/CS_B	AK29		
6	IO_L01P_6	AC22		
6	IO_L01N_6	AB23		
6	IO_L02P_6/VRN_6	AG28		
6	IO_L02N_6/VRP_6	AF28		
6	IO_L03P_6	AJ30		
6	IO_L03N_6/VREF_6	AH30		
6	IO_L04P_6	AD23		
6	IO_L04N_6	AC23		
6	IO_L05P_6	AF27		
6	IO_L05N_6	AE27		
6	IO_L06P_6	AG29		
6	IO_L06N_6	AH29		
6	IO_L19P_6	AE24		
6	IO_L19N_6	AD24		

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
4	IO_L20N_4	AJ10	
4	IO_L20P_4	AJ9	
4	IO_L21N_4	AH9	
4	IO_L21P_4/VREF_4	AH10	
4	IO_L22N_4	AN5	
4	IO_L22P_4	AN4	
4	IO_L23N_4	AE12	
4	IO_L23P_4	AE13	
4	IO_L24N_4	AM9	
4	IO_L24P_4	AL8	
4	IO_L25N_4	AP5	
4	IO_L25P_4	AP4	
4	IO_L26N_4	AG11	
4	IO_L26P_4	AG12	
4	IO_L27N_4	AN7	
4	IO_L27P_4/VREF_4	AN6	
4	IO_L28N_4	AL10	
4	IO_L28P_4	AL9	
4	IO_L29N_4	AF12	
4	IO_L29P_4	AF13	
4	IO_L30N_4	AK10	
4	IO_L30P_4	AK11	
4	IO_L49N_4	AP7	
4	IO_L49P_4	AP6	
4	IO_L50N_4	AH13	
4	IO_L50P_4	AH12	
4	IO_L51N_4	AJ11	
4	IO_L51P_4/VREF_4	AJ12	
4	IO_L52N_4	AP9	
4	IO_L52P_4	AN8	
4	IO_L53N_4	AG13	
4	IO_L53P_4	AG14	
4	IO_L54N_4	AM11	
4	IO_L54P_4	AL11	
4	IO_L60N_4	AN10	NC
4	IO_L60P_4	AN9	NC

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
5	VCCO_5	AP19	
5	VCCO_5	AL28	
5	VCCO_5	AK20	
5	VCCO_5	AD23	
5	VCCO_5	AD22	
5	VCCO_5	AD21	
5	VCCO_5	AD20	
5	VCCO_5	AC22	
5	VCCO_5	AC21	
5	VCCO_5	AC20	
5	VCCO_5	AC19	
5	VCCO_5	AC18	
6	VCCO_6	AH31	
6	VCCO_6	AE34	
6	VCCO_6	AC24	
6	VCCO_6	AB24	
6	VCCO_6	AB23	
6	VCCO_6	AA24	
6	VCCO_6	AA23	
6	VCCO_6	Y30	
6	VCCO_6	Y24	
6	VCCO_6	Y23	
6	VCCO_6	W34	
6	VCCO_6	W23	
6	VCCO_6	V23	
7	VCCO_7	U23	
7	VCCO_7	T34	
7	VCCO_7	T23	
7	VCCO_7	R30	
7	VCCO_7	R24	
7	VCCO_7	R23	
7	VCCO_7	P24	
7	VCCO_7	P23	
7	VCCO_7	N24	
7	VCCO_7	N23	
7	VCCO_7	M24	