AMD Xilinx - XC2V250-5FG256I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	384
Number of Logic Elements/Cells	-
Total RAM Bits	442368
Number of I/O	172
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v250-5fg256i

Virtex-II Platform FPGAs: Introduction and Overview

DS031-1 (v3.5) November 5, 2007 **Product Specification**

Summary of Virtex-II™ Features

- Industry First Platform FPGA Solution
- IP-Immersion Architecture
  - Densities from 40K to 8M system gates
  - 420 MHz internal clock speed (Advance Data)
  - 840+ Mb/s I/O (Advance Data)
- SelectRAM™ Memory Hierarchy
  - 3 Mb of dual-port RAM in 18 Kbit block SelectRAM resources
  - Up to 1.5 Mb of distributed SelectRAM resources
- High-Performance Interfaces to External Memory
  - DRAM interfaces
    - SDR / DDR SDRAM
    - Network FCRAM
    - Reduced Latency DRAM
  - SRAM interfaces
    - SDR / DDR SRAM
    - QDR™ SRAM
  - CAM interfaces
- Arithmetic Functions
  - Dedicated 18-bit x 18-bit multiplier blocks
  - Fast look-ahead carry logic chains
- Flexible Logic Resources
  - Up to 93,184 internal registers / latches with Clock Enable
  - Up to 93,184 look-up tables (LUTs) or cascadable 16-bit shift registers
  - Wide multiplexers and wide-input function support
  - Horizontal cascade chain and sum-of-products support
  - Internal 3-state bussing
- High-Performance Clock Management Circuitry
  - Up to 12 DCM (Digital Clock Manager) modules
    - Precise clock de-skew
    - Flexible frequency synthesis
    - High-resolution phase shifting
  - 16 global clock multiplexer buffers
- Active Interconnect Technology
  - Fourth generation segmented routing structure
  - Predictable, fast routing delay, independent of fanout
- SelectIO™-Ultra Technology
  - Up to 1,108 user I/Os
  - 19 single-ended and six differential standards
  - Programmable sink current (2 mA to 24 mA) per I/O
  - Digitally Controlled Impedance (DCI) I/O: on-chip termination resistors for single-ended I/O standards
  - PCI-X compatible (133 MHz and 66 MHz) at 3.3V
  - PCI compliant (66 MHz and 33 MHz) at 3.3V
  - CardBus compliant (33 MHz) at 3.3V
  - Differential Signaling
    - 840 Mb/s Low-Voltage Differential Signaling I/O (LVDS) with current mode drivers
    - Bus LVDS I/O
    - Lightning Data Transport (LDT) I/O with current driver buffers
    - Low-Voltage Positive Emitter-Coupled Logic (LVPECL) I/O
    - Built-in DDR input and output registers
  - Proprietary high-performance SelectLink Technology
    - High-bandwidth data path
    - Double Data Rate (DDR) link
    - Web-based HDL generation methodology
- Supported by Xilinx Foundation™ and Alliance Series™ Development Systems
  - Integrated VHDL and Verilog design flows
  - Compilation of 10M system gates designs
  - Internet Team Design (ITD) tool
- SRAM-Based In-System Configuration
  - Fast SelectMAP configuration
  - Triple Data Encryption Standard (DES) security option (Bitstream Encryption)
  - IEEE 1532 support
  - Partial reconfiguration
  - Unlimited reprogrammability
  - Readback capability
- 0.15 µm 8-Layer Metal Process with 0.12 µm High-Speed Transistors
- 1.5V (V_{CCINT}) Core Power Supply, Dedicated 3.3V V_{CCAUX} Auxiliary and V_{CCO} I/O Power Supplies
- IEEE 1149.1 Compatible Boundary-Scan Logic Support
- Flip-Chip and Wire-Bond Ball Grid Array (BGA) Packages in Three Standard Fine Pitches (0.80 mm, 1.00 mm, and 1.27 mm)
- Wire-Bond BGA Devices Available in Pb-Free Packaging (www.xilinx.com/pbfree)
- 100% Factory Tested

Architecture

Virtex-II Array Overview

Virtex-II devices are user-programmable gate arrays with various configurable elements. The Virtex-II architecture is optimized for high-density and high-performance logic designs. As shown in Figure 1, the programmable device is comprised of input/output blocks (IOBs) and internal configurable logic blocks (CLBs).

Programmable I/O blocks provide the interface between package pins and the internal configurable logic. Most popular and leading-edge I/O standards are supported by the programmable IOBs.

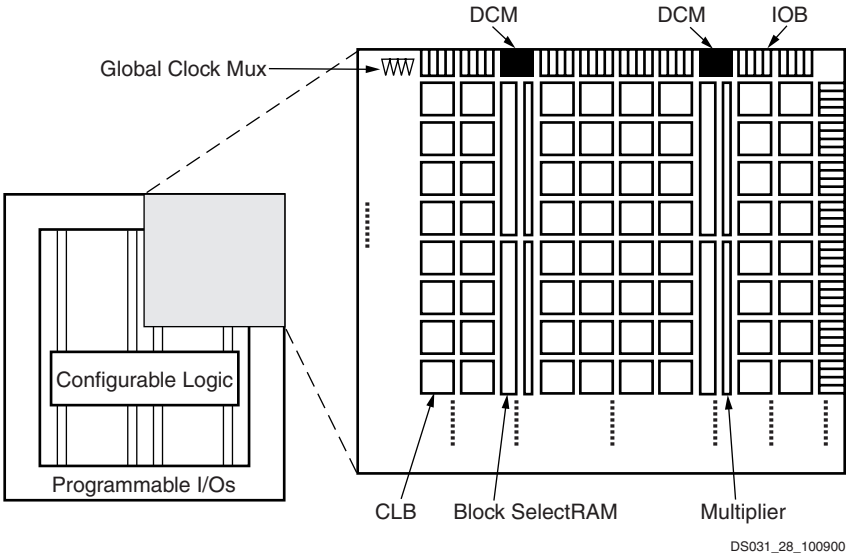

Figure 1: **Virtex-II Architecture Overview**

The internal configurable logic includes four major elements organized in a regular array.

- Configurable Logic Blocks (CLBs) provide functional elements for combinatorial and synchronous logic, including basic storage elements. BUFTs (3-state buffers) associated with each CLB element drive dedicated segmentable horizontal routing resources.
- Block SelectRAM memory modules provide large 18 Kbit storage elements of dual-port RAM.
- Multiplier blocks are 18-bit x 18-bit dedicated multipliers.
- DCM (Digital Clock Manager) blocks provide self-calibrating, fully digital solutions for clock distribution delay compensation, clock multiplication and division, coarse- and fine-grained clock phase shifting.

A new generation of programmable routing resources called Active Interconnect Technology interconnects all of these elements. The general routing matrix (GRM) is an array of routing switches. Each programmable element is tied to a switch matrix, allowing multiple connections to the general routing matrix. The overall programmable interconnection is hierarchical and designed to support high-speed designs.

All programmable elements, including the routing resources, are controlled by values stored in static memory cells. These values are loaded in the memory cells during configuration and can be reloaded to change the functions of the programmable elements.

Virtex-II Features

This section briefly describes Virtex-II features.

Input/Output Blocks (IOBs)

IOBs are programmable and can be categorized as follows:

- Input block with an optional single-data-rate or double-data-rate (DDR) register
- Output block with an optional single-data-rate or DDR register, and an optional 3-state buffer, to be driven directly or through a single or DDR register
- Bidirectional block (any combination of input and output configurations)

These registers are either edge-triggered D-type flip-flops or level-sensitive latches.

IOBs support the following single-ended I/O standards:

- LVTTL, LVCMOS (3.3V, 2.5V, 1.8V, and 1.5V)
- PCI-X compatible (133 MHz and 66 MHz) at 3.3V
- PCI compliant (66 MHz and 33 MHz) at 3.3V
- CardBus compliant (33 MHz) at 3.3V
- GTL and GTLP

Notice of Disclaimer

Virtex-II Data Sheet

The Virtex-II Data Sheet contains the following modules:

- Virtex-II Platform FPGAs: Introduction and Overview (Module 1)
- Virtex-II Platform FPGAs: Functional Description (Module 2)
- Virtex-II Platform FPGAs: DC and Switching Characteristics (Module 3)
- Virtex-II Platform FPGAs: Pinout Information (Module 4)

Table 17: **IOB Output Switching Characteristics Standard Adjustments *(Continued)***

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-6	-5	-4	
LVCMOS, 2.5V, Fast, 16 mA	LVCMOS25_F16	$T_{OLVCMOS25\_F16}$	–0.18	–0.19	–0.21	ns
LVCMOS, 2.5V, Fast, 24 mA	LVCMOS25_F24	$T_{OLVCMOS25\_F24}$	–0.35	–0.36	–0.40	ns
LVCMOS, 1.8V, Slow, 2 mA	LVCMOS18_S2	$T_{OLVCMOS18\_S2}$	15.62	16.10	17.71	ns
LVCMOS, 1.8V, Slow, 4 mA	LVCMOS18_S4	$T_{OLVCMOS18\_S4}$	10.20	10.51	11.57	ns
LVCMOS, 1.8V, Slow, 6 mA	LVCMOS18_S6	$T_{OLVCMOS18\_S6}$	7.52	7.75	8.53	ns
LVCMOS, 1.8V, Slow, 8 mA	LVCMOS18_S8	$T_{OLVCMOS18\_S8}$	6.87	7.08	7.78	ns
LVCMOS, 1.8V, Slow, 12 mA	LVCMOS18_S12	$T_{OLVCMOS18\_S12}$	5.54	5.71	6.28	ns
LVCMOS, 1.8V, Slow, 16 mA	LVCMOS18_S16	$T_{OLVCMOS18\_S16}$	5.31	5.47	6.02	ns
LVCMOS, 1.8V, Fast, 2 mA	LVCMOS18_F2	$T_{OLVCMOS18\_F2}$	5.55	5.72	6.30	ns
LVCMOS, 1.8V, Fast, 4 mA	LVCMOS18_F4	$T_{OLVCMOS18\_F4}$	1.89	1.95	2.15	ns
LVCMOS, 1.8V, Fast, 6 mA	LVCMOS18_F6	$T_{OLVCMOS18\_F6}$	0.83	0.85	0.94	ns
LVCMOS, 1.8V, Fast, 8 mA	LVCMOS18_F8	$T_{OLVCMOS18\_F8}$	0.70	0.72	0.80	ns
LVCMOS, 1.8V, Fast, 12 mA	LVCMOS18_F12	$T_{OLVCMOS18\_F12}$	0.26	0.27	0.30	ns
LVCMOS, 1.8V, Fast, 16 mA	LVCMOS18_F16	$T_{OLVCMOS18\_F16}$	0.23	0.23	0.26	ns
LVCMOS, 1.5V, Slow, 2 mA	LVCMOS15_S2	$T_{OLVCMOS15\_S2}$	18.96	19.55	21.50	ns
LVCMOS, 1.5V, Slow, 4 mA	LVCMOS15_S4	$T_{OLVCMOS15\_S4}$	12.77	13.17	14.48	ns
LVCMOS, 1.5V, Slow, 6 mA	LVCMOS15_S6	$T_{OLVCMOS15\_S6}$	12.05	12.42	13.66	ns
LVCMOS, 1.5V, Slow, 8 mA	LVCMOS15_S8	$T_{OLVCMOS15\_S8}$	9.75	10.06	11.06	ns
LVCMOS, 1.5V, Slow, 12 mA	LVCMOS15_S12	$T_{OLVCMOS15\_S12}$	9.04	9.32	10.25	ns
LVCMOS, 1.5V, Slow, 16 mA	LVCMOS15_S16	$T_{OLVCMOS15\_S16}$	8.21	8.46	9.31	ns
LVCMOS, 1.5V, Fast, 2 mA	LVCMOS15_F2	$T_{OLVCMOS15\_F2}$	5.09	5.25	5.78	ns
LVCMOS, 1.5V, Fast, 4 mA	LVCMOS15_F4	$T_{OLVCMOS15\_F4}$	2.01	2.07	2.27	ns
LVCMOS, 1.5V, Fast, 6 mA	LVCMOS15_F6	$T_{OLVCMOS15\_F6}$	1.46	1.51	1.66	ns
LVCMOS, 1.5V, Fast, 8 mA	LVCMOS15_F8	$T_{OLVCMOS15\_F8}$	0.93	0.96	1.05	ns
LVCMOS, 1.5V, Fast, 12 mA	LVCMOS15_F12	$T_{OLVCMOS15\_F12}$	0.74	0.77	0.84	ns
LVCMOS, 1.5V, Fast, 16 mA	LVCMOS15_F16	$T_{OLVCMOS15\_F16}$	0.67	0.69	0.75	ns
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	T_{OLVDS_25}	–0.31	–0.32	–0.36	ns
LVDS, 3.3V	LVDS_33	T_{OLVDS_33}	–0.25	–0.26	–0.29	ns
LVDSEXT (LVDS Extended Mode), 2.5V	LVDSEXT_25	$T_{OLVDSEXT\_25}$	–0.18	–0.19	–0.21	ns
LVDSEXT, 3.3V	LVDSEXT_33	$T_{OLVDSEXT\_33}$	–0.17	–0.18	–0.19	ns
ULVDS (Ultra LVDS), 2.5V	ULVDS_25	T_{OULVDS_25}	–0.20	–0.21	–0.23	ns
BLVDS (Bus LVDS), 2.5V	BLVDS_25	T_{OBLVDS_25}	0.67	0.69	0.76	ns
LDT (HyperTransport), 2.5V	LDT_25	T_{OLDT_25}	–0.20	–0.21	–0.23	ns
LVPECL (Low-Voltage Positive Electron-Coupled Logic), 3.3V	LVPECL_33	$T_{OLVPECL\_33}$	0.29	0.30	0.33	ns
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3	T_{OPCI33_3}	1.15	1.19	1.31	ns
PCI, 66 MHz, 3.3V	PCI66_3	T_{OPCI66_3}	–0.01	–0.01	–0.01	ns
PCI-X, 133 MHz, 3.3V	PCIX	T_{OPCIX}	–0.01	–0.01	–0.01	ns
GTL (Gunning Transceiver Logic)	GTL	T_{OGTL}	–0.31	–0.32	–0.36	ns
GTL Plus	GTLP	T_{OGTLP}	–0.17	–0.18	–0.20	ns
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	T_{OHSTL_I}	0.26	0.27	0.29	ns
HSTL, Class II	HSTL_II	T_{OHSTL_II}	–0.15	–0.16	–0.17	ns
HSTL, Class III	HSTL_III	T_{OHSTL_III}	–0.17	–0.17	–0.19	ns
HSTL, Class IV	HSTL_IV	T_{OHSTL_IV}	–0.40	–0.41	–0.45	ns
HSTL, Class I, 1.8V	HSTL_I_18	$T_{OHSTL\_I\_18}$	0.03	0.03	0.04	ns

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *Without* DCM

Table 35: **Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *Without* DCM**

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
LVTTL Global Clock Input to Output Delay using Output flip-flop, 12 mA, Fast Slew Rate, *without* DCM. For data *output* with different standards, adjust the delays with the values shown in IOB Output Switching Characteristics Standard Adjustments, page 14.						
Global Clock and OFF without DCM	T_{ICKOF}	XC2V40	3.46	3.58	3.69	ns
		XC2V80	3.62	3.58	3.69	ns
		XC2V250	3.79	3.88	4.47	ns
		XC2V500	3.85	3.88	4.47	ns
		XC2V1000	4.02	4.28	4.62	ns
		XC2V1500	4.16	4.28	4.62	ns
		XC2V2000	4.30	4.43	5.10	ns
		XC2V3000	4.49	4.64	5.34	ns
		XC2V4000	4.82	4.99	5.74	ns
		XC2V6000	5.19	5.38	5.93	ns
		XC2V8000		6.09	7.00	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with test setup shown in Figure 1. For other I/O standards, see Table 19.

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
NA	VCCINT	R16		
NA	VCCINT	R7		
NA	VCCINT	H16		
NA	VCCINT	H7		
NA	VCCINT	G16		
NA	VCCINT	G15		
NA	VCCINT	G8		
NA	VCCINT	G7		
NA	VCCINT	F17		
NA	VCCINT	F6		
NA	GND	AB22		
NA	GND	AB1		
NA	GND	AA21		
NA	GND	AA2		
NA	GND	Y20		
NA	GND	Y3		
NA	GND	W19		
NA	GND	W4		
NA	GND	P14		
NA	GND	P13		
NA	GND	P12		
NA	GND	P11		
NA	GND	P10		
NA	GND	P9		
NA	GND	N14		
NA	GND	N13		
NA	GND	N12		
NA	GND	N11		
NA	GND	N10		
NA	GND	N9		
NA	GND	M14		
NA	GND	M13		
NA	GND	M12		
NA	GND	M11		

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
0	IO_L69P_0/VREF_0	B9	NC	
0	IO_L70N_0	F10	NC	
0	IO_L70P_0	E10	NC	
0	IO_L72N_0	A10	NC	
0	IO_L72P_0	A11	NC	
0	IO_L73N_0	C10	NC	NC
0	IO_L73P_0	B10	NC	NC
0	IO_L91N_0/VREF_0	D11		
0	IO_L91P_0	C11		
0	IO_L92N_0	G11		
0	IO_L92P_0	E11		
0	IO_L93N_0	C12		
0	IO_L93P_0	B12		
0	IO_L94N_0/VREF_0	E12		
0	IO_L94P_0	D12		
0	IO_L95N_0/GCLK7P	G12		
0	IO_L95P_0/GCLK6S	F12		
0	IO_L96N_0/GCLK5P	H11		
0	IO_L96P_0/GCLK4S	H12		
1	IO_L96N_1/GCLK3P	A13		
1	IO_L96P_1/GCLK2S	A14		
1	IO_L95N_1/GCLK1P	B13		
1	IO_L95P_1/GCLK0S	C13		
1	IO_L94N_1	D13		
1	IO_L94P_1/VREF_1	E13		
1	IO_L93N_1	F13		
1	IO_L93P_1	G13		
1	IO_L92N_1	H13		
1	IO_L92P_1	H14		
1	IO_L91N_1	C14		
1	IO_L91P_1/VREF_1	D14		
1	IO_L73N_1	E14	NC	NC
1	IO_L73P_1	G14	NC	NC
1	IO_L72N_1	A15	NC	
1	IO_L72P_1	A16	NC	

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
NA	VCCINT	K10
NA	GND	AG27
NA	GND	AG26
NA	GND	AG14
NA	GND	AG2
NA	GND	AG1
NA	GND	AF27
NA	GND	AF26
NA	GND	AF20
NA	GND	AF8
NA	GND	AF2
NA	GND	AF1
NA	GND	AE25
NA	GND	AE3
NA	GND	AD24
NA	GND	AD14
NA	GND	AD4
NA	GND	AC23
NA	GND	AC17
NA	GND	AC11
NA	GND	AC5
NA	GND	AB22
NA	GND	AB6
NA	GND	AA21
NA	GND	AA7
NA	GND	Y26
NA	GND	Y20
NA	GND	Y8
NA	GND	Y2
NA	GND	W14
NA	GND	U23
NA	GND	U5
NA	GND	T16
NA	GND	T15
NA	GND	T14
NA	GND	T13

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
4	IO_L19N_4	AK6		
4	IO_L19P_4	AK5		
4	IO_L20N_4	AE9		
4	IO_L20P_4	AE10		
4	IO_L21N_4	AF7		
4	IO_L21P_4/VREF_4	AF8		
4	IO_L22N_4	AK7		
4	IO_L22P_4	AJ6		
4	IO_L23N_4	AD10		
4	IO_L23P_4	AD11		
4	IO_L24N_4	AG8		
4	IO_L24P_4	AG7		
4	IO_L49N_4	AJ8		
4	IO_L49P_4	AJ7		
4	IO_L50N_4	AE11		
4	IO_L50P_4	AE12		
4	IO_L51N_4	AG9		
4	IO_L51P_4/VREF_4	AG10		
4	IO_L52N_4	AK9		
4	IO_L52P_4	AJ9		
4	IO_L53N_4	AH8		
4	IO_L53P_4	AH9		
4	IO_L54N_4	AF11		
4	IO_L54P_4	AF10		
4	IO_L67N_4	AJ11	NC	
4	IO_L67P_4	AJ10	NC	
4	IO_L68N_4	AC12	NC	
4	IO_L68P_4	AC13	NC	
4	IO_L69N_4	AG11	NC	
4	IO_L69P_4/VREF_4	AG12	NC	
4	IO_L70N_4	AK11	NC	
4	IO_L70P_4	AK10	NC	
4	IO_L71N_4	AD12	NC	
4	IO_L71P_4	AD13	NC	
4	IO_L72N_4	AH12	NC	
4	IO_L72P_4	AH11	NC	
4	IO_L73N_4	AJ13	NC	NC

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
5	IO_L23N_5	AD20		
5	IO_L23P_5	AD21		
5	IO_L22N_5	AK25		
5	IO_L22P_5	AK24		
5	IO_L21N_5/VREF_5	AH24		
5	IO_L21P_5	AH25		
5	IO_L20N_5	AE21		
5	IO_L20P_5	AD22		
5	IO_L19N_5	AJ25		
5	IO_L19P_5	AJ24		
5	IO_L06N_5	AG25		
5	IO_L06P_5	AG24		
5	IO_L05N_5/VRP_5	AC20		
5	IO_L05P_5/VRN_5	AC21		
5	IO_L04N_5	AK26		
5	IO_L04P_5/VREF_5	AK27		
5	IO_L03N_5/D4/ALT_VRP_5	AH26		
5	IO_L03P_5/D5/ALT_VRN_5	AJ27		
5	IO_L02N_5/D6	AE22		
5	IO_L02P_5/D7	AE23		
5	IO_L01N_5/RDWR_B	AJ28		
5	IO_L01P_5/CS_B	AK29		
6	IO_L01P_6	AC22		
6	IO_L01N_6	AB23		
6	IO_L02P_6/VRN_6	AG28		
6	IO_L02N_6/VRP_6	AF28		
6	IO_L03P_6	AJ30		
6	IO_L03N_6/VREF_6	AH30		
6	IO_L04P_6	AD23		
6	IO_L04N_6	AC23		
6	IO_L05P_6	AF27		
6	IO_L05N_6	AE27		
6	IO_L06P_6	AG29		
6	IO_L06N_6	AH29		
6	IO_L19P_6	AE24		
6	IO_L19N_6	AD24		

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
7	IO_L45N_7	J34	
7	IO_L44P_7	M27	
7	IO_L44N_7	L27	
7	IO_L43P_7	H31	
7	IO_L43N_7	J31	
7	IO_L30P_7	F32	
7	IO_L30N_7	G32	
7	IO_L29P_7	N25	
7	IO_L29N_7	M25	
7	IO_L28P_7	F34	
7	IO_L28N_7	G34	
7	IO_L27P_7/VREF_7	J30	
7	IO_L27N_7	H30	
7	IO_L26P_7	K28	
7	IO_L26N_7	L28	
7	IO_L25P_7	H28	
7	IO_L25N_7	J29	
7	IO_L24P_7	G29	
7	IO_L24N_7	H29	
7	IO_L23P_7	L26	
7	IO_L23N_7	K26	
7	IO_L22P_7	F33	
7	IO_L22N_7	G33	
7	IO_L21P_7/VREF_7	J28	
7	IO_L21N_7	J27	
7	IO_L20P_7	K27	
7	IO_L20N_7	J26	
7	IO_L19P_7	E31	
7	IO_L19N_7	F31	
7	IO_L06P_7	D32	
7	IO_L06N_7	E32	
7	IO_L05P_7	L25	
7	IO_L05N_7	K24	
7	IO_L04P_7	D34	
7	IO_L04N_7	E34	
7	IO_L03P_7/VREF_7	G30	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
1	IO_L93N_1	E19		
1	IO_L93P_1	E20		
1	IO_L92N_1	J19		
1	IO_L92P_1	J18		
1	IO_L91N_1	A18		
1	IO_L91P_1/VREF_1	A19		
1	IO_L84N_1	D18		
1	IO_L84P_1	D19		
1	IO_L83N_1	K19		
1	IO_L83P_1	K18		
1	IO_L82N_1	B18		
1	IO_L82P_1	B19		
1	IO_L81N_1/VREF_1	G18		
1	IO_L81P_1	G19		
1	IO_L80N_1	E18		
1	IO_L80P_1	E17		
1	IO_L79N_1	A16		
1	IO_L79P_1	A17		
1	IO_L78N_1	F17		
1	IO_L78P_1	F18		
1	IO_L77N_1	L19		
1	IO_L77P_1	L18		
1	IO_L76N_1	B16		
1	IO_L76P_1	B17		
1	IO_L75N_1/VREF_1	G16		
1	IO_L75P_1	G17		
1	IO_L74N_1	M19		
1	IO_L74P_1	M18		
1	IO_L73N_1	C16		
1	IO_L73P_1	C17		
1	IO_L72N_1	D15		
1	IO_L72P_1	D16		
1	IO_L71N_1	J17		
1	IO_L71P_1	J16		
1	IO_L70N_1	A14		
1	IO_L70P_1	A15		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
5	IO_L79N_5	AV24		
5	IO_L79P_5	AV23		
5	IO_L78N_5	AP23		
5	IO_L78P_5	AP22		
5	IO_L77N_5	AJ21		
5	IO_L77P_5	AJ22		
5	IO_L76N_5	AU24		
5	IO_L76P_5	AU23		
5	IO_L75N_5/VREF_5	AT25		
5	IO_L75P_5	AT24		
5	IO_L74N_5	AH21		
5	IO_L74P_5	AH22		
5	IO_L73N_5	AW26		
5	IO_L73P_5	AW25		
5	IO_L72N_5	AR25		
5	IO_L72P_5	AR24		
5	IO_L71N_5	AN23		
5	IO_L71P_5	AN24		
5	IO_L70N_5	AU25		
5	IO_L70P_5	AV25		
5	IO_L69N_5/VREF_5	AL24		
5	IO_L69P_5	AL23		
5	IO_L68N_5	AK23		
5	IO_L68P_5	AK24		
5	IO_L67N_5	AU27		
5	IO_L67P_5	AU26		
5	IO_L60N_5	AP25		
5	IO_L60P_5	AP24		
5	IO_L59N_5	AM24		
5	IO_L59P_5	AM25		
5	IO_L58N_5	AW28		
5	IO_L58P_5	AW27		
5	IO_L57N_5/VREF_5	AT27		
5	IO_L57P_5	AT26		
5	IO_L56N_5	AH23		
5	IO_L56P_5	AH24		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
1	VCCO_1	E11		
1	VCCO_1	C18		
1	VCCO_1	B14		
2	VCCO_2	W14		
2	VCCO_2	W13		
2	VCCO_2	V14		
2	VCCO_2	V13		
2	VCCO_2	V3		
2	VCCO_2	U14		
2	VCCO_2	U13		
2	VCCO_2	U11		
2	VCCO_2	T14		
2	VCCO_2	T13		
2	VCCO_2	R14		
2	VCCO_2	R13		
2	VCCO_2	R9		
2	VCCO_2	P13		
2	VCCO_2	P2		
2	VCCO_2	N7		
2	VCCO_2	L5		
3	VCCO_3	AJ5		
3	VCCO_3	AG7		
3	VCCO_3	AF13		
3	VCCO_3	AF2		
3	VCCO_3	AE14		
3	VCCO_3	AE13		
3	VCCO_3	AE9		
3	VCCO_3	AD14		
3	VCCO_3	AD13		
3	VCCO_3	AC14		
3	VCCO_3	AC13		
3	VCCO_3	AC11		
3	VCCO_3	AB14		
3	VCCO_3	AB13		
3	VCCO_3	AB3		
3	VCCO_3	AA14		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	VCCINT	R19		
NA	VCCINT	R18		
NA	VCCINT	R17		
NA	VCCINT	R16		
NA	VCCINT	R15		
NA	VCCINT	P26		
NA	VCCINT	P20		
NA	VCCINT	P14		
NA	VCCINT	N27		
NA	VCCINT	N20		
NA	VCCINT	N13		
NA	GND	AW38		
NA	GND	AW37		
NA	GND	AW20		
NA	GND	AW3		
NA	GND	AW2		
NA	GND	AV39		
NA	GND	AV38		
NA	GND	AV37		
NA	GND	AV29		
NA	GND	AV11		
NA	GND	AV3		
NA	GND	AV2		
NA	GND	AV1		
NA	GND	AU39		
NA	GND	AU38		
NA	GND	AU37		
NA	GND	AU3		
NA	GND	AU2		
NA	GND	AU1		
NA	GND	AT36		
NA	GND	AT23		
NA	GND	AT20		
NA	GND	AT17		
NA	GND	AT4		
NA	GND	AR35		

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
0	IO_L92N_0	F17	
0	IO_L92P_0	F16	
0	IO_L93N_0	B18	
0	IO_L93P_0	B17	
0	IO_L94N_0/VREF_0	J17	
0	IO_L94P_0	J16	
0	IO_L95N_0/GCLK7P	E17	
0	IO_L95P_0/GCLK6S	E16	
0	IO_L96N_0/GCLK5P	A18	
0	IO_L96P_0/GCLK4S	A17	
1	IO_L96N_1/GCLK3P	C16	
1	IO_L96P_1/GCLK2S	C15	
1	IO_L95N_1/GCLK1P	H16	
1	IO_L95P_1/GCLK0S	H15	
1	IO_L94N_1	A15	
1	IO_L94P_1/VREF_1	A14	
1	IO_L93N_1	F15	
1	IO_L93P_1	F14	
1	IO_L92N_1	G15	
1	IO_L92P_1	G14	
1	IO_L91N_1	B15	
1	IO_L91P_1/VREF_1	B14	
1	IO_L78N_1	D15	
1	IO_L78P_1	E15	
1	IO_L77N_1	J15	
1	IO_L77P_1	K14	
1	IO_L76N_1	D14	
1	IO_L76P_1	D13	
1	IO_L75N_1/VREF_1	E14	
1	IO_L75P_1	E13	
1	IO_L74N_1	A13	
1	IO_L74P_1	A12	
1	IO_L73N_1	F13	
1	IO_L73P_1	F12	
1	IO_L72N_1	J14	
1	IO_L72P_1	J13	
1	IO_L71N_1	B13	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
1	IO_L21P_1	A4	
1	IO_L20N_1	G10	
1	IO_L20P_1	G9	
1	IO_L19N_1	B6	
1	IO_L19P_1	C5	
1	IO_L06N_1	C6	
1	IO_L06P_1	D6	
1	IO_L05N_1	H9	
1	IO_L05P_1	G8	
1	IO_L04N_1	D7	
1	IO_L04P_1/VREF_1	E6	
1	IO_L03N_1/VRP_1	E8	
1	IO_L03P_1/VRN_1	E7	
1	IO_L02N_1	F8	
1	IO_L02P_1	F7	
1	IO_L01N_1	B5	
1	IO_L01P_1	B3	
2	IO_L01N_2	F5	
2	IO_L01P_2	G4	
2	IO_L02N_2/VRP_2	G6	
2	IO_L02P_2/VRN_2	H6	
2	IO_L03N_2	D3	
2	IO_L03P_2/VREF_2	E4	
2	IO_L04N_2	K10	
2	IO_L04P_2	K9	
2	IO_L05N_2	D2	
2	IO_L05P_2	E3	
2	IO_L06N_2	F4	
2	IO_L06P_2	F3	
2	IO_L19N_2	L10	
2	IO_L19P_2	M10	
2	IO_L20N_2	H7	
2	IO_L20P_2	J8	
2	IO_L21N_2	D1	
2	IO_L21P_2/VREF_2	E1	
2	IO_L22N_2	G5	
2	IO_L22P_2	H5	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
4	IO_L29N_4	AL6	NC
4	IO_L29P_4	AL7	NC
4	IO_L30N_4	AJ9	NC
4	IO_L30P_4	AJ10	NC
4	IO_L49N_4	AE11	
4	IO_L49P_4	AE12	
4	IO_L50N_4	AG10	
4	IO_L50P_4	AG11	
4	IO_L51N_4	AL8	
4	IO_L51P_4/VREF_4	AL9	
4	IO_L52N_4	AF12	
4	IO_L52P_4	AF13	
4	IO_L53N_4	AK9	
4	IO_L53P_4	AK10	
4	IO_L54N_4	AH11	
4	IO_L54P_4	AH12	
4	IO_L67N_4	AC12	
4	IO_L67P_4	AC13	
4	IO_L68N_4	AG12	
4	IO_L68P_4	AG13	
4	IO_L69N_4	AL10	
4	IO_L69P_4/VREF_4	AL11	
4	IO_L70N_4	AD13	
4	IO_L70P_4	AD15	
4	IO_L71N_4	AJ11	
4	IO_L71P_4	AJ12	
4	IO_L72N_4	AK11	
4	IO_L72P_4	AK12	
4	IO_L73N_4	AE14	
4	IO_L73P_4	AE15	
4	IO_L74N_4	AF14	
4	IO_L74P_4	AF15	
4	IO_L75N_4	AL12	
4	IO_L75P_4/VREF_4	AL13	
4	IO_L76N_4	AB14	
4	IO_L76P_4	AC14	
4	IO_L77N_4	AH13	
4	IO_L77P_4	AH14	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
2	VCCO_2	N12	
2	VCCO_2	P3	
2	VCCO_2	P8	
2	VCCO_2	P11	
2	VCCO_2	P12	
2	VCCO_2	R11	
2	VCCO_2	R12	
3	VCCO_3	U11	
3	VCCO_3	U12	
3	VCCO_3	V3	
3	VCCO_3	V8	
3	VCCO_3	V11	
3	VCCO_3	V12	
3	VCCO_3	W11	
3	VCCO_3	W12	
3	VCCO_3	Y11	
3	VCCO_3	AB6	
3	VCCO_3	AE3	
4	VCCO_4	Y13	
4	VCCO_4	Y14	
4	VCCO_4	Y15	
4	VCCO_4	AA12	
4	VCCO_4	AA13	
4	VCCO_4	AA14	
4	VCCO_4	AA15	
4	VCCO_4	AD14	
4	VCCO_4	AF10	
4	VCCO_4	AJ7	
4	VCCO_4	AJ14	
5	VCCO_5	Y17	
5	VCCO_5	Y18	
5	VCCO_5	Y19	
5	VCCO_5	AA17	
5	VCCO_5	AA18	
5	VCCO_5	AA19	
5	VCCO_5	AA20	
5	VCCO_5	AD18	
5	VCCO_5	AF22	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
NA	GND	D10	
NA	GND	D16	
NA	GND	D22	
NA	GND	D28	
NA	GND	E5	
NA	GND	E27	
NA	GND	F6	
NA	GND	F26	
NA	GND	G7	
NA	GND	G13	
NA	GND	G16	
NA	GND	G19	
NA	GND	G25	
NA	GND	H2	
NA	GND	H8	
NA	GND	H24	
NA	GND	H30	
NA	GND	J9	
NA	GND	J23	
NA	GND	K4	
NA	GND	K16	
NA	GND	K28	
NA	GND	N7	
NA	GND	N25	
NA	GND	P14	
NA	GND	P15	
NA	GND	P16	
NA	GND	P17	
NA	GND	P18	
NA	GND	R14	
NA	GND	R15	
NA	GND	R16	
NA	GND	R17	
NA	GND	R18	
NA	GND	T1	
NA	GND	T4	
NA	GND	T7	
NA	GND	T10	