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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	384
Number of Logic Elements/Cells	-
Total RAM Bits	442368
Number of I/O	200
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v250-5fgg456c

Table 5: Summary of Voltage Supply Requirements for All Input and Output Standards

I/O Standard	V _{CCO}		V _{REF}	Termination Type	
	Output	Input	Input	Output	Input
LVDS_33	3.3	N/R	N/R ⁽¹⁾	N/R	N/R
LVDSEXT_33			N/R	N/R	N/R
LVPECL_33			N/R	N/R	N/R
SSTL3_I			1.5	N/R	N/R
SSTL3_II			1.5	N/R	N/R
AGP			1.32	N/R	N/R
LVTTTL		3.3	N/R	N/R	N/R
LVC MOS33			N/R	N/R	N/R
LVDCI_33			N/R	Series	N/R
LVDCI_DV2_33			N/R	Series	N/R
PCI33_3			N/R	N/R	N/R
PCI66_3			N/R	N/R	N/R
PCI X			N/R	N/R	N/R
SSTL3_I_DCI			1.5	N/R	Split
SSTL3_II_DCI			1.5	Split	Split
LVDS_25	2.5	N/R	N/R	N/R	N/R
LVDSEXT_25			N/R	N/R	N/R
LDT_25			N/R	N/R	N/R
ULVDS_25			N/R	N/R	N/R
BLVDS_25			N/R	N/R	N/R
SSTL2_I			1.25	N/R	N/R
SSTL2_II			1.25	N/R	N/R
LVC MOS25		2.5	N/R	N/R	N/R
LVDCI_25			N/R	Series	N/R
LVDCI_DV2_25			N/R	Series	N/R
LVDS_25_DCI			N/R	N/R	Split
LVDSEXT_25_DC I			N/R	N/R	Split
SSTL2_I_DCI			1.25	N/R	Split
SSTL2_II_DCI			1.25	Split	Split

Table 5: Summary of Voltage Supply Requirements for All Input and Output Standards (Continued)

I/O Standard	V _{CCO}		V _{REF}	Termination Type	
	Output	Input	Input	Output	Input
HSTL_III_18	1.8	N/R	1.1	N/R	N/R
HSTL_IV_18			1.1	N/R	N/R
HSTL_I_18			0.9	N/R	N/R
HSTL_II_18			0.9	N/R	N/R
SSTL18_I			0.9	N/R	N/R
SSTL18_II			0.9	N/R	N/R
LVC MOS18		1.8	N/R	N/R	N/R
LVDCI_18			N/R	Series	N/R
LVDCI_DV2_18			N/R	Series	N/R
HSTL_III_DCI_18			1.1	N/R	Single
HSTL_IV_DCI_18			1.1	Single	Single
HSTL_I_DCI_18			0.9	N/R	Split
HSTL_II_DCI_18			0.9	Split	Split
SSTL18_I_DCI			0.9	N/R	Split
SSTL18_II_DCI			0.9	Split	Split
HSTL_III	1.5	N/R	0.9	N/R	N/R
HSTL_IV			0.9	N/R	N/R
HSTL_I			0.75	N/R	N/R
HSTL_II			0.75	N/R	N/R
LVC MOS15		1.5	N/R	N/R	N/R
LVDCI_15			N/R	Series	N/R
LVDCI_DV2_15			N/R	Series	N/R
GTLP_DCI			1	Single	Single
HSTL_III_DCI			0.9	N/R	Single
HSTL_IV_DCI			0.9	Single	Single
HSTL_I_DCI			0.75	N/R	Split
HSTL_II_DCI			0.75	Split	Split
GTLP	1.2	1.2	0.8	Single	Single
GTLP	N/R	N/R	1	N/R	N/R
GTL			0.8	N/R	N/R

Notes:

1. N/R = no requirement.

Sum of Products

Each Virtex-II slice has a dedicated OR gate named ORCY, ORing together outputs from the slices carryout and the ORCY from an adjacent slice. The ORCY gate with the dedicated Sum of Products (SOP) chain are designed for implementing

large, flexible SOP chains. One input of each ORCY is connected through the fast SOP chain to the output of the previous ORCY in the same slice row. The second input is connected to the output of the top MUXCY in the same slice, as shown in Figure 25.

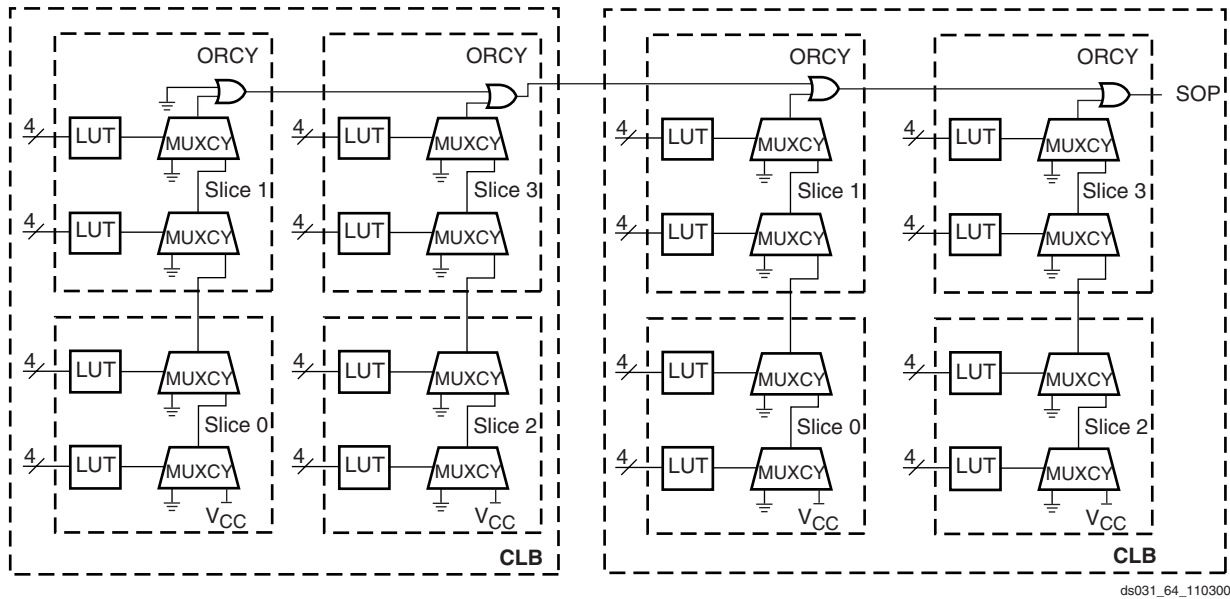


Figure 25: Horizontal Cascade Chain

LUTs and MUXCYs can implement large AND gates or other combinational logic functions. Figure 26 illustrates

LUT and MUXCY resources configured as a 16-input AND gate.

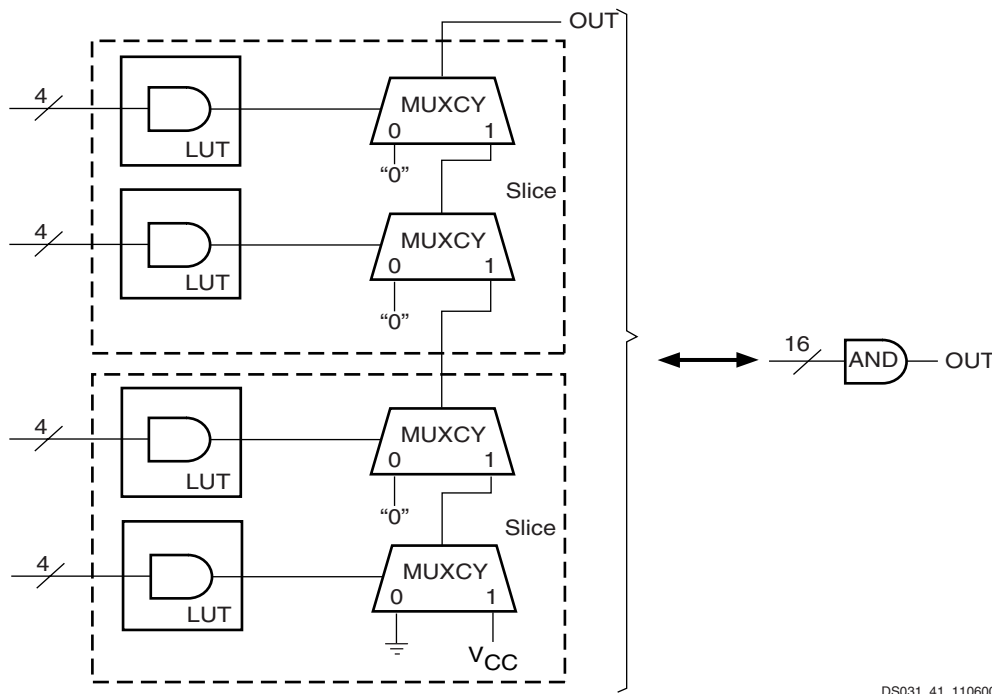


Figure 26: Wide-Input AND Gate (16 Inputs)

Table 27: Enhanced Pipelined Multiplier Switching Characteristics

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Setup and Hold Times Before/After Clock					
Data Inputs	T _{MULIDCK} /T _{MULCKID}	3.00/0.00	3.45/0.00	3.89/0.00	ns, Max
Clock Enable	T _{MULIDCK_CE} /T _{MULCKID_CE}	0.72/0.00	0.80/0.00	0.86/0.00	ns, Max
Reset	T _{MULIDCK_RST} /T _{MULCKID_RST}	0.72/0.00	0.80/0.00	0.86/0.00	ns, Max
Clock to Output Pin					
Clock to Pin 35	T _{MULTCK1_P35}	3.05	3.25	3.74	ns, Max
Clock to Pin 34	T _{MULTCK1_P34}	2.95	3.14	3.61	ns, Max
Clock to Pin 33	T _{MULTCK1_P33}	2.85	3.04	3.49	ns, Max
Clock to Pin 32	T _{MULTCK1_P32}	2.76	2.93	3.37	ns, Max
Clock to Pin 31	T _{MULTCK1_P31}	2.66	2.82	3.25	ns, Max
Clock to Pin 30	T _{MULTCK1_P30}	2.56	2.72	3.12	ns, Max
Clock to Pin 29	T _{MULTCK1_P29}	2.47	2.61	3.00	ns, Max
Clock to Pin 28	T _{MULTCK1_P28}	2.37	2.50	2.88	ns, Max
Clock to Pin 27	T _{MULTCK1_P27}	2.27	2.40	2.75	ns, Max
Clock to Pin 26	T _{MULTCK1_P26}	2.17	2.29	2.63	ns, Max
Clock to Pin 25	T _{MULTCK1_P25}	2.08	2.18	2.51	ns, Max
Clock to Pin 24	T _{MULTCK1_P24}	1.98	2.07	2.38	ns, Max
Clock to Pin 23	T _{MULTCK1_P23}	1.88	1.97	2.26	ns, Max
Clock to Pin 22	T _{MULTCK1_P22}	1.79	1.86	2.14	ns, Max
Clock to Pin 21	T _{MULTCK1_P21}	1.69	1.75	2.02	ns, Max
Clock to Pin 20	T _{MULTCK1_P20}	1.59	1.65	1.89	ns, Max
Clock to Pin 19	T _{MULTCK1_P19}	1.50	1.54	1.77	ns, Max
Clock to Pin 18	T _{MULTCK1_P18}	1.40	1.43	1.65	ns, Max
Clock to Pin 17	T _{MULTCK1_P17}	1.30	1.33	1.52	ns, Max
Clock to Pin 16	T _{MULTCK1_P16}	1.20	1.22	1.40	ns, Max
Clock to Pin 15	T _{MULTCK1_P15}	1.11	1.11	1.28	ns, Max
Clock to Pin 14	T _{MULTCK1_P14}	1.01	1.00	1.15	ns, Max
Clock to Pin 13	T _{MULTCK1_P13}	0.91	1.00	1.15	ns, Max
Clock to Pin 12	T _{MULTCK1_P12}	0.91	1.00	1.15	ns, Max
Clock to Pin 11	T _{MULTCK1_P11}	0.91	1.00	1.15	ns, Max
Clock to Pin 10	T _{MULTCK1_P10}	0.91	1.00	1.15	ns, Max
Clock to Pin 9	T _{MULTCK1_P9}	0.91	1.00	1.15	ns, Max
Clock to Pin 8	T _{MULTCK1_P8}	0.91	1.00	1.15	ns, Max
Clock to Pin 7	T _{MULTCK1_P7}	0.91	1.00	1.15	ns, Max
Clock to Pin 6	T _{MULTCK1_P6}	0.91	1.00	1.15	ns, Max
Clock to Pin 5	T _{MULTCK1_P5}	0.91	1.00	1.15	ns, Max
Clock to Pin 4	T _{MULTCK1_P4}	0.91	1.00	1.15	ns, Max
Clock to Pin 3	T _{MULTCK1_P3}	0.91	1.00	1.15	ns, Max
Clock to Pin 2	T _{MULTCK1_P2}	0.91	1.00	1.15	ns, Max
Clock to Pin 1	T _{MULTCK1_P1}	0.91	1.00	1.15	ns, Max
Clock to Pin 0	T _{MULTCK1_P0}	0.91	1.00	1.15	ns, Max

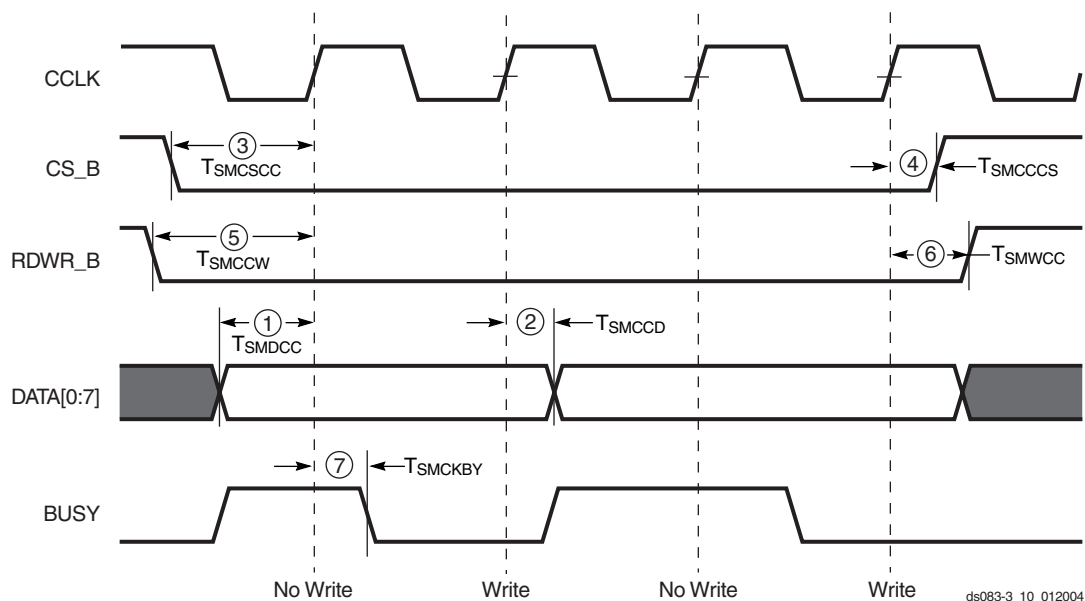


Figure 5: SelectMAP Mode Data Loading Sequence (Generic)

Table 32: SelectMAP Mode Write Timing Characteristics

	Description	Figure References	Symbol	Value	Units
CCLK	DATA[0:7] setup/hold	1/2	T_{SMDCC}/T_{SMCCD}	5.0/0.0	ns, min
	CS_B setup/hold	3/4	T_{SMCSCC}/T_{SMCCCS}	7.0/0.0	ns, min
	RDWR_B setup/hold	5/6	T_{SMCCW}/T_{SMWCC}	7.0/0.0	ns, min
	BUSY propagation delay	7	T_{SMCKBY}	12.0	ns, max
	Maximum start-up frequency		$F_{CC_STARTUP}$	50	MHz, max
	Maximum frequency		$F_{CC_SELECTMAP}$	50	MHz, max
	Maximum frequency with no handshake		F_{CCNH}	50	MHz, max

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *Without* DCM

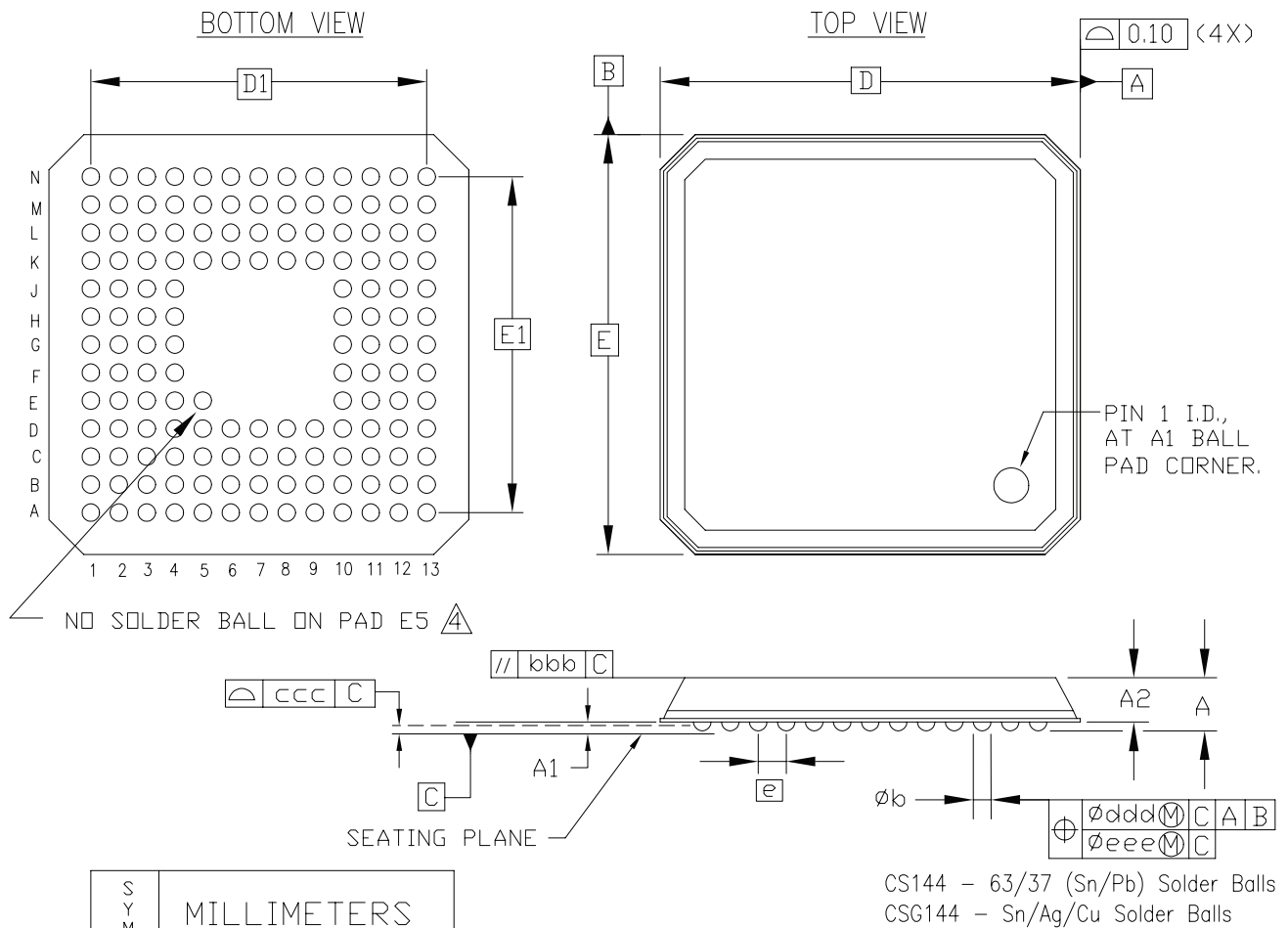
Table 35: Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *Without* DCM

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
LVTTL Global Clock Input to Output Delay using Output flip-flop, 12 mA, Fast Slew Rate, <i>without</i> DCM. For data <i>output</i> with different standards, adjust the delays with the values shown in <i>IOB Output Switching Characteristics Standard Adjustments</i> , page 14.						
Global Clock and OFF without DCM	T _{ICKOF}	XC2V40	3.46	3.58	3.69	ns
		XC2V80	3.62	3.58	3.69	ns
		XC2V250	3.79	3.88	4.47	ns
		XC2V500	3.85	3.88	4.47	ns
		XC2V1000	4.02	4.28	4.62	ns
		XC2V1500	4.16	4.28	4.62	ns
		XC2V2000	4.30	4.43	5.10	ns
		XC2V3000	4.49	4.64	5.34	ns
		XC2V4000	4.82	4.99	5.74	ns
		XC2V6000	5.19	5.38	5.93	ns
		XC2V8000		6.09	7.00	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with test setup shown in [Figure 1](#). For other I/O standards, see [Table 19](#).

CS144/CSG144 Chip-Scale BGA Package Specifications (0.80mm pitch)



144-BALL CHIP SCALE BGA (CS144/CSG144)

Figure 1: CS144/CSG144 Chip-Scale BGA Package Specifications

Table 7: FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
4	IO_L02N_4/D0/DIN ⁽¹⁾	V18		
4	IO_L02P_4/D1	V17		
4	IO_L03N_4/D2/ALT_VRP_4	W18		
4	IO_L03P_4/D3/ALT_VRN_4	Y18		
4	IO_L04N_4/VREF_4	AA18		
4	IO_L04P_4	AB18		
4	IO_L05N_4/VRP_4	W17		
4	IO_L05P_4/VRN_4	Y17		
4	IO_L06N_4	AA17		
4	IO_L06P_4	AB17		
4	IO_L19N_4	V16	NC	NC
4	IO_L19P_4	V15	NC	NC
4	IO_L21N_4	W16	NC	NC
4	IO_L21P_4/VREF_4	Y16	NC	NC
4	IO_L22N_4	AA16	NC	NC
4	IO_L22P_4	AB16	NC	NC
4	IO_L24N_4	W15	NC	NC
4	IO_L24P_4	Y15	NC	NC
4	IO_L49N_4	AA15	NC	
4	IO_L49P_4	AB15	NC	
4	IO_L51N_4	U14	NC	
4	IO_L51P_4/VREF_4	V14	NC	
4	IO_L52N_4	W14	NC	
4	IO_L52P_4	Y14	NC	
4	IO_L54N_4	AA14	NC	
4	IO_L54P_4	AB14	NC	
4	IO_L91N_4/VREF_4	U13		
4	IO_L91P_4	V13		
4	IO_L92N_4	W13		
4	IO_L92P_4	Y13		
4	IO_L93N_4	AA13		
4	IO_L93P_4	AB13		
4	IO_L94N_4/VREF_4	U12		
4	IO_L94P_4	V12		

Table 7: FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
4	IO_L95N_4/GCLK3S	W12		
4	IO_L95P_4/GCLK2P	Y12		
4	IO_L96N_4/GCLK1S	AA12		
4	IO_L96P_4/GCLK0P	AB12		
5	IO_L96N_5/GCLK7S	AA11		
5	IO_L96P_5/GCLK6P	Y11		
5	IO_L95N_5/GCLK5S	W11		
5	IO_L95P_5/GCLK4P	V11		
5	IO_L94N_5	U11		
5	IO_L94P_5/VREF_5	U10		
5	IO_L93N_5	AB10		
5	IO_L93P_5	AA10		
5	IO_L92N_5	Y10		
5	IO_L92P_5	W10		
5	IO_L91N_5	V10		
5	IO_L91P_5/VREF_5	V9		
5	IO_L54N_5	AB9	NC	
5	IO_L54P_5	AA9	NC	
5	IO_L52N_5	Y9	NC	
5	IO_L52P_5	W9	NC	
5	IO_L51N_5/VREF_5	AB8	NC	
5	IO_L51P_5	AA8	NC	
5	IO_L49N_5	Y8	NC	
5	IO_L49P_5	W8	NC	
5	IO_L24N_5	U9	NC	NC
5	IO_L24P_5	V8	NC	NC
5	IO_L22N_5	AB7	NC	NC
5	IO_L22P_5	AA7	NC	NC
5	IO_L21N_5/VREF_5	Y7	NC	NC
5	IO_L21P_5	W7	NC	NC
5	IO_L19N_5	AB6	NC	NC
5	IO_L19P_5	AA6	NC	NC
5	IO_L06N_5	Y6		

Table 8: FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
2	IO_L45N_2	H23		
2	IO_L45P_2/VREF_2	H24		
2	IO_L46N_2	J21		
2	IO_L46P_2	J20		
2	IO_L48N_2	H25		
2	IO_L48P_2	H26		
2	IO_L49N_2	J22		
2	IO_L49P_2	J23		
2	IO_L51N_2	K21		
2	IO_L51P_2/VREF_2	K22		
2	IO_L52N_2	K20		
2	IO_L52P_2	L20		
2	IO_L54N_2	J24		
2	IO_L54P_2	J25		
2	IO_L67N_2	K23		
2	IO_L67P_2	K24		
2	IO_L69N_2	J26		
2	IO_L69P_2/VREF_2	K26		
2	IO_L70N_2	L22		
2	IO_L70P_2	L21		
2	IO_L72N_2	L25		
2	IO_L72P_2	L26		
2	IO_L73N_2	L19	NC	
2	IO_L73P_2	M19	NC	
2	IO_L75N_2	L23	NC	
2	IO_L75P_2/VREF_2	L24	NC	
2	IO_L76N_2	M22	NC	
2	IO_L76P_2	M21	NC	
2	IO_L78N_2	M23	NC	
2	IO_L78P_2	M24	NC	
2	IO_L91N_2	M25		
2	IO_L91P_2	M26		
2	IO_L93N_2	M20		
2	IO_L93P_2/VREF_2	N20		
2	IO_L94N_2	N22		
2	IO_L94P_2	N21		
2	IO_L96N_2	N24		

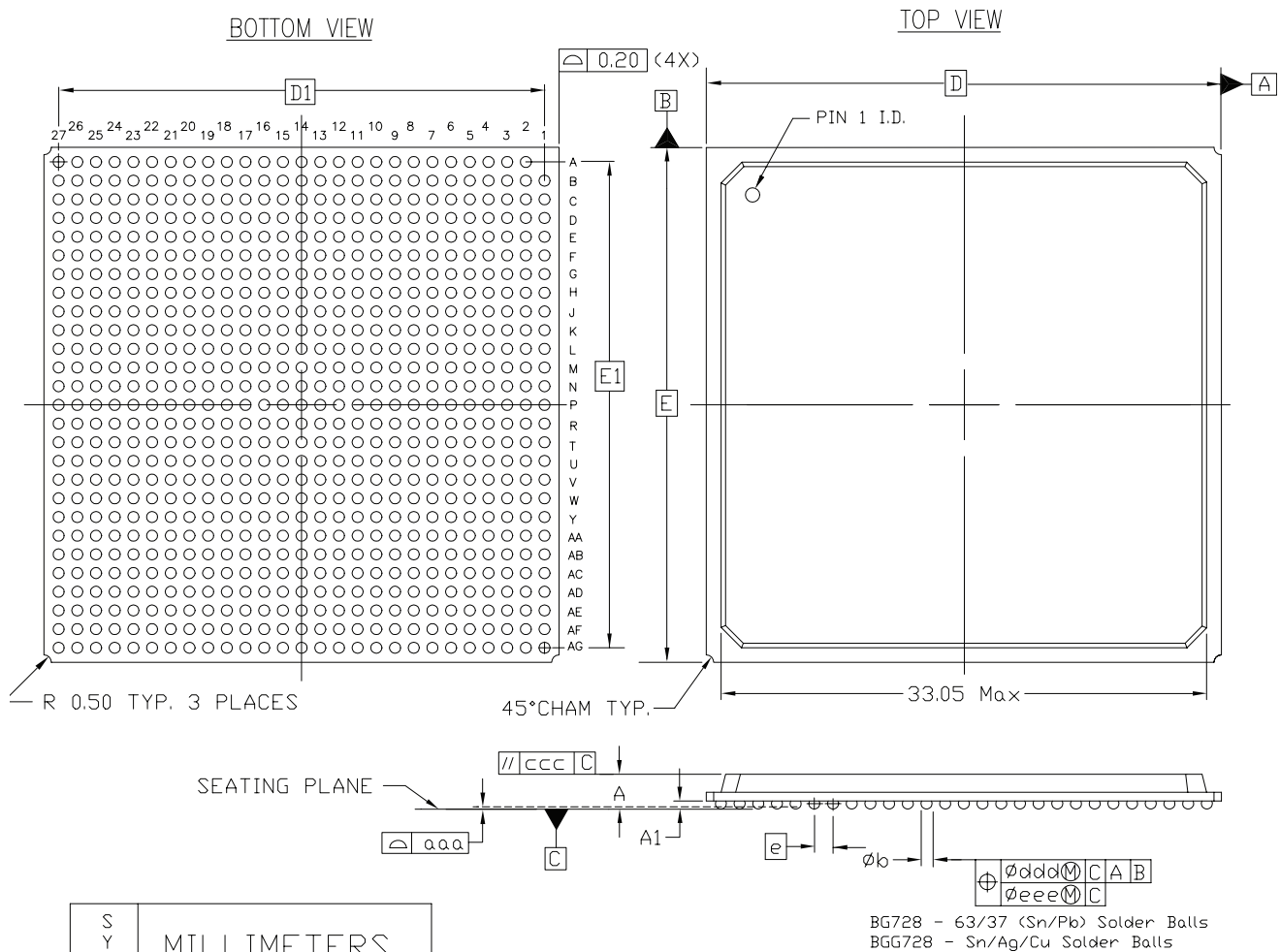
Table 8: FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
5	IO_L70N_5	W11		
5	IO_L70P_5	Y10		
5	IO_L69N_5/VREF_5	Y11		
5	IO_L69P_5	AA11		
5	IO_L67N_5	AF9		
5	IO_L67P_5	AF8		
5	IO_L54N_5	AE9		
5	IO_L54P_5	AD9		
5	IO_L52N_5	AB10		
5	IO_L52P_5	AA10		
5	IO_L51N_5/VREF_5	AD10		
5	IO_L51P_5	AC10		
5	IO_L49N_5	AE8		
5	IO_L49P_5	AF7		
5	IO_L28N_5	AD8	NC	NC
5	IO_L28P_5	AC8	NC	NC
5	IO_L27N_5/VREF_5	AB9	NC	NC
5	IO_L27P_5	AC9	NC	NC
5	IO_L25N_5	AA9	NC	NC
5	IO_L25P_5	Y9	NC	NC
5	IO_L24N_5	AF6		
5	IO_L24P_5	AE6		
5	IO_L22N_5	AB8		
5	IO_L22P_5	AA8		
5	IO_L21N_5/VREF_5	AC7		
5	IO_L21P_5	AD7		
5	IO_L19N_5	AF5		
5	IO_L19P_5	AE5		
5	IO_L06N_5	AF4		
5	IO_L06P_5	AE4		
5	IO_L05N_5/VRP_5	AF3		
5	IO_L05P_5/VRN_5	AE3		
5	IO_L04N_5	Y8		
5	IO_L04P_5/VREF_5	Y7		
5	IO_L03N_5/D4/ALT_VRP_5	AB7		
5	IO_L03P_5/D5/ALT_VRN_5	AA7		
5	IO_L02N_5/D6	AD6		

Table 10: BG728 BGA — XC2V3000

Bank	Pin Description	Pin Number
7	IO_L27P_7/VREF_7	H5
7	IO_L27N_7	H6
7	IO_L25P_7	J7
7	IO_L25N_7	J8
7	IO_L24P_7	G1
7	IO_L24N_7	F1
7	IO_L22P_7	G2
7	IO_L22N_7	G3
7	IO_L21P_7/VREF_7	F2
7	IO_L21N_7	F3
7	IO_L19P_7	G5
7	IO_L19N_7	G6
7	IO_L06P_7	F4
7	IO_L06N_7	F5
7	IO_L04P_7	E1
7	IO_L04N_7	E2
7	IO_L03P_7/VREF_7	D1
7	IO_L03N_7	C1
7	IO_L02P_7/VRN_7	E3
7	IO_L02N_7/VRP_7	E4
7	IO_L01P_7	D2
7	IO_L01N_7	D3
0	VCCO_0	K13
0	VCCO_0	K12
0	VCCO_0	K11
0	VCCO_0	J11
0	VCCO_0	J10
0	VCCO_0	G12
0	VCCO_0	D7
0	VCCO_0	C12
1	VCCO_1	K17
1	VCCO_1	K16
1	VCCO_1	K15
1	VCCO_1	J18
1	VCCO_1	J17

BG728/BGG728 Standard BGA Package Specifications (1.27mm pitch)



NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-BAR-1
4. NO SOLDER BALL AND LAND ON A1.

728-BALL MOLDED BGA (BG728/BGG728)

Figure 6: BG728/BGG728 Standard BGA Package Specifications

Table 11: FF896 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
NA	GND	T13		
NA	GND	T12		
NA	GND	R19		
NA	GND	R18		
NA	GND	R17		
NA	GND	R16		
NA	GND	R15		
NA	GND	R14		
NA	GND	R13		
NA	GND	R12		
NA	GND	P24		
NA	GND	P19		
NA	GND	P18		
NA	GND	P17		
NA	GND	P16		
NA	GND	P15		
NA	GND	P14		
NA	GND	P13		
NA	GND	P12		
NA	GND	P7		
NA	GND	N19		
NA	GND	N18		
NA	GND	N17		
NA	GND	N16		
NA	GND	N15		
NA	GND	N14		
NA	GND	N13		
NA	GND	N12		
NA	GND	M26		
NA	GND	M19		
NA	GND	M18		
NA	GND	M17		
NA	GND	M16		
NA	GND	M15		
NA	GND	M14		
NA	GND	M13		
NA	GND	M12		

FF896 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)

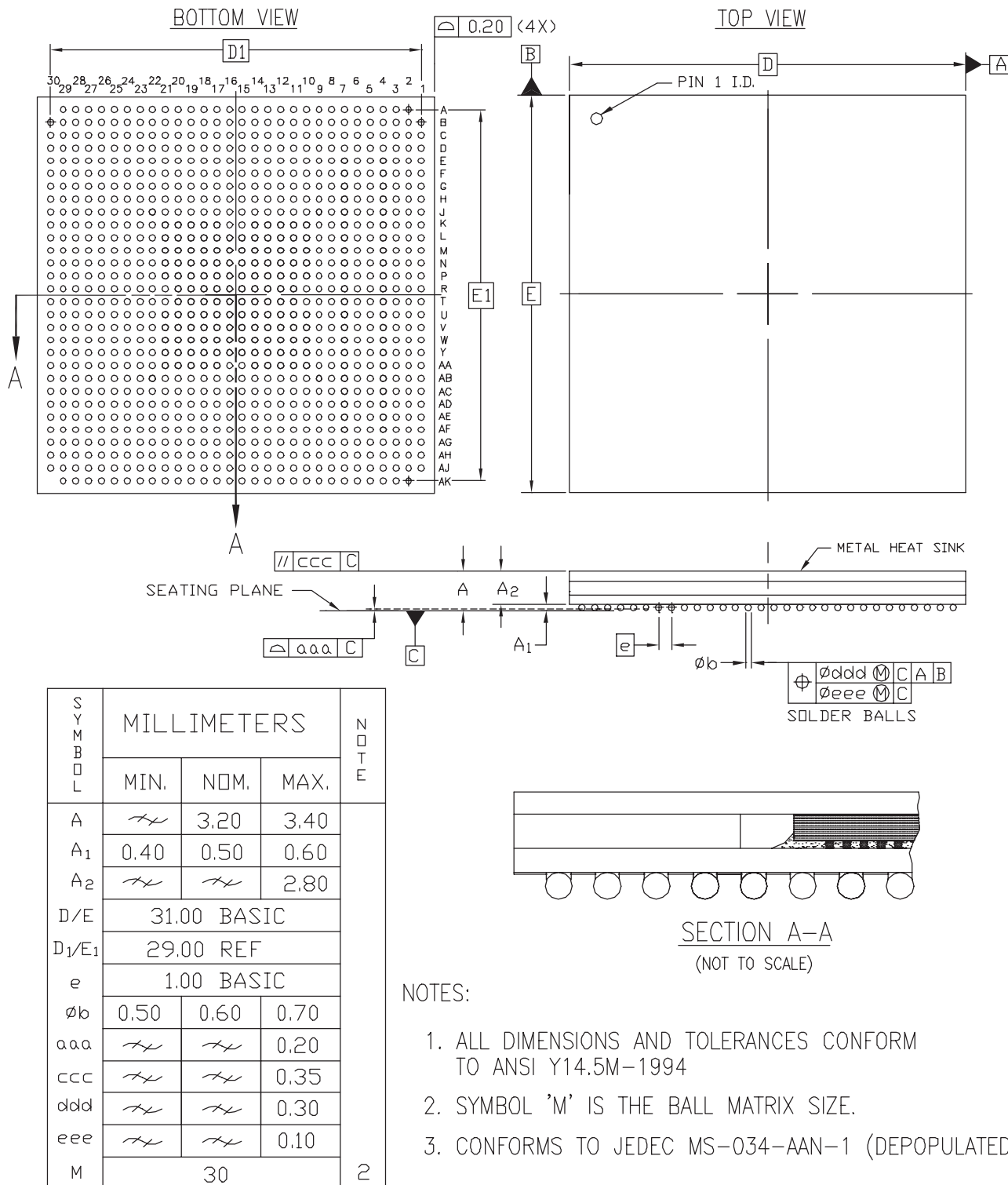


Figure 7: FF896 Flip-Chip Fine-Pitch BGA Package Specifications

FF1152 Flip-Chip Fine-Pitch BGA Package

As shown in Table 12, XC2V3000, XC2V4000, XC2V6000, and XC2V8000 Virtex-II devices are available in the FF1152 flip-chip fine-pitch BGA package. Pins in each of these devices are the same, except for the pin differences in the XC2V3000

Table 12: FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
4	IO_L20N_4	AJ10	
4	IO_L20P_4	AJ9	
4	IO_L21N_4	AH9	
4	IO_L21P_4/VREF_4	AH10	
4	IO_L22N_4	AN5	
4	IO_L22P_4	AN4	
4	IO_L23N_4	AE12	
4	IO_L23P_4	AE13	
4	IO_L24N_4	AM9	
4	IO_L24P_4	AL8	
4	IO_L25N_4	AP5	
4	IO_L25P_4	AP4	
4	IO_L26N_4	AG11	
4	IO_L26P_4	AG12	
4	IO_L27N_4	AN7	
4	IO_L27P_4/VREF_4	AN6	
4	IO_L28N_4	AL10	
4	IO_L28P_4	AL9	
4	IO_L29N_4	AF12	
4	IO_L29P_4	AF13	
4	IO_L30N_4	AK10	
4	IO_L30P_4	AK11	
4	IO_L49N_4	AP7	
4	IO_L49P_4	AP6	
4	IO_L50N_4	AH13	
4	IO_L50P_4	AH12	
4	IO_L51N_4	AJ11	
4	IO_L51P_4/VREF_4	AJ12	
4	IO_L52N_4	AP9	
4	IO_L52P_4	AN8	
4	IO_L53N_4	AG13	
4	IO_L53P_4	AG14	
4	IO_L54N_4	AM11	
4	IO_L54P_4	AL11	
4	IO_L60N_4	AN10	NC
4	IO_L60P_4	AN9	NC

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
0	IO_L22P_0	A34		
0	IO_L23N_0	K27		
0	IO_L23P_0	K26		
0	IO_L24N_0	F29		
0	IO_L24P_0	F30		
0	IO_L25N_0	B32		
0	IO_L25P_0	B33		
0	IO_L26N_0	L26		
0	IO_L26P_0	L25		
0	IO_L27N_0	G28		
0	IO_L27P_0/VREF_0	G29		
0	IO_L28N_0	C30		
0	IO_L28P_0	C31		
0	IO_L29N_0	J27		
0	IO_L29P_0	J26		
0	IO_L30N_0	D30		
0	IO_L30P_0	D31		
0	IO_L31N_0	A31	NC	
0	IO_L31P_0	A32	NC	
0	IO_L32N_0	H27	NC	
0	IO_L32P_0	H26	NC	
0	IO_L33N_0	F27	NC	
0	IO_L33P_0/VREF_0	F28	NC	
0	IO_L34N_0	B30	NC	
0	IO_L34P_0	B31	NC	
0	IO_L35N_0	M24	NC	
0	IO_L35P_0	M23	NC	
0	IO_L36N_0	D28	NC	
0	IO_L36P_0	D29	NC	
0	IO_L49N_0	C28		
0	IO_L49P_0	C29		
0	IO_L50N_0	K25		
0	IO_L50P_0	L24		
0	IO_L51N_0	E27		
0	IO_L51P_0/VREF_0	E28		
0	IO_L52N_0	A29		

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
1	IO_L93N_1	E19		
1	IO_L93P_1	E20		
1	IO_L92N_1	J19		
1	IO_L92P_1	J18		
1	IO_L91N_1	A18		
1	IO_L91P_1/VREF_1	A19		
1	IO_L84N_1	D18		
1	IO_L84P_1	D19		
1	IO_L83N_1	K19		
1	IO_L83P_1	K18		
1	IO_L82N_1	B18		
1	IO_L82P_1	B19		
1	IO_L81N_1/VREF_1	G18		
1	IO_L81P_1	G19		
1	IO_L80N_1	E18		
1	IO_L80P_1	E17		
1	IO_L79N_1	A16		
1	IO_L79P_1	A17		
1	IO_L78N_1	F17		
1	IO_L78P_1	F18		
1	IO_L77N_1	L19		
1	IO_L77P_1	L18		
1	IO_L76N_1	B16		
1	IO_L76P_1	B17		
1	IO_L75N_1/VREF_1	G16		
1	IO_L75P_1	G17		
1	IO_L74N_1	M19		
1	IO_L74P_1	M18		
1	IO_L73N_1	C16		
1	IO_L73P_1	C17		
1	IO_L72N_1	D15		
1	IO_L72P_1	D16		
1	IO_L71N_1	J17		
1	IO_L71P_1	J16		
1	IO_L70N_1	A14		
1	IO_L70P_1	A15		

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
4	IO_L32P_4	AM14	NC	
4	IO_L33N_4	AT10	NC	
4	IO_L33P_4/VREF_4	AT9	NC	
4	IO_L34N_4	AV10	NC	
4	IO_L34P_4	AV9	NC	
4	IO_L35N_4	AH16	NC	
4	IO_L35P_4	AH17	NC	
4	IO_L36N_4	AP13	NC	
4	IO_L36P_4	AP12	NC	
4	IO_L49N_4	AU12		
4	IO_L49P_4	AU11		
4	IO_L50N_4	AK15		
4	IO_L50P_4	AJ16		
4	IO_L51N_4	AT12		
4	IO_L51P_4/VREF_4	AT11		
4	IO_L52N_4	AN15		
4	IO_L52P_4	AN14		
4	IO_L53N_4	AR12		
4	IO_L53P_4	AR13		
4	IO_L54N_4	AT14		
4	IO_L54P_4	AT13		
4	IO_L55N_4	AW11		
4	IO_L55P_4	AW10		
4	IO_L56N_4	AM15		
4	IO_L56P_4	AM16		
4	IO_L57N_4	AP15		
4	IO_L57P_4/VREF_4	AP14		
4	IO_L58N_4	AV13		
4	IO_L58P_4	AV12		
4	IO_L59N_4	AK16		
4	IO_L59P_4	AK17		
4	IO_L60N_4	AR16		
4	IO_L60P_4	AR15		
4	IO_L67N_4	AW13		
4	IO_L67P_4	AW12		
4	IO_L68N_4	AL16		

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	GND	AR26		
NA	GND	AR14		
NA	GND	AR5		
NA	GND	AP34		
NA	GND	AP6		
NA	GND	AN33		
NA	GND	AN20		
NA	GND	AN7		
NA	GND	AM32		
NA	GND	AM23		
NA	GND	AM17		
NA	GND	AM8		
NA	GND	AL31		
NA	GND	AL9		
NA	GND	AK30		
NA	GND	AK20		
NA	GND	AK10		
NA	GND	AJ38		
NA	GND	AJ29		
NA	GND	AJ11		
NA	GND	AJ2		
NA	GND	AF35		
NA	GND	AF5		
NA	GND	AD23		
NA	GND	AD22		
NA	GND	AD21		
NA	GND	AD20		
NA	GND	AD19		
NA	GND	AD18		
NA	GND	AD17		
NA	GND	AC36		
NA	GND	AC32		
NA	GND	AC24		
NA	GND	AC23		
NA	GND	AC22		
NA	GND	AC21		

Table 14: BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000

Bank	Pin Description	Pin Number	No Connect in XC2V2000
2	IO_L23N_2	E2	
2	IO_L23P_2	F2	
2	IO_L24N_2	H4	
2	IO_L24P_2	J4	
2	IO_L25N_2	K8	NC
2	IO_L25P_2	L8	NC
2	IO_L27N_2	J7	NC
2	IO_L27P_2/VREF_2	K7	NC
2	IO_L43N_2	F1	
2	IO_L43P_2	G1	
2	IO_L44N_2	L9	
2	IO_L44P_2	M9	
2	IO_L45N_2	G2	
2	IO_L45P_2/VREF_2	J2	
2	IO_L46N_2	H3	
2	IO_L46P_2	J3	
2	IO_L47N_2	J6	
2	IO_L47P_2	L6	
2	IO_L48N_2	J5	
2	IO_L48P_2	K5	
2	IO_L49N_2	H1	
2	IO_L49P_2	J1	
2	IO_L50N_2	N10	
2	IO_L50P_2	P10	
2	IO_L51N_2	L7	
2	IO_L51P_2/VREF_2	M7	
2	IO_L52N_2	K3	
2	IO_L52P_2	L3	
2	IO_L53N_2	M8	
2	IO_L53P_2	N8	
2	IO_L54N_2	L5	
2	IO_L54P_2	M5	
2	IO_L67N_2	K2	
2	IO_L67P_2	L2	
2	IO_L68N_2	M6	
2	IO_L68P_2	N6	
2	IO_L69N_2	L4	
2	IO_L69P_2/VREF_2	M4	