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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	384
Number of Logic Elements/Cells	-
Total RAM Bits	442368
Number of I/O	200
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v250-5fgg456i

Table 4: LVTTTL and LVC MOS Programmable Currents (Sink and Source)

SelectI/O-Ultra	Programmable Current (Worst-Case Guaranteed Minimum)						
LVTTTL	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA
LVC MOS33	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA
LVC MOS25	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA
LVC MOS18	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	n/a
LVC MOS15	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	n/a

Figure 6 shows the SSTL2, SSTL3, and HSTL configurations. HSTL can sink current up to 48 mA. (HSTL IV)

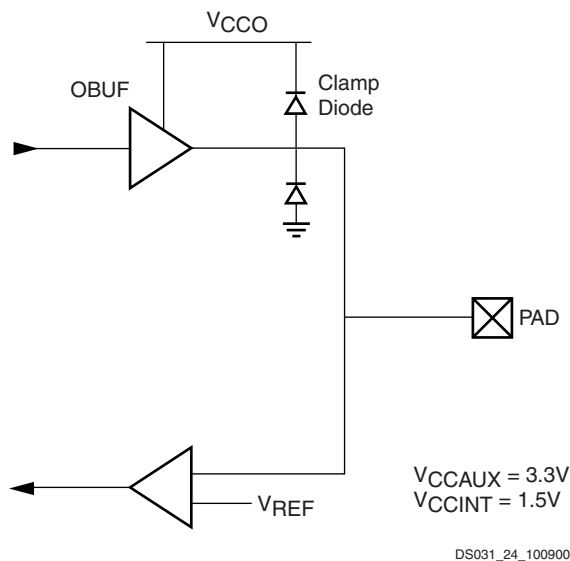


Figure 6: SSTL or HSTL SelectI/O-Ultra Standards

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. Virtex-II uses two memory cells to control the configuration of an I/O as an input. This is to reduce the probability of an I/O configured as an input from flipping to an output when subjected to a single event upset (SEU) in space applications.

Prior to configuration, all outputs not involved in configuration are forced into their high-impedance state. The pull-down resistors and the weak-keeper circuits are inactive. The dedicated pin HSWAP_EN controls the pull-up resistors prior to configuration. By default, HSWAP_EN is set high, which disables the pull-up resistors on user I/O pins. When HSWAP_EN is set low, the pull-up resistors are activated on user I/O pins.

All Virtex-II IOBs support IEEE 1149.1 compatible Boundary-Scan testing.

Input Path

The Virtex-II IOB input path routes input signals directly to internal logic and / or through an optional input flip-flop or latch, or through the DDR input registers. An optional delay element at the D-input of the storage element eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the Virtex-II device, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signaling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, V_{REF} . The need to supply V_{REF} imposes constraints on which standards can be used in the same bank. See I/O banking description.

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output and / or the 3-state signal can be routed to the buffer directly from the internal logic or through an output / 3-state flip-flop or latch, or through the DDR output / 3-state registers.

Each output driver can be individually programmed for a wide range of low-voltage signaling standards. In most signaling standards, the output High voltage depends on an externally supplied V_{CCO} voltage. The need to supply V_{CCO} imposes constraints on which standards can be used in the same bank. See I/O banking description.

I/O Banking

Some of the I/O standards described above require V_{CCO} and V_{REF} voltages. These voltages are externally supplied and connected to device pins that serve groups of IOB blocks, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from dividing each edge of the FPGA into two banks, as shown in Figure 7 and Figure 8. Each bank has multiple V_{CCO} pins, all of which must be connected to the same voltage. This voltage is determined by the output standards in use.

The Virtex-II implementation process is comprised of Synthesis, translation, mapping, place and route, and configuration file generation. While the tools can be run individually, many designers choose to run the entire implementation process with the click of a button. To assist those who prefer to script their design flows, Xilinx provides Xflow, an automated single command line process.

Design Verification

In addition to conventional design verification using static timing analysis or simulation techniques, Xilinx offers powerful in-circuit debugging techniques using ChipScope ILA (Integrated Logic Analysis). The reconfigurable nature of Xilinx FPGAs means that designs can be verified in real time without the need for extensive sets of software simulation vectors.

For simulation, the system extracts post-layout timing information from the design database, and back-annotates this information into the netlist for use by the simulator. The back annotation features a variety of patented Xilinx techniques, resulting in the industry's most powerful simulation flows. Alternatively, timing-critical portions of a design can be verified using the Xilinx static timing analyzer or a third party static timing analysis tool like Synopsys Prime Time™, by exporting timing data in the STAMP data format.

For in-circuit debugging, ChipScope ILA enables designers to analyze the real-time behavior of a device while operating at full system speeds. Logic analysis commands and captured data are transferred between the ChipScope software and ILA cores within the Virtex-II FPGA, using industry standard JTAG protocols. These JTAG transactions are driven over an optional download cable (MultiLINUX or JTAG), connecting the Virtex device in the target system to a PC or workstation.

ChipScope ILA was designed to look and feel like a logic analyzer, making it easy to begin debugging a design immediately. Modifications to the desired logic analysis can be downloaded directly into the system in a matter of minutes.

Other Unique Features of Virtex-II Design Flow

Xilinx design flows feature a number of unique capabilities. Among these are efficient incremental HDL design flows; a

robust capability that is enabled by Xilinx exclusive hierarchical floorplanning capabilities. Another powerful design capability only available in the Xilinx design flow is "Modular Design", part of the Xilinx suite of team design tools, which enables autonomous design, implementation, and verification of design modules.

Incremental Synthesis

Xilinx unique hierarchical floorplanning capabilities enable designers to create a programmable logic design by isolating design changes within one hierarchical "logic block", and perform synthesis, verification and implementation processes on that specific logic block. By preserving the logic in unchanged portions of a design, Xilinx incremental design makes the high-density design process more efficient.

Xilinx hierarchical floorplanning capabilities can be specified using the high-level floorplanner or a preferred RTL floorplanner (see the Xilinx web site for a list of supported EDA partners). When used in conjunction with one of the EDA partners' floorplanners, higher performance results can be achieved, as many synthesis tools use this more predictable detailed physical implementation information to establish more aggressive and accurate timing estimates when performing their logic optimizations.

Modular Design

Xilinx innovative modular design capabilities take the incremental design process one step further by enabling the designer to delegate responsibility for completing the design, synthesis, verification, and implementation of a hierarchical "logic block" to an arbitrary number of designers - assigning a specific region within the target FPGA for exclusive use by each of the team members.

This team design capability enables an autonomous approach to design modules, changing the hand-off point to the lead designer or integrator from "my module works in simulation" to "my module works in the FPGA". This unique design methodology also leverages the Xilinx hierarchical floorplanning capabilities and enables the Xilinx (or EDA partner) floorplanner to manage the efficient implementation of very high-density FPGAs.

Table 4: Quiescent Supply Current

Symbol	Description	Device	Min	Typical	Max	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC2V40		3	125	mA
		XC2V80		5	125	
		XC2V250		8	150	
		XC2V500		10	200	
		XC2V1000		12	250	
		XC2V1500		15	350	
		XC2V2000		20	400	
		XC2V3000		27	500	
		XC2V4000		35	650	
		XC2V6000		45	800	
		XC2V8000		60	1100	
I_{CCOQ}	Quiescent V_{CCO} supply current ^(1,2)	XC2V40		1	2	mA
		XC2V80		1	2	
		XC2V250		1	2	
		XC2V500		1	2	
		XC2V1000		1	2	
		XC2V1500		2	4	
		XC2V2000		2	4	
		XC2V3000		2	4	
		XC2V4000		2	4	
		XC2V6000		2	4	
		XC2V8000		2	4	
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current ^(1,2)	XC2V40		5	25	mA
		XC2V80		5	25	
		XC2V250		5	25	
		XC2V500		5	25	
		XC2V1000		5	25	
		XC2V1500		7.5	50	
		XC2V2000		7.5	50	
		XC2V3000		10	75	
		XC2V4000		10	75	
		XC2V6000		12.5	100	
		XC2V8000		12.5	100	

Notes:

1. With no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
2. If DCI or differential signaling is used, more accurate values can be obtained by using the Power Estimator or XPOWER™.
3. Data are retained even if V_{CCO} drops to 0 V.
4. Values specified for quiescent supply current parameters are Commercial Grade. For Industrial Grade values, multiply Commercial Grade values by 1.25.

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device operation. The actual current consumed depends on the power-on ramp rate of the power supply.

The V_{CCINT} , V_{CCAUX} , and V_{CCO} power supplies shall each ramp on, monotonically, no faster than 200 μ s and no slower than 50 ms. Ramp on is defined as: 0 V_{DC} to minimum supply voltages.

Table 5 shows the minimum current required by Virtex-II devices for proper power on and configuration.

Power supplies can be turned on in any sequence.⁽¹⁾

If any V_{CCO} bank powers up before V_{CCAUX} , then each bank draws up to 300 mA, worst case, until the V_{CCAUX} powers up.⁽²⁾ This does not harm the device. If the current is limited to the minimum value above, or larger, the device powers on properly after all three supplies have passed through their power-on reset threshold voltages.

Once initialized and configured, use the power calculator to estimate current drain on these supplies.

Notes:

1. If the V_{CCINT} ramp rate is longer than 10 ms, then V_{CCINT} must be applied before V_{CCO} and V_{CCAUX} . The device will not be damaged if this requirement is violated, but configuration will probably fail.
2. The 300 mA is transient current (peak); it eventually disappears even if V_{CCAUX} does not power up.

Table 6: DC Input and Output Levels (Continued)

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
SSTL3 I	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	$V_{CCO} + 0.5$	$V_{REF} - 0.6$	$V_{REF} + 0.6$	8	-8
SSTL3 II	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	$V_{CCO} + 0.5$	$V_{REF} - 0.8$	$V_{REF} + 0.8$	16	-16
SSTL2 I	-0.5	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$V_{CCO} + 0.5$	$V_{REF} - 0.65$	$V_{REF} + 0.65$	7.6	-7.6
SSTL2 II	-0.5	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$V_{CCO} + 0.5$	$V_{REF} - 0.80$	$V_{REF} + 0.80$	15.2	-15.2
AGP	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	$V_{CCO} + 0.5$	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2

Notes:

1. V_{OL} and V_{OH} for lower drive currents are sample tested. The DONE pin is always LVTTTL 12 mA.
2. Tested according to the relevant specifications.
3. LVTTTL and LVCMOS inputs have approximately 100 mV of hysteresis.

LDT Differential Signal DC Specifications (LDT_25)

Table 7: LDT DC Specifications

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Differential Output Voltage	V_{OD}	$R_T = 100 \Omega$ across Q and $\bar{Q}$ signals	500	600	700	mV
Change in V_{OD} Magnitude	ΔV_{OD}		-15		15	mV
Output Common Mode Voltage	V_{OCM}	$R_T = 100 \Omega$ across Q and $\bar{Q}$ signals	560	600	640	mV
Change in V_{OS} Magnitude	ΔV_{OCM}		-15		15	mV
Input Differential Voltage	V_{ID}		200	600	1000	mV
Change in V_{ID} Magnitude	ΔV_{ID}		-15		15	mV
Input Common Mode Voltage	V_{ICM}		500	600	700	mV
Change in V_{ICM} Magnitude	ΔV_{ICM}		-15		15	mV

LVDS DC Specifications (LVDS_33 & LVDS_25)

Table 8: LVDS DC Specifications

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}			3.3 or 2.5		V
Output High Voltage for Q and $\bar{Q}$	V_{OH}	$R_T = 100 \Omega$ across Q and $\bar{Q}$ signals			1.575	V
Output Low Voltage for Q and $\bar{Q}$	V_{OL}	$R_T = 100 \Omega$ across Q and $\bar{Q}$ signals	0.925			V
Differential Output Voltage (Q - $\bar{Q}$), Q = High ($\bar{Q}$ - Q), $\bar{Q}$ = High	V_{ODIFF}	$R_T = 100 \Omega$ across Q and $\bar{Q}$ signals	250	350	400	mV
Output Common-Mode Voltage	V_{OCM}	$R_T = 100 \Omega$ across Q and $\bar{Q}$ signals	1.125	1.2	1.375	V
Differential Input Voltage (Q - $\bar{Q}$), Q = High ($\bar{Q}$ - Q), $\bar{Q}$ = High	V_{IDIFF}	Common-mode input voltage = 1.25 V	100	350	N/A	mV
Input Common-Mode Voltage	V_{ICM}	Differential input voltage = ± 350 mV	0.2	1.25	$V_{CCO} - 0.5$	V

Table 15: IOB Input Switching Characteristics Standard Adjustments (Continued)

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-6	-5	-4	
LVDCI, 3.3V, Half-Impedance	LVDCI_DV2_33	T _{ILVDCI_DV2_33}	0.00	0.00	0.00	ns
LVDCI, 2.5V, Half-Impedance	LVDCI_DV2_25	T _{ILVDCI_DV2_25}	0.11	0.11	0.12	ns
LVDCI, 1.8V, Half-Impedance	LVDCI_DV2_18	T _{ILVDCI_DV2_18}	0.42	0.43	0.49	ns
LVDCI, 1.5V, Half-Impedance	LVDCI_DV2_15	T _{ILVDCI_DV2_15}	0.98	1.00	1.14	ns
HSLVDCI (High-Speed Low-Voltage DCI), 1.5V	HSLVDCI_15	T _{IHSLVDCI_15}	0.42	0.42	0.48	ns
HSLVDCI, 1.8V	HSLVDCI_18	T _{IHSLVDCI_18}	0.52	0.53	0.60	ns
HSLVDCI, 2.5V	HSLVDCI_25	T _{IHSLVDCI_25}	0.42	0.42	0.48	ns
HSLVDCI, 3.3V	HSLVDCI_33	T _{IHSLVDCI_33}	0.42	0.42	0.48	ns
GTL (Gunning Transceiver Logic) with DCI	GTL_DCI	T _{IGTL_DCI}	0.42	0.42	0.48	ns
GTL Plus with DCI	GTLP_DCI	T _{IGTLP_DCI}	0.42	0.42	0.48	ns
HSTL (High-Speed Transceiver Logic), Class I, with DCI	HSTL_I_DCI	T _{IHSTL_I_DCI}	0.42	0.42	0.48	ns
HSTL, Class II, with DCI	HSTL_II_DCI	T _{IHSTL_II_DCI}	0.42	0.42	0.48	ns
HSTL, Class III, with DCI	HSTL_III_DCI	T _{IHSTL_III_DCI}	0.42	0.42	0.48	ns
HSTL, Class IV, with DCI	HSTL_IV_DCI	T _{IHSTL_IV_DCI}	0.42	0.42	0.48	ns
HSTL, Class I, 1.8V, with DCI	HSTL_I_DCI_18	T _{IHSTL_I_DCI_18}	0.42	0.42	0.48	ns
HSTL, Class II, 1.8V, with DCI	HSTL_II_DCI_18	T _{IHSTL_II_DCI_18}	0.42	0.42	0.48	ns
HSTL, Class III, 1.8V, with DCI	HSTL_III_DCI_18	T _{IHSTL_III_DCI_18}	0.42	0.42	0.48	ns
HSTL, Class IV, 1.8V, with DCI	HSTL_IV_DCI_18	T _{IHSTL_IV_DCI_18}	0.42	0.42	0.48	ns
SSTL (Stub Series Terminated Logic), Class I, 1.8V, with DCI	SSTL18_I_DCI	T _{ISSTL18_I_DCI}	0.42	0.42	0.48	ns
SSTL, Class II, 1.8V, with DCI	SSTL18_II_DCI	T _{ISSTL18_II_DCI}	0.42	0.42	0.48	ns
SSTL, Class I, 2.5V, with DCI	SSTL2_I_DCI	T _{ISSTL2_I_DCI}	0.42	0.42	0.48	ns
SSTL, Class II, 2.5V, with DCI	SSTL2_II_DCI	T _{ISSTL2_II_DCI}	0.42	0.42	0.48	ns
SSTL, Class I, 3.3V, with DCI	SSTL3_I_DCI	T _{ISSTL3_I_DCI}	0.35	0.35	0.40	ns
SSTL, Class II, 3.3V, with DCI	SSTL3_II_DCI	T _{ISSTL3_II_DCI}	0.35	0.35	0.40	ns
LVDS (Low-Voltage Differential Signaling), 2.5V, with DCI	LVDS_25_DCI	T _{ILVDS_25_DCI}	0.60	0.60	0.69	ns
LVDS, 3.3V, with DCI	LVDS_33_DCI	T _{ILVDS_33_DCI}	0.60	0.60	0.69	ns
LVDSEXT (LVDS Extended Mode), 2.5V, with DCI	LVDSEXT_25_DCI	T _{ILVDSEXT_25_DCI}	0.58	0.59	0.79	ns
LVDSEXT, 3.3V, with DCI	LVDSEXT_33_DCI	T _{ILVDSEXT_33_DCI}	0.56	0.56	0.65	ns

Notes:

1. Input timing for LVTTTL is measured at 1.4V. For other I/O standards, see [Table 18](#).

Multiplier Switching Characteristics

Table 24: Multiplier Switching Characteristics

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Propagation Delay to Output Pin					
Input to Pin 35	T_{MULT_P35}	4.66	8.50	10.36	ns, Max
Input to Pin 34	T_{MULT_P34}	4.57	8.33	10.15	ns, Max
Input to Pin 33	T_{MULT_P33}	4.47	8.16	9.95	ns, Max
Input to Pin 32	T_{MULT_P32}	4.37	7.99	9.74	ns, Max
Input to Pin 31	T_{MULT_P31}	4.28	7.82	9.53	ns, Max
Input to Pin 30	T_{MULT_P30}	4.18	7.65	9.33	ns, Max
Input to Pin 29	T_{MULT_P29}	4.08	7.48	9.12	ns, Max
Input to Pin 28	T_{MULT_P28}	3.99	7.31	8.91	ns, Max
Input to Pin 27	T_{MULT_P27}	3.89	7.14	8.70	ns, Max
Input to Pin 26	T_{MULT_P26}	3.79	6.97	8.50	ns, Max
Input to Pin 25	T_{MULT_P25}	3.69	6.80	8.29	ns, Max
Input to Pin 24	T_{MULT_P24}	3.60	6.63	8.08	ns, Max
Input to Pin 23	T_{MULT_P23}	3.50	6.46	7.88	ns, Max
Input to Pin 22	T_{MULT_P22}	3.40	6.29	7.67	ns, Max
Input to Pin 21	T_{MULT_P21}	3.31	6.12	7.46	ns, Max
Input to Pin 20	T_{MULT_P20}	3.21	5.95	7.26	ns, Max
Input to Pin 19	T_{MULT_P19}	3.11	5.78	7.05	ns, Max
Input to Pin 18	T_{MULT_P18}	3.02	5.61	6.84	ns, Max
Input to Pin 17	T_{MULT_P17}	2.92	5.44	6.63	ns, Max
Input to Pin 16	T_{MULT_P16}	2.82	5.27	6.43	ns, Max
Input to Pin 15	T_{MULT_P15}	2.72	5.10	6.22	ns, Max
Input to Pin 14	T_{MULT_P14}	2.63	4.93	6.01	ns, Max
Input to Pin 13	T_{MULT_P13}	2.53	4.76	5.81	ns, Max
Input to Pin 12	T_{MULT_P12}	2.43	4.59	5.60	ns, Max
Input to Pin 11	T_{MULT_P11}	2.34	4.42	5.39	ns, Max
Input to Pin 10	T_{MULT_P10}	2.24	4.25	5.19	ns, Max
Input to Pin 9	T_{MULT_P9}	2.14	4.08	4.98	ns, Max
Input to Pin 8	T_{MULT_P8}	2.05	3.91	4.77	ns, Max
Input to Pin 7	T_{MULT_P7}	1.95	3.74	4.56	ns, Max
Input to Pin 6	T_{MULT_P6}	1.85	3.57	4.36	ns, Max
Input to Pin 5	T_{MULT_P5}	1.75	3.40	4.15	ns, Max
Input to Pin 4	T_{MULT_P4}	1.66	3.23	3.94	ns, Max
Input to Pin 3	T_{MULT_P3}	1.56	3.06	3.74	ns, Max
Input to Pin 2	T_{MULT_P2}	1.46	2.89	3.53	ns, Max
Input to Pin 1	T_{MULT_P1}	1.37	2.72	3.32	ns, Max
Input to Pin 0	T_{MULT_P0}	1.27	2.55	3.12	ns, Max

Configuration Timing

Configuration Memory Clearing Parameters

Power-up timing of configuration signals is shown in Figure 2; corresponding timing characteristics are listed in Table 30.

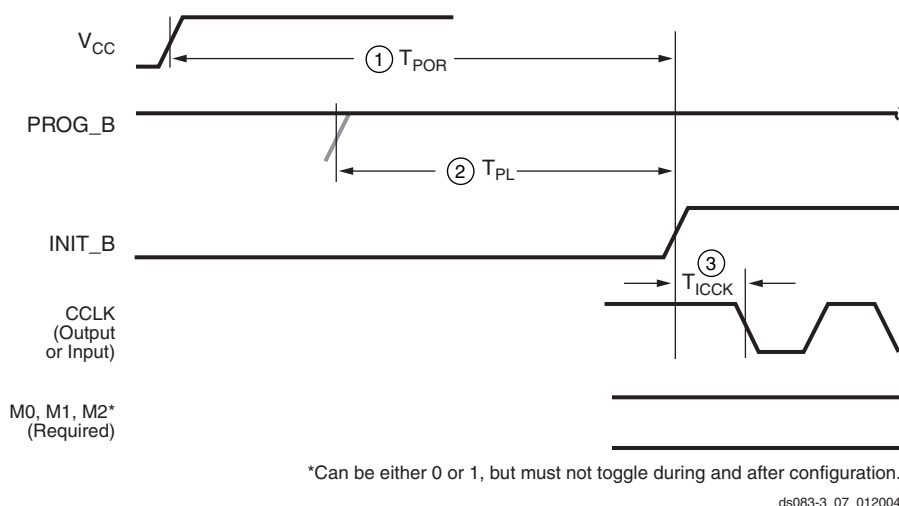


Figure 2: Configuration Power-Up Timing

Table 30: Power-Up Timing Characteristics

Description	Figure References	Symbol	Value	Units
Power-on reset	1	T_{POR}	$T_{PL} + 2$	ms, max
Program latency	2	T_{PL}	4	μ s per frame, max
CCLK (output) delay	3	T_{ICCK}	0.5	μ s, min
			4.0	μ s, max
Program pulse width		$T_{PROGRAM}$	300	ns, min

Notes:

- The M2, M1, and M0 mode pins should be set at a constant DC voltage level, either through pull-up or pull-down resistors, or tied directly to ground or V_{CCAUX} . The mode pins should not be toggled during and after configuration.

Master/Slave Serial Mode Parameters

Clock timing for Slave Serial configuration programming is shown in Figure 3, with Master Serial clock timing shown in Figure 4. Programming parameters for both Slave and Master modes are given in Table 31.

DCM Timing Parameters

All devices are 100% functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values

across the recommended operating conditions. All output jitter and phase specifications are determined through statistical measurement at the package pins.

Operating Frequency Ranges

Table 38: Operating Frequency Ranges

Description	Symbol	Constraint s	Speed Grade			Unit s
			-6	-5	-4	
Output Clocks (Low Frequency Mode)						
CLK0, CLK90, CLK180, CLK270	CLKOUT_FREQ_1X_LF_Min		24.00	24.00	24.00	MHz
	CLKOUT_FREQ_1X_LF_Max		230.00	210.00	180.00	MHz
CLK2X, CLK2X180	CLKOUT_FREQ_2X_LF_Min		48.00	48.00	48.00	MHz
	CLKOUT_FREQ_2X_LF_Max		450.00	420.00	360.00	MHz
CLKDV	CLKOUT_FREQ_DV_LF_Min		1.50	1.50	1.50	MHz
	CLKOUT_FREQ_DV_LF_Max		150.00	140.00	120.00	MHz
CLKFX, CLKFX180	CLKOUT_FREQ_FX_LF_Min		24.00	24.00	24.00	MHz
	CLKOUT_FREQ_FX_LF_Max		260.00	240.00	210.00	MHz
Input Clocks (Low Frequency Mode)						
CLKIN (using DLL outputs) ^(1,3,4)	CLKIN_FREQ_DLL_LF_Min		24.00	24.00	24.00	MHz
	CLKIN_FREQ_DLL_LF_Max		230.00	210.00	180.00	MHz
CLKIN (using CLKFX outputs) ^(2,3,4)	CLKIN_FREQ_FX_LF_Min		1.00	1.00	1.00	MHz
	CLKIN_FREQ_FX_LF_Max		260.00	240.00	210.00	MHz
PSCLK	PSCLK_FREQ_LF_Min		0.01	0.01	0.01	MHz
	PSCLK_FREQ_LF_Max		450.00	420.00	360.00	MHz
Output Clocks (High Frequency Mode)						
CLK0, CLK180	CLKOUT_FREQ_1X_HF_Min		48.00	48.00	48.00	MHz
	CLKOUT_FREQ_1X_HF_Max		450.00	420.00	360.00	MHz
CLKDV	CLKOUT_FREQ_DV_HF_Min		3.00	3.00	3.00	MHz
	CLKOUT_FREQ_DV_HF_Max		300.00	280.00	240.00	MHz
CLKFX, CLKFX180	CLKOUT_FREQ_FX_HF_Min		210.00	210.00	210.00	MHz
	CLKOUT_FREQ_FX_HF_Max		350.00	320.00	270.00	MHz
Input Clocks (High Frequency Mode)						
CLKIN (using DLL outputs) ^(1,3,4)	CLKIN_FREQ_DLL_HF_Min		48.00	48.00	48.00	MHz
	CLKIN_FREQ_DLL_HF_Max		450.00	420.00	360.00	MHz
CLKIN (using CLKFX outputs) ^(2,3,4)	CLKIN_FRQ_FX_HF_Min		50.00	50.00	50.00	MHz
	CLKIN_FRQ_FX_HF_Max		350.00	320.00	270.00	MHz
PSCLK	PSCLK_FREQ_HF_Min		0.01	0.01	0.01	MHz
	PSCLK_FREQ_HF_Max		450.00	420.00	360.00	MHz

Notes:

1. "DLL outputs" is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. If both DLL and CLKFX outputs are used, follow the more restrictive specification.
3. If the CLKIN_DIVIDE_BY_2 attribute of the DCM is used, then double these values.
4. If the CLKIN_DIVIDE_BY_2 attribute of the DCM is used and CLKIN frequency > 400 MHz, CLKIN duty cycle must be within $\pm 5\%$ (45/55 to 55/45).

Table 4: Virtex-II Pin Definitions (Continued)

Pin Name	Direction	Description
PROG_B	Input	Active Low asynchronous reset to configuration logic. This pin has a permanent weak pull-up resistor.
DONE	Input/Output	DONE is a bidirectional signal with an optional internal pull-up resistor. As an output, this pin indicates completion of the configuration process. As an input, a Low level on DONE can be configured to delay the start-up sequence.
M2, M1, M0	Input	Configuration mode selection.
HSWAP_EN	Input	Enable I/O pull-ups during configuration.
TCK	Input	Boundary Scan Clock.
TDI	Input	Boundary Scan Data Input.
TDO	Output	Boundary Scan Data Output.
TMS	Input	Boundary Scan Mode Select.
PWRDWN_B	Input (unsupported)	Active Low power-down pin (unsupported). <i>Driving this pin Low can adversely affect device operation and configuration.</i> PWRDWN_B is internally pulled High, which is its default state. It does not require an external pull-up.
Other Pins		
DXN, DXP	N/A	Temperature-sensing diode pins (Anode: DXP, Cathode: DXN).
V _{BATT}	Input	Decryptor key memory backup supply. Connect V _{BATT} to V _{CCAUX} or GND if battery is not used.
RSVD	N/A	Reserved pin - do not connect.
V _{CCO}	Input	Power-supply pins for the output drivers (per bank).
V _{CCAUX}	Input	Power-supply pins for auxiliary circuits.
V _{CCINT}	Input	Power-supply pins for the internal core logic.
GND	Input	Ground.

Notes:

1. All dedicated pins (JTAG and configuration) are powered by V_{CCAUX} (independent of the bank V_{CCO} voltage).

Table 7: FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
0	IO_L93N_0	B10		
0	IO_L93P_0	A10		
0	IO_L94N_0/VREF_0	E11		
0	IO_L94P_0	F11		
0	IO_L95N_0/GCLK7P	D11		
0	IO_L95P_0/GCLK6S	C11		
0	IO_L96N_0/GCLK5P	B11		
0	IO_L96P_0/GCLK4S	A11		
1	IO_L96N_1/GCLK3P	F12		
1	IO_L96P_1/GCLK2S	F13		
1	IO_L95N_1/GCLK1P	E12		
1	IO_L95P_1/GCLK0S	D12		
1	IO_L94N_1	C12		
1	IO_L94P_1/VREF_1	B12		
1	IO_L93N_1	A13		
1	IO_L93P_1	B13		
1	IO_L92N_1	C13		
1	IO_L92P_1	D13		
1	IO_L91N_1	E13		
1	IO_L91P_1/VREF_1	E14		
1	IO_L54N_1	A14	NC	
1	IO_L54P_1	B14	NC	
1	IO_L52N_1	C14	NC	
1	IO_L52P_1	D14	NC	
1	IO_L51N_1/VREF_1	A15	NC	
1	IO_L51P_1	B15	NC	
1	IO_L49N_1	C15	NC	
1	IO_L49P_1	D15	NC	
1	IO_L24N_1	F14	NC	NC
1	IO_L24P_1	E15	NC	NC
1	IO_L22N_1	A16	NC	NC
1	IO_L22P_1	B16	NC	NC
1	IO_L21N_1/VREF_1	C16	NC	NC

Table 7: FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
2	IO_L45N_2	H19		
2	IO_L45P_2/VREF_2	H20		
2	IO_L46N_2	H21		
2	IO_L46P_2	H22		
2	IO_L48N_2	J17		
2	IO_L48P_2	J18		
2	IO_L49N_2	J19	NC	
2	IO_L49P_2	J20	NC	
2	IO_L51N_2	J21	NC	
2	IO_L51P_2/VREF_2	J22	NC	
2	IO_L52N_2	K17	NC	
2	IO_L52P_2	K18	NC	
2	IO_L54N_2	K19	NC	
2	IO_L54P_2	K20	NC	
2	IO_L91N_2	K21		
2	IO_L91P_2	K22		
2	IO_L93N_2	L17		
2	IO_L93P_2/VREF_2	L18		
2	IO_L94N_2	L19		
2	IO_L94P_2	L20		
2	IO_L96N_2	L21		
2	IO_L96P_2	L22		
3	IO_L96N_3	M21		
3	IO_L96P_3	M20		
3	IO_L94N_3	M19		
3	IO_L94P_3	M18		
3	IO_L93N_3/VREF_3	M17		
3	IO_L93P_3	N17		
3	IO_L91N_3	N22		
3	IO_L91P_3	N21		
3	IO_L54N_3	N20	NC	
3	IO_L54P_3	N19	NC	
3	IO_L52N_3	N18	NC	

Table 7: FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
NA	VCCINT	R16		
NA	VCCINT	R7		
NA	VCCINT	H16		
NA	VCCINT	H7		
NA	VCCINT	G16		
NA	VCCINT	G15		
NA	VCCINT	G8		
NA	VCCINT	G7		
NA	VCCINT	F17		
NA	VCCINT	F6		
NA	GND	AB22		
NA	GND	AB1		
NA	GND	AA21		
NA	GND	AA2		
NA	GND	Y20		
NA	GND	Y3		
NA	GND	W19		
NA	GND	W4		
NA	GND	P14		
NA	GND	P13		
NA	GND	P12		
NA	GND	P11		
NA	GND	P10		
NA	GND	P9		
NA	GND	N14		
NA	GND	N13		
NA	GND	N12		
NA	GND	N11		
NA	GND	N10		
NA	GND	N9		
NA	GND	M14		
NA	GND	M13		
NA	GND	M12		
NA	GND	M11		

Table 9: BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
7	IO_L46P_7	H2		
7	IO_L46N_7	G2		
7	IO_L45P_7/VREF_7	H3		
7	IO_L45N_7	H4		
7	IO_L43P_7	G3		
7	IO_L43N_7	G4		
7	IO_L24P_7	H5		
7	IO_L24N_7	H6		
7	IO_L22P_7	J6		
7	IO_L22N_7	J7		
7	IO_L21P_7/VREF_7	K7		
7	IO_L21N_7	K8		
7	IO_L19P_7	E1		
7	IO_L19N_7	E2		
7	IO_L06P_7	D2		
7	IO_L06N_7	D3		
7	IO_L04P_7	E3		
7	IO_L04N_7	E4		
7	IO_L03P_7/VREF_7	F4		
7	IO_L03N_7	F5		
7	IO_L02P_7/VRN_7	G5		
7	IO_L02N_7/VRP_7	G6		
7	IO_L01P_7	H7		
7	IO_L01N_7	J8		
0	VCCO_0	J12		
0	VCCO_0	J11		
0	VCCO_0	J10		
0	VCCO_0	F11		
0	VCCO_0	C6		
0	VCCO_0	B11		
1	VCCO_1	J15		
1	VCCO_1	J14		
1	VCCO_1	J13		
1	VCCO_1	F14		
1	VCCO_1	C19		

Table 12: FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
4	IO_L20N_4	AJ10	
4	IO_L20P_4	AJ9	
4	IO_L21N_4	AH9	
4	IO_L21P_4/VREF_4	AH10	
4	IO_L22N_4	AN5	
4	IO_L22P_4	AN4	
4	IO_L23N_4	AE12	
4	IO_L23P_4	AE13	
4	IO_L24N_4	AM9	
4	IO_L24P_4	AL8	
4	IO_L25N_4	AP5	
4	IO_L25P_4	AP4	
4	IO_L26N_4	AG11	
4	IO_L26P_4	AG12	
4	IO_L27N_4	AN7	
4	IO_L27P_4/VREF_4	AN6	
4	IO_L28N_4	AL10	
4	IO_L28P_4	AL9	
4	IO_L29N_4	AF12	
4	IO_L29P_4	AF13	
4	IO_L30N_4	AK10	
4	IO_L30P_4	AK11	
4	IO_L49N_4	AP7	
4	IO_L49P_4	AP6	
4	IO_L50N_4	AH13	
4	IO_L50P_4	AH12	
4	IO_L51N_4	AJ11	
4	IO_L51P_4/VREF_4	AJ12	
4	IO_L52N_4	AP9	
4	IO_L52P_4	AN8	
4	IO_L53N_4	AG13	
4	IO_L53P_4	AG14	
4	IO_L54N_4	AM11	
4	IO_L54P_4	AL11	
4	IO_L60N_4	AN10	NC
4	IO_L60P_4	AN9	NC

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
3	IO_L34N_3	AH6	NC	
3	IO_L34P_3	AJ6	NC	
3	IO_L33N_3/VREF_3	AJ8	NC	
3	IO_L33P_3	AH8	NC	
3	IO_L32N_3	AL1	NC	
3	IO_L32P_3	AM1	NC	
3	IO_L31N_3	AH7	NC	
3	IO_L31P_3	AJ7	NC	
3	IO_L30N_3	AH10		
3	IO_L30P_3	AG10		
3	IO_L29N_3	AK3		
3	IO_L29P_3	AL3		
3	IO_L28N_3	AK4		
3	IO_L28P_3	AL4		
3	IO_L27N_3/VREF_3	AJ9		
3	IO_L27P_3	AH9		
3	IO_L26N_3	AM2		
3	IO_L26P_3	AN2		
3	IO_L25N_3	AK5		
3	IO_L25P_3	AL5		
3	IO_L24N_3	AK9		
3	IO_L24P_3	AK8		
3	IO_L23N_3	AN1		
3	IO_L23P_3	AP1		
3	IO_L22N_3	AK6		
3	IO_L22P_3	AL6		
3	IO_L21N_3/VREF_3	AH12		
3	IO_L21P_3	AG12		
3	IO_L20N_3	AM3		
3	IO_L20P_3	AN3		
3	IO_L19N_3	AM4		
3	IO_L19P_3	AN4		
3	IO_L12N_3	AJ12	NC	
3	IO_L12P_3	AH11	NC	
3	IO_L11N_3	AP2	NC	
3	IO_L11P_3	AR2	NC	

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
4	IO_L68P_4	AL17		
4	IO_L69N_4	AT16		
4	IO_L69P_4/VREF_4	AT15		
4	IO_L70N_4	AU14		
4	IO_L70P_4	AU13		
4	IO_L71N_4	AH18		
4	IO_L71P_4	AH19		
4	IO_L72N_4	AN17		
4	IO_L72P_4	AN16		
4	IO_L73N_4	AW15		
4	IO_L73P_4	AW14		
4	IO_L74N_4	AJ18		
4	IO_L74P_4	AJ19		
4	IO_L75N_4	AP17		
4	IO_L75P_4/VREF_4	AP16		
4	IO_L76N_4	AV15		
4	IO_L76P_4	AU15		
4	IO_L77N_4	AK18		
4	IO_L77P_4	AK19		
4	IO_L78N_4	AR18		
4	IO_L78P_4	AR17		
4	IO_L79N_4	AU17		
4	IO_L79P_4	AU16		
4	IO_L80N_4	AL18		
4	IO_L80P_4	AL19		
4	IO_L81N_4	AN19		
4	IO_L81P_4/VREF_4	AN18		
4	IO_L82N_4	AV17		
4	IO_L82P_4	AV16		
4	IO_L83N_4	AM18		
4	IO_L83P_4	AM19		
4	IO_L84N_4	AP19		
4	IO_L84P_4	AP18		
4	IO_L85N_4	AW17	NC	NC
4	IO_L85P_4	AW16	NC	NC
4	IO_L91N_4/VREF_4	AV19		

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	GND	AC20		
NA	GND	AC19		
NA	GND	AC18		
NA	GND	AC17		
NA	GND	AC16		
NA	GND	AC8		
NA	GND	AC4		
NA	GND	AB24		
NA	GND	AB23		
NA	GND	AB22		
NA	GND	AB21		
NA	GND	AB20		
NA	GND	AB19		
NA	GND	AB18		
NA	GND	AB17		
NA	GND	AB16		
NA	GND	AA24		
NA	GND	AA23		
NA	GND	AA22		
NA	GND	AA21		
NA	GND	AA20		
NA	GND	AA19		
NA	GND	AA18		
NA	GND	AA17		
NA	GND	AA16		
NA	GND	Y39		
NA	GND	Y36		
NA	GND	Y33		
NA	GND	Y30		
NA	GND	Y24		
NA	GND	Y23		
NA	GND	Y22		
NA	GND	Y21		
NA	GND	Y20		
NA	GND	Y19		
NA	GND	Y18		

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	GND	U4		
NA	GND	T23		
NA	GND	T22		
NA	GND	T21		
NA	GND	T20		
NA	GND	T19		
NA	GND	T18		
NA	GND	T17		
NA	GND	P35		
NA	GND	P5		
NA	GND	L38		
NA	GND	L29		
NA	GND	L11		
NA	GND	L2		
NA	GND	K30		
NA	GND	K20		
NA	GND	K10		
NA	GND	J31		
NA	GND	J9		
NA	GND	H32		
NA	GND	H23		
NA	GND	H17		
NA	GND	H8		
NA	GND	G33		
NA	GND	G20		
NA	GND	G7		
NA	GND	F34		
NA	GND	F6		
NA	GND	E35		
NA	GND	E26		
NA	GND	E14		
NA	GND	E5		
NA	GND	D36		
NA	GND	D23		
NA	GND	D20		
NA	GND	D17		

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	GND	D4		
NA	GND	C39		
NA	GND	C38		
NA	GND	C37		
NA	GND	C3		
NA	GND	C2		
NA	GND	C1		
NA	GND	B39		
NA	GND	B38		
NA	GND	B37		
NA	GND	B29		
NA	GND	B11		
NA	GND	B3		
NA	GND	B2		
NA	GND	B1		
NA	GND	A38		
NA	GND	A37		
NA	GND	A20		
NA	GND	A3		
NA	GND	A2		

Notes:

1. See Table 4 for an explanation of the signals available on this pin.

Table 14: BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000

Bank	Pin Description	Pin Number	No Connect in XC2V2000
0	IO_L49N_0	C23	
0	IO_L49P_0	C22	
0	IO_L50N_0	E22	
0	IO_L50P_0	E21	
0	IO_L51N_0	F21	
0	IO_L51P_0/VREF_0	F20	
0	IO_L52N_0	A24	
0	IO_L52P_0	A23	
0	IO_L53N_0	E20	
0	IO_L53P_0	E19	
0	IO_L54N_0	B22	
0	IO_L54P_0	B21	
0	IO_L67N_0	D21	
0	IO_L67P_0	D20	
0	IO_L68N_0	J20	
0	IO_L68P_0	J19	
0	IO_L69N_0	F19	
0	IO_L69P_0/VREF_0	F18	
0	IO_L70N_0	A22	
0	IO_L70P_0	A21	
0	IO_L71N_0	H19	
0	IO_L71P_0	H17	
0	IO_L72N_0	C21	
0	IO_L72P_0	C20	
0	IO_L73N_0	B20	
0	IO_L73P_0	B19	
0	IO_L74N_0	G18	
0	IO_L74P_0	G17	
0	IO_L75N_0	E18	
0	IO_L75P_0/VREF_0	D17	
0	IO_L76N_0	A20	
0	IO_L76P_0	A19	
0	IO_L77N_0	D19	
0	IO_L77P_0	D18	
0	IO_L78N_0	C19	
0	IO_L78P_0	C17	
0	IO_L91N_0/VREF_0	K18	
0	IO_L91P_0	J18	