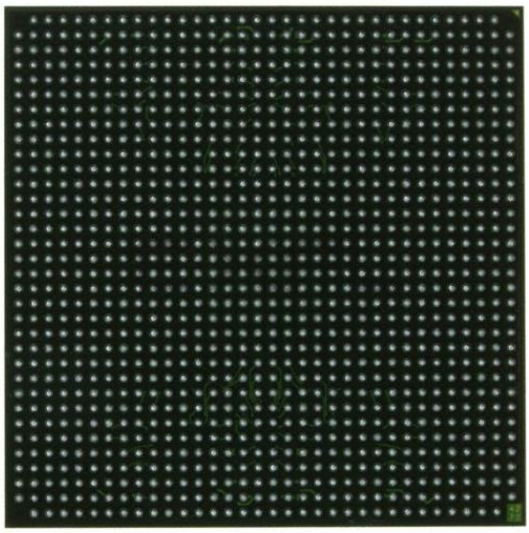

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Details	
Product Status	Obsolete
Number of LABs/CLBs	3584
Number of Logic Elements/Cells	-
Total RAM Bits	1769472
Number of I/O	720
Number of Gates	3000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v3000-4ffg1152c

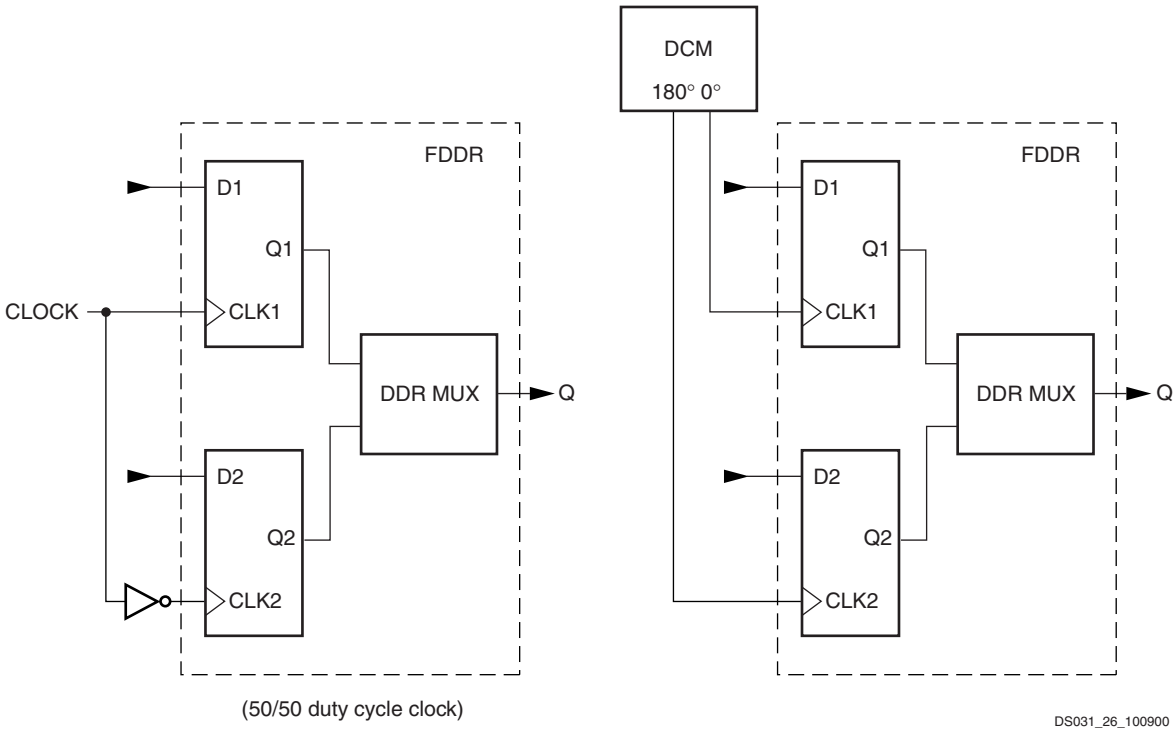


Figure 3: **Double Data Rate Registers**

The DDR mechanism shown in Figure 3 can be used to mirror a copy of the clock on the output. This is useful for propagating a clock along the data that has an identical delay. It is also useful for multiple clock generation, where there is a unique clock driver for every clock load. Virtex-II devices can produce many copies of a clock with very little skew.

Each group of two registers has a clock enable signal (ICE for the input registers, OCE for the output registers, and TCE for the 3-state registers). The clock enable signals are active High by default. If left unconnected, the clock enable for that storage element defaults to the active state.

Each IOB block has common synchronous or asynchronous set and reset (SR and REV signals).

SR forces the storage element into the state specified by the SRHIGH or SRLOW attribute. SRHIGH forces a logic “1”. SRLOW forces a logic “0”. When SR is used, a second input (REV) forces the storage element into the opposite state. The reset condition predominates over the set condition. The initial state after configuration or global initialization state is defined by a separate INIT0 and INIT1 attribute. By default, the SRLOW attribute forces INIT0, and the SRHIGH attribute forces INIT1.

For each storage element, the SRHIGH, SRLOW, INIT0, and INIT1 attributes are independent. Synchronous or asynchronous set / reset is consistent in an IOB block.

All the control signals have independent polarity. Any inverter placed on a control input is automatically absorbed.

Each register or latch (independent of all other registers or latches) (see Figure 4) can be configured as follows:

- No set or reset
- Synchronous set
- Synchronous reset
- Synchronous set and reset
- Asynchronous set (preset)
- Asynchronous reset (clear)
- Asynchronous set and reset (preset and clear)

The synchronous reset overrides a set, and an asynchronous clear overrides a preset.

Configuration

Virtex-II devices are configured by loading application specific configuration data into the internal configuration memory. Configuration is carried out using a subset of the device pins, some of which are dedicated, while others can be re-used as general purpose inputs and outputs once configuration is complete.

Depending on the system design, several configuration modes are supported, selectable via mode pins. The mode pins M2, M1 and M0 are dedicated pins. The M2, M1, and M0 mode pins should be set at a constant DC voltage level, either through pull-up or pull-down resistors, or tied directly to ground or V_{CCAUX}. The mode pins should not be toggled during and after configuration.

An additional pin, HSWAP_EN is used in conjunction with the mode pins to select whether user I/O pins have pull-ups during configuration. By default, HSWAP_EN is tied High (internal pull-up) which shuts off the pull-ups on the user I/O pins during configuration. When HSWAP_EN is tied Low, user I/Os have pull-ups during configuration. Other dedicated pins are CCLK (the configuration clock pin), DONE, PROG_B, and the Boundary-Scan pins: TDI, TDO, TMS, and TCK. Depending on the configuration mode chosen, CCLK can be an output generated by the FPGA, or an input accepting an externally generated clock. The configuration pins and Boundary-Scan pins are independent of the V_{CCO}. The auxiliary power supply (V_{CCAUX}) of 3.3V is used for these pins. All configuration pins are LVTTL 12 mA. (See Virtex-II DC Characteristics in Module 3.)

A persist option is available which can be used to force the configuration pins to retain their configuration function even after device configuration is complete. If the persist option is not selected then the configuration pins with the exception of CCLK, PROG_B, and DONE can be used as user I/O in normal operation. The persist option does not apply to the Boundary-Scan related pins. The persist feature is valuable in applications which employ partial reconfiguration or reconfiguration on the fly.

Configuration Modes

Virtex-II supports the following five configuration modes:

- Slave-Serial Mode
- Master-Serial Mode
- Slave SelectMAP Mode
- Master SelectMAP Mode
- Boundary-Scan (JTAG, IEEE 1532) Mode

A detailed description of configuration modes is provided in the Virtex-II *User Guide*.

Slave-Serial Mode

In slave-serial mode, the FPGA receives configuration data in bit-serial form from a serial PROM or other serial source of configuration data. The CCLK pin on the FPGA is an input in this mode. The serial bitstream must be setup at the DIN input pin a short time before each rising edge of the externally generated CCLK.

Multiple FPGAs can be daisy-chained for configuration from a single source. After a particular FPGA has been configured, the data for the next device is routed internally to the DOUT pin. The data on the DOUT pin changes on the falling edge of CCLK.

Slave-serial mode is selected by applying <111> to the mode pins (M2, M1, M0). A weak pull-up on the mode pins makes slave serial the default mode if the pins are left unconnected.

Master-Serial Mode

In master-serial mode, the CCLK pin is an output pin. It is the Virtex-II FPGA device that drives the configuration clock on the CCLK pin to a Xilinx Serial PROM which in turn feeds bit-serial data to the DIN input. The FPGA accepts this data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the falling CCLK edge.

The interface is identical to slave serial except that an internal oscillator is used to generate the configuration clock (CCLK). A wide range of frequencies can be selected for CCLK which always starts at a slow default frequency. Configuration bits then switch CCLK to a higher frequency for the remainder of the configuration.

Slave SelectMAP Mode

The SelectMAP mode is the fastest configuration option. Byte-wide data is written into the Virtex-II FPGA device with a BUSY flag controlling the flow of data. An external data source provides a byte stream, CCLK, an active Low Chip Select (CS_B) signal and a Write signal (RDWR_B). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low. Data can also be read using the SelectMAP mode. If RDWR_B is asserted, configuration data is read out of the FPGA as part of a readback operation.

After configuration, the pins of the SelectMAP port can be used as additional user I/O. Alternatively, the port can be retained to permit high-speed 8-bit readback using the persist option.

Multiple Virtex-II FPGAs can be configured using the SelectMAP mode, and be made to start-up simultaneously. To configure multiple devices in this way, wire the individual CCLK, Data, RDWR_B, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by deasserting the CS_B pin of each device in turn and writing the appropriate data.

Master SelectMAP Mode

This mode is a master version of the SelectMAP mode. The device is configured byte-wide on a CCLK supplied by the

IOB Output Switching Characteristics Standard Adjustments

Table 17 gives all standard-specific adjustments for output delays terminating at pads, based on standard capacitive load, C_{REF}. Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

Table 17: **IOB Output Switching Characteristics Standard Adjustments**

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-6	-5	-4	
LVTTL (Low-Voltage Transistor-Transistor Logic), Slow, 2 mA	LVTTL_S2	T_{OLVTTL_S2}	9.42	9.71	10.68	ns
LVTTL, Slow, 4 mA	LVTTL_S4	T_{OLVTTL_S4}	5.77	5.95	6.55	ns
LVTTL, Slow, 6 mA	LVTTL_S6	T_{OLVTTL_S6}	4.11	4.24	4.66	ns
LVTTL, Slow, 8 mA	LVTTL_S8	T_{OLVTTL_S8}	2.87	2.96	3.26	ns
LVTTL, Slow, 12 mA	LVTTL_S12	T_{OLVTTL_S12}	2.32	2.39	2.63	ns
LVTTL, Slow, 16 mA	LVTTL_S16	T_{OLVTTL_S16}	1.70	1.75	1.93	ns
LVTTL, Slow, 24 mA	LVTTL_S24	T_{OLVTTL_S24}	1.26	1.30	1.43	ns
LVTTL, Fast, 2 mA	LVTTL_F2	T_{OLVTTL_F2}	6.52	6.72	7.39	ns
LVTTL, Fast, 4 mA	LVTTL_F4	T_{OLVTTL_F4}	2.80	2.88	3.17	ns
LVTTL, Fast, 6 mA	LVTTL_F6	T_{OLVTTL_F6}	1.57	1.62	1.78	ns
LVTTL, Fast, 8 mA	LVTTL_F8	T_{OLVTTL_F8}	0.46	0.48	0.52	ns
LVTTL, Fast, 12 mA	LVTTL_F12	T_{OLVTTL_F12}	0.00	0.00	0.00	ns
LVTTL, Fast, 16 mA	LVTTL_F16	T_{OLVTTL_F16}	–0.13	–0.14	–0.15	ns
LVTTL, Fast, 24 mA	LVTTL_F24	T_{OLVTTL_F24}	–0.22	–0.23	–0.26	ns
LVCMOS (Low-Voltage CMOS), 3.3V, Slow, 2 mA	LVCMOS33_S2	$T_{OLVCMOS33\_S2}$	7.67	7.91	8.70	ns
LVCMOS, 3.3V, Slow, 4 mA	LVCMOS33_S4	$T_{OLVCMOS33\_S4}$	4.37	4.50	4.95	ns
LVCMOS, 3.3V, Slow, 6 mA	LVCMOS33_S6	$T_{OLVCMOS33\_S6}$	3.34	3.44	3.78	ns
LVCMOS, 3.3V, Slow, 8 mA	LVCMOS33_S8	$T_{OLVCMOS33\_S8}$	2.29	2.36	2.60	ns
LVCMOS, 3.3V, Slow, 12 mA	LVCMOS33_S12	$T_{OLVCMOS33\_S12}$	1.91	1.97	2.16	ns
LVCMOS, 3.3V, Slow, 16 mA	LVCMOS33_S16	$T_{OLVCMOS33\_S16}$	1.24	1.27	1.40	ns
LVCMOS, 3.3V, Slow, 24 mA	LVCMOS33_S24	$T_{OLVCMOS33\_S24}$	1.18	1.22	1.34	ns
LVCMOS, 3.3V, Fast, 2 mA	LVCMOS33_F2	$T_{OLVCMOS33\_F2}$	5.82	6.00	6.60	ns
LVCMOS, 3.3V, Fast, 4 mA	LVCMOS33_F4	$T_{OLVCMOS33\_F4}$	2.48	2.55	2.81	ns
LVCMOS, 3.3V, Fast, 6 mA	LVCMOS33_F6	$T_{OLVCMOS33\_F6}$	1.28	1.31	1.45	ns
LVCMOS, 3.3V, Fast, 8 mA	LVCMOS33_F8	$T_{OLVCMOS33\_F8}$	0.48	0.49	0.54	ns
LVCMOS, 3.3V, Fast, 12 mA	LVCMOS33_F12	$T_{OLVCMOS33\_F12}$	0.27	0.28	0.31	ns
LVCMOS, 3.3V, Fast, 16 mA	LVCMOS33_F16	$T_{OLVCMOS33\_F16}$	–0.14	–0.14	–0.15	ns
LVCMOS, 3.3V, Fast, 24 mA	LVCMOS33_F24	$T_{OLVCMOS33\_F24}$	–0.21	–0.21	–0.23	ns
LVCMOS, 2.5V, Slow, 2 mA	LVCMOS25_S2	$T_{OLVCMOS25\_S2}$	9.11	9.39	10.33	ns
LVCMOS, 2.5V, Slow, 4 mA	LVCMOS25_S4	$T_{OLVCMOS25\_S4}$	5.00	5.16	5.67	ns
LVCMOS, 2.5V, Slow, 6 mA	LVCMOS25_S6	$T_{OLVCMOS25\_S6}$	4.53	4.67	5.13	ns
LVCMOS, 2.5V, Slow, 8 mA	LVCMOS25_S8	$T_{OLVCMOS25\_S8}$	3.86	3.98	4.38	ns
LVCMOS, 2.5V, Slow, 12 mA	LVCMOS25_S12	$T_{OLVCMOS25\_S12}$	2.84	2.93	3.22	ns
LVCMOS, 2.5V, Slow, 16 mA	LVCMOS25_S16	$T_{OLVCMOS25\_S16}$	2.36	2.43	2.67	ns
LVCMOS, 2.5V, Slow, 24 mA	LVCMOS25_S24	$T_{OLVCMOS25\_S24}$	2.00	2.06	2.27	ns
LVCMOS, 2.5V, Fast, 2 mA	LVCMOS25_F2	$T_{OLVCMOS25\_F2}$	4.06	4.18	4.60	ns
LVCMOS, 2.5V, Fast, 4 mA	LVCMOS25_F4	$T_{OLVCMOS25\_F4}$	1.15	1.18	1.30	ns
LVCMOS, 2.5V, Fast, 6 mA	LVCMOS25_F6	$T_{OLVCMOS25\_F6}$	0.72	0.74	0.81	ns
LVCMOS, 2.5V, Fast, 8 mA	LVCMOS25_F8	$T_{OLVCMOS25\_F8}$	0.33	0.34	0.37	ns
LVCMOS, 2.5V, Fast, 12 mA	LVCMOS25_F12	$T_{OLVCMOS25\_F12}$	0.02	0.02	0.03	ns

Table 17: **IOB Output Switching Characteristics Standard Adjustments *(Continued)***

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-6	-5	-4	
LVCMOS, 2.5V, Fast, 16 mA	LVCMOS25_F16	$T_{OLVCMOS25\_F16}$	–0.18	–0.19	–0.21	ns
LVCMOS, 2.5V, Fast, 24 mA	LVCMOS25_F24	$T_{OLVCMOS25\_F24}$	–0.35	–0.36	–0.40	ns
LVCMOS, 1.8V, Slow, 2 mA	LVCMOS18_S2	$T_{OLVCMOS18\_S2}$	15.62	16.10	17.71	ns
LVCMOS, 1.8V, Slow, 4 mA	LVCMOS18_S4	$T_{OLVCMOS18\_S4}$	10.20	10.51	11.57	ns
LVCMOS, 1.8V, Slow, 6 mA	LVCMOS18_S6	$T_{OLVCMOS18\_S6}$	7.52	7.75	8.53	ns
LVCMOS, 1.8V, Slow, 8 mA	LVCMOS18_S8	$T_{OLVCMOS18\_S8}$	6.87	7.08	7.78	ns
LVCMOS, 1.8V, Slow, 12 mA	LVCMOS18_S12	$T_{OLVCMOS18\_S12}$	5.54	5.71	6.28	ns
LVCMOS, 1.8V, Slow, 16 mA	LVCMOS18_S16	$T_{OLVCMOS18\_S16}$	5.31	5.47	6.02	ns
LVCMOS, 1.8V, Fast, 2 mA	LVCMOS18_F2	$T_{OLVCMOS18\_F2}$	5.55	5.72	6.30	ns
LVCMOS, 1.8V, Fast, 4 mA	LVCMOS18_F4	$T_{OLVCMOS18\_F4}$	1.89	1.95	2.15	ns
LVCMOS, 1.8V, Fast, 6 mA	LVCMOS18_F6	$T_{OLVCMOS18\_F6}$	0.83	0.85	0.94	ns
LVCMOS, 1.8V, Fast, 8 mA	LVCMOS18_F8	$T_{OLVCMOS18\_F8}$	0.70	0.72	0.80	ns
LVCMOS, 1.8V, Fast, 12 mA	LVCMOS18_F12	$T_{OLVCMOS18\_F12}$	0.26	0.27	0.30	ns
LVCMOS, 1.8V, Fast, 16 mA	LVCMOS18_F16	$T_{OLVCMOS18\_F16}$	0.23	0.23	0.26	ns
LVCMOS, 1.5V, Slow, 2 mA	LVCMOS15_S2	$T_{OLVCMOS15\_S2}$	18.96	19.55	21.50	ns
LVCMOS, 1.5V, Slow, 4 mA	LVCMOS15_S4	$T_{OLVCMOS15\_S4}$	12.77	13.17	14.48	ns
LVCMOS, 1.5V, Slow, 6 mA	LVCMOS15_S6	$T_{OLVCMOS15\_S6}$	12.05	12.42	13.66	ns
LVCMOS, 1.5V, Slow, 8 mA	LVCMOS15_S8	$T_{OLVCMOS15\_S8}$	9.75	10.06	11.06	ns
LVCMOS, 1.5V, Slow, 12 mA	LVCMOS15_S12	$T_{OLVCMOS15\_S12}$	9.04	9.32	10.25	ns
LVCMOS, 1.5V, Slow, 16 mA	LVCMOS15_S16	$T_{OLVCMOS15\_S16}$	8.21	8.46	9.31	ns
LVCMOS, 1.5V, Fast, 2 mA	LVCMOS15_F2	$T_{OLVCMOS15\_F2}$	5.09	5.25	5.78	ns
LVCMOS, 1.5V, Fast, 4 mA	LVCMOS15_F4	$T_{OLVCMOS15\_F4}$	2.01	2.07	2.27	ns
LVCMOS, 1.5V, Fast, 6 mA	LVCMOS15_F6	$T_{OLVCMOS15\_F6}$	1.46	1.51	1.66	ns
LVCMOS, 1.5V, Fast, 8 mA	LVCMOS15_F8	$T_{OLVCMOS15\_F8}$	0.93	0.96	1.05	ns
LVCMOS, 1.5V, Fast, 12 mA	LVCMOS15_F12	$T_{OLVCMOS15\_F12}$	0.74	0.77	0.84	ns
LVCMOS, 1.5V, Fast, 16 mA	LVCMOS15_F16	$T_{OLVCMOS15\_F16}$	0.67	0.69	0.75	ns
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	T_{OLVDS_25}	–0.31	–0.32	–0.36	ns
LVDS, 3.3V	LVDS_33	T_{OLVDS_33}	–0.25	–0.26	–0.29	ns
LVDSEXT (LVDS Extended Mode), 2.5V	LVDSEXT_25	$T_{OLVDSEXT\_25}$	–0.18	–0.19	–0.21	ns
LVDSEXT, 3.3V	LVDSEXT_33	$T_{OLVDSEXT\_33}$	–0.17	–0.18	–0.19	ns
ULVDS (Ultra LVDS), 2.5V	ULVDS_25	T_{OULVDS_25}	–0.20	–0.21	–0.23	ns
BLVDS (Bus LVDS), 2.5V	BLVDS_25	T_{OBLVDS_25}	0.67	0.69	0.76	ns
LDT (HyperTransport), 2.5V	LDT_25	T_{OLDT_25}	–0.20	–0.21	–0.23	ns
LVPECL (Low-Voltage Positive Electron-Coupled Logic), 3.3V	LVPECL_33	$T_{OLVPECL\_33}$	0.29	0.30	0.33	ns
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3	T_{OPCI33_3}	1.15	1.19	1.31	ns
PCI, 66 MHz, 3.3V	PCI66_3	T_{OPCI66_3}	–0.01	–0.01	–0.01	ns
PCI-X, 133 MHz, 3.3V	PCIX	T_{OPCIX}	–0.01	–0.01	–0.01	ns
GTL (Gunning Transceiver Logic)	GTL	T_{OGTL}	–0.31	–0.32	–0.36	ns
GTL Plus	GTLP	T_{OGTLP}	–0.17	–0.18	–0.20	ns
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	T_{OHSTL_I}	0.26	0.27	0.29	ns
HSTL, Class II	HSTL_II	T_{OHSTL_II}	–0.15	–0.16	–0.17	ns
HSTL, Class III	HSTL_III	T_{OHSTL_III}	–0.17	–0.17	–0.19	ns
HSTL, Class IV	HSTL_IV	T_{OHSTL_IV}	–0.40	–0.41	–0.45	ns
HSTL, Class I, 1.8V	HSTL_I_18	$T_{OHSTL\_I\_18}$	0.03	0.03	0.04	ns

Table 27: **Enhanced Pipelined Multiplier Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Setup and Hold Times Before/After Clock					
Data Inputs	$T_{MULIDCK}/T_{MULCKID}$	3.00/0.00	3.45/0.00	3.89/0.00	ns, Max
Clock Enable	$T_{MULIDCK\_CE}/T_{MULCKID\_CE}$	0.72/0.00	0.80/0.00	0.86/0.00	ns, Max
Reset	$T_{MULIDCK\_RST}/T_{MULCKID\_RST}$	0.72/0.00	0.80/0.00	0.86/0.00	ns, Max
Clock to Output Pin					
Clock to Pin 35	$T_{MULTCK1\_P35}$	3.05	3.25	3.74	ns, Max
Clock to Pin 34	$T_{MULTCK1\_P34}$	2.95	3.14	3.61	ns, Max
Clock to Pin 33	$T_{MULTCK1\_P33}$	2.85	3.04	3.49	ns, Max
Clock to Pin 32	$T_{MULTCK1\_P32}$	2.76	2.93	3.37	ns, Max
Clock to Pin 31	$T_{MULTCK1\_P31}$	2.66	2.82	3.25	ns, Max
Clock to Pin 30	$T_{MULTCK1\_P30}$	2.56	2.72	3.12	ns, Max
Clock to Pin 29	$T_{MULTCK1\_P29}$	2.47	2.61	3.00	ns, Max
Clock to Pin 28	$T_{MULTCK1\_P28}$	2.37	2.50	2.88	ns, Max
Clock to Pin 27	$T_{MULTCK1\_P27}$	2.27	2.40	2.75	ns, Max
Clock to Pin 26	$T_{MULTCK1\_P26}$	2.17	2.29	2.63	ns, Max
Clock to Pin 25	$T_{MULTCK1\_P25}$	2.08	2.18	2.51	ns, Max
Clock to Pin 24	$T_{MULTCK1\_P24}$	1.98	2.07	2.38	ns, Max
Clock to Pin 23	$T_{MULTCK1\_P23}$	1.88	1.97	2.26	ns, Max
Clock to Pin 22	$T_{MULTCK1\_P22}$	1.79	1.86	2.14	ns, Max
Clock to Pin 21	$T_{MULTCK1\_P21}$	1.69	1.75	2.02	ns, Max
Clock to Pin 20	$T_{MULTCK1\_P20}$	1.59	1.65	1.89	ns, Max
Clock to Pin 19	$T_{MULTCK1\_P19}$	1.50	1.54	1.77	ns, Max
Clock to Pin 18	$T_{MULTCK1\_P18}$	1.40	1.43	1.65	ns, Max
Clock to Pin 17	$T_{MULTCK1\_P17}$	1.30	1.33	1.52	ns, Max
Clock to Pin 16	$T_{MULTCK1\_P16}$	1.20	1.22	1.40	ns, Max
Clock to Pin 15	$T_{MULTCK1\_P15}$	1.11	1.11	1.28	ns, Max
Clock to Pin 14	$T_{MULTCK1\_P14}$	1.01	1.00	1.15	ns, Max
Clock to Pin 13	$T_{MULTCK1\_P13}$	0.91	1.00	1.15	ns, Max
Clock to Pin 12	$T_{MULTCK1\_P12}$	0.91	1.00	1.15	ns, Max
Clock to Pin 11	$T_{MULTCK1\_P11}$	0.91	1.00	1.15	ns, Max
Clock to Pin 10	$T_{MULTCK1\_P10}$	0.91	1.00	1.15	ns, Max
Clock to Pin 9	$T_{MULTCK1\_P9}$	0.91	1.00	1.15	ns, Max
Clock to Pin 8	$T_{MULTCK1\_P8}$	0.91	1.00	1.15	ns, Max
Clock to Pin 7	$T_{MULTCK1\_P7}$	0.91	1.00	1.15	ns, Max
Clock to Pin 6	$T_{MULTCK1\_P6}$	0.91	1.00	1.15	ns, Max
Clock to Pin 5	$T_{MULTCK1\_P5}$	0.91	1.00	1.15	ns, Max
Clock to Pin 4	$T_{MULTCK1\_P4}$	0.91	1.00	1.15	ns, Max
Clock to Pin 3	$T_{MULTCK1\_P3}$	0.91	1.00	1.15	ns, Max
Clock to Pin 2	$T_{MULTCK1\_P2}$	0.91	1.00	1.15	ns, Max
Clock to Pin 1	$T_{MULTCK1\_P1}$	0.91	1.00	1.15	ns, Max
Clock to Pin 0	$T_{MULTCK1\_P0}$	0.91	1.00	1.15	ns, Max

Configuration Timing

Configuration Memory Clearing Parameters

Power-up timing of configuration signals is shown in Figure 2; corresponding timing characteristics are listed in Table 30.

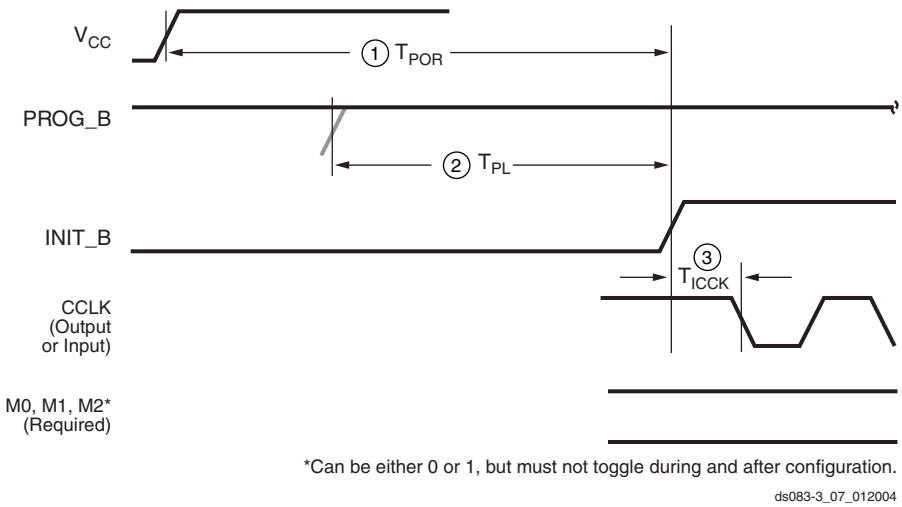


Figure 2: **Configuration Power-Up Timing**

Table 30: **Power-Up Timing Characteristics**

Description	Figure References	Symbol	Value	Units
Power-on reset	1	T_{POR}	T_{PL} + 2	ms, max
Program latency	2	T_{PL}	4	µs per frame, max
CCLK (output) delay	3	T_{ICCK}	0.5	µs, min
			4.0	µs, max
Program pulse width		$T_{PROGRAM}$	300	ns, min

Notes:
1. The M2, M1, and M0 mode pins should be set at a constant DC voltage level, either through pull-up or pull-down resistors, or tied directly to ground or V_{CCAUX}. The mode pins should not be toggled during and after configuration.

Master/Slave Serial Mode Parameters

Clock timing for Slave Serial configuration programming is shown in Figure 3, with Master Serial clock timing shown in Figure 4. Programming parameters for both Slave and Master modes are given in Table 31.

JTAG Test Access Port Switching Characteristics

Characterization data for some of the most commonly requested timing parameters shown in Figure 6 is listed in Table 33.

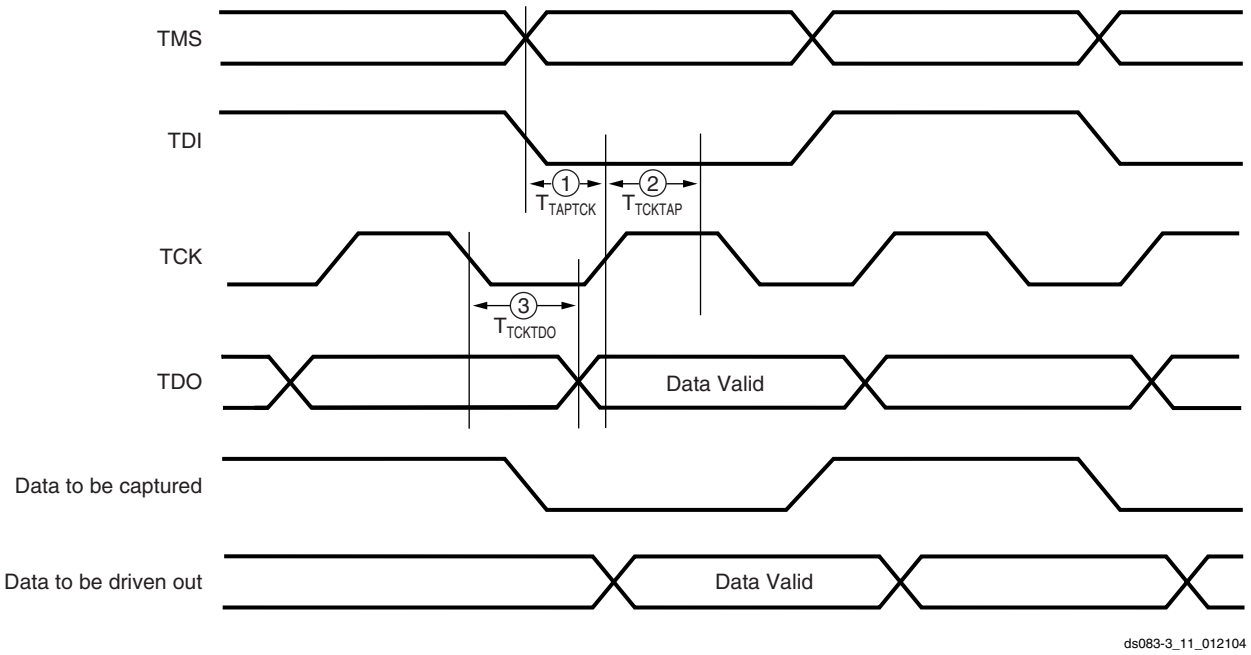


Figure 6: **Virtex-II Pro Boundary Scan Port Timing Waveforms**

Table 33: **Boundary-Scan Port Timing Specifications**

	Description	Figure References	Symbol	Value	Units
TCK	TMS and TDI setup time	1	T_{TAPTCK}	5.5	ns, min
	TMS and TDI hold times	2	T_{TCKTAP}	0.0	ns, min
	Falling edge to TDO output valid	3	T_{TCKTDO}	10.0	ns, max
	Maximum frequency		F_{TCK}	33.0	MHz, max

Output Clock Jitter

Table 40: **Output Clock Jitter**

Description	Symbol	Constraints	Speed Grade			Units
			-6	-5	-4	
Clock Synthesis Period Jitter						
CLK0	CLKOUT_PER_JITT_0		±100	±100	±100	ps
CLK90	CLKOUT_PER_JITT_90		±150	±150	±150	ps
CLK180	CLKOUT_PER_JITT_180		±150	±150	±150	ps
CLK270	CLKOUT_PER_JITT_270		±150	±150	±150	ps
CLK2X, CLK2X180	CLKOUT_PER_JITT_2X		±200	±200	±200	ps
CLKDV (integer division)	CLKOUT_PER_JITT_DV1		±150	±150	±150	ps
CLKDV (non-integer division)	CLKOUT_PER_JITT_DV2		±300	±300	±300	ps
CLKFX, CLKFX180	CLKOUT_PER_JITT_FX		Note 1	Note 1	Note 1	ps

Notes:
1. Values for this parameter are available at www.xilinx.com.

Output Clock Phase Alignment

Table 41: **Output Clock Phase Alignment**

Description	Symbol	Constraints	Speed Grade			Units
			-6	-5	-4	
Phase Offset Between CLKIN and CLKFB						
CLKIN/CLKFB	CLKIN_CLKFB_PHASE		±50	±50	±50	ps
Phase Offset Between Any DCM Outputs						
All CLK outputs	CLKOUT_PHASE		±140	±140	±140	ps
Duty Cycle Precision						
DLL outputs(1)	CLKOUT_DUTY_CYCLE_DLL(2)		±150	±150	±150	ps
CLKFX outputs	CLKOUT_DUTY_CYCLE_FX		±100	±100	±100	ps

Notes:
1. "DLL outputs" is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. CLKOUT_DUTY_CYCLE_DLL applies to the 1X clock outputs (CLK0, CLK90, CLK180, and CLK270) only if DUTY_CYCLE_CORRECTION = TRUE.
3. Specification also applies to PSCLK.

Date	Version	Revision
03/01/05 (*cont'd*)	3.4 (*cont'd*)	• Table 15, Table 17, Table 18, and Table 19: Restructured these I/O-related tables to include descriptions, as well as the actual IOSTANDARD attributes (used in Xilinx ISE™ software) for all I/O standards. • Table 15: Added data for the following I/O standards: SSTL18_I, SSTL18_II, SSTL18_I_DCI, SSTL18_II_DCI, HSTL_I_18, HSTL_II_18, HSTL_III_18, HSTL_IV_18, LVDSEXT_25, LVDSEXT_33, BLVDS_25, LVDS_25_DCI, LVDS_33_DCI, LVDSEXT_25_DCI, LVDSEXT_33_DCI, HSLVDCI_15, HSLVDCI_18, HSLVDCI_25, HSLVDCI_33. Rearranged I/O standards in a more logical order. • Table 16: Added parameter T_{RPW} (Minimum Pulse Width, SR Input). • Table 17: Added data for the following I/O standards: SSTL18_I, SSTL18_II, SSTL18_I_DCI, SSTL18_II_DCI, HSLVDCI_15, HSLVDCI_18, HSLVDCI_25, HSLVDCI_33. Changed "Csl" to "C_{REF}" to agree with Figure 1 and Table 19. Rearranged I/O standards in a more logical order. • Table 18: Added data for the following I/O standards: SSTL18_I, SSTL18_II, HSTL_I_18, HSTL_II_18, HSTL_III_18, HSTL_IV_18. Added footnote defining equivalents for DCI standards. • Table 19: Added Footnotes (2) and (3) to PCI/PCI-X capacitive load (C_{REF}) values. Added HSLVDCI callouts to LVDCI parameter rows (same values). • Table 28: Added parameter T_{BCCS}, CLKA to CLKB Setup Time. • Table 31: Added Footnote (1) indicating that F_{CC_SERIAL} should not exceed $F_{CC\_STARTUP}$ if no provision is made to adjust the speed of CCLK. • Table 33: T_{TCKTDO} corrected from a "Min" to a "Max" specification.
11/05/07	3.5	• Updated copyright notice and legal disclaimer.

Notice of Disclaimer

Virtex-II Data Sheet

The Virtex-II Data Sheet contains the following modules:

- Virtex-II Platform FPGAs: Introduction and Overview (Module 1)
- Virtex-II Platform FPGAs: Functional Description (Module 2)
- Virtex-II Platform FPGAs: DC and Switching Characteristics (Module 3)
- Virtex-II Platform FPGAs: Pinout Information (Module 4)

Table 6: **FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
3	IO_L96N_3	J16		
3	IO_L96P_3	J15		
3	IO_L94N_3	J14		
3	IO_L94P_3	J13		
3	IO_L93N_3/VREF_3	K16	NC	
3	IO_L93P_3	K15	NC	
3	IO_L91N_3	K14	NC	
3	IO_L91P_3	K13	NC	
3	IO_L45N_3/VREF_3	K12	NC	NC
3	IO_L45P_3	L12	NC	NC
3	IO_L43N_3	L16	NC	NC
3	IO_L43P_3	L15	NC	NC
3	IO_L06N_3	L14	NC	
3	IO_L06P_3	L13	NC	
3	IO_L04N_3	M16	NC	
3	IO_L04P_3	M15	NC	
3	IO_L03N_3/VREF_3	M14		
3	IO_L03P_3	M13		
3	IO_L02N_3/VRP_3	N15		
3	IO_L02P_3/VRN_3	N14		
3	IO_L01N_3	N16		
3	IO_L01P_3	P16		
4	IO_L01N_4/BUSY/DOUT(1)	T14		
4	IO_L01P_4/INIT_B	T13		
4	IO_L02N_4/D0/DIN(1)	P13		
4	IO_L02P_4/D1	R13		
4	IO_L03N_4/D2/ALT_VRP_4	N12		
4	IO_L03P_4/D3/ALT_VRN_4	P12		
4	IO_L04N_4/VREF_4	R12	NC	NC
4	IO_L04P_4	T12	NC	NC
4	IO_L05N_4/VRP_4	N11	NC	NC
4	IO_L05P_4/VRN_4	P11	NC	NC

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
4	IO_L02N_4/D0/DIN(1)	V18		
4	IO_L02P_4/D1	V17		
4	IO_L03N_4/D2/ALT_VRP_4	W18		
4	IO_L03P_4/D3/ALT_VRN_4	Y18		
4	IO_L04N_4/VREF_4	AA18		
4	IO_L04P_4	AB18		
4	IO_L05N_4/VRP_4	W17		
4	IO_L05P_4/VRN_4	Y17		
4	IO_L06N_4	AA17		
4	IO_L06P_4	AB17		
4	IO_L19N_4	V16	NC	NC
4	IO_L19P_4	V15	NC	NC
4	IO_L21N_4	W16	NC	NC
4	IO_L21P_4/VREF_4	Y16	NC	NC
4	IO_L22N_4	AA16	NC	NC
4	IO_L22P_4	AB16	NC	NC
4	IO_L24N_4	W15	NC	NC
4	IO_L24P_4	Y15	NC	NC
4	IO_L49N_4	AA15	NC	
4	IO_L49P_4	AB15	NC	
4	IO_L51N_4	U14	NC	
4	IO_L51P_4/VREF_4	V14	NC	
4	IO_L52N_4	W14	NC	
4	IO_L52P_4	Y14	NC	
4	IO_L54N_4	AA14	NC	
4	IO_L54P_4	AB14	NC	
4	IO_L91N_4/VREF_4	U13		
4	IO_L91P_4	V13		
4	IO_L92N_4	W13		
4	IO_L92P_4	Y13		
4	IO_L93N_4	AA13		
4	IO_L93P_4	AB13		
4	IO_L94N_4/VREF_4	U12		
4	IO_L94P_4	V12		

FG676/FGG676 Fine-Pitch BGA Package

As shown in Table 8, XC2V1500, XC2V2000, and XC2V3000 Virtex-II devices are available in the FG676/FGG676 fine-pitch BGA package. Pins in the XC2V1500, XC2V2000, and XC2V3000 devices are the same, except for the pin differences in the XC2V1500 and XC2V2000 devices shown in the No Connect columns. Following this table are the FG676/FGG676 Fine-Pitch BGA Package Specifications (1.00mm pitch).

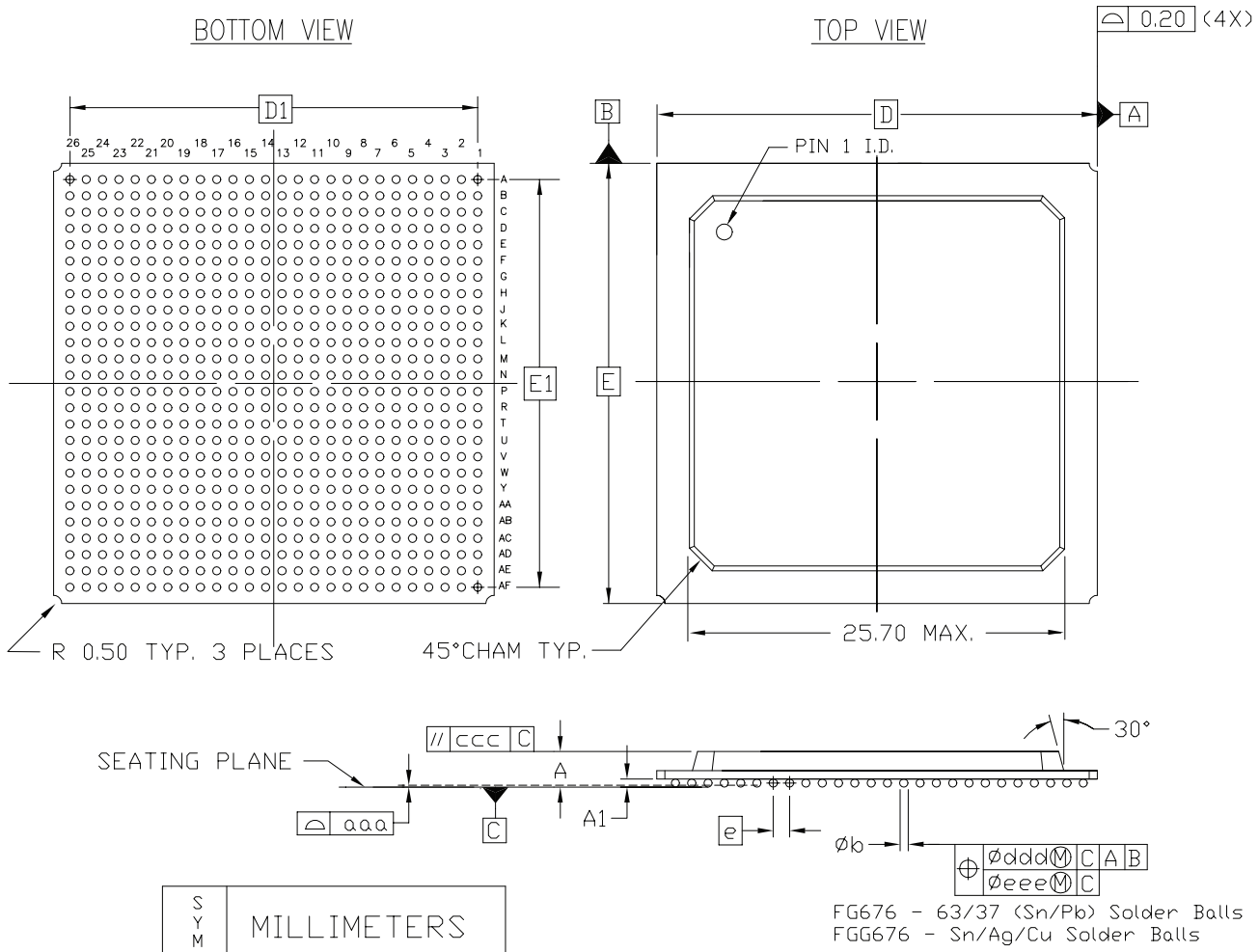
Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
0	IO_L01N_0	D6		
0	IO_L01P_0	C6		
0	IO_L02N_0	B1		
0	IO_L02P_0	A2		
0	IO_L03N_0/VRP_0	D7		
0	IO_L03P_0/VRN_0	C7		
0	IO_L04N_0/VREF_0	B3		
0	IO_L04P_0	A3		
0	IO_L05N_0	G6		
0	IO_L05P_0	G7		
0	IO_L06N_0	E6		
0	IO_L06P_0	E7		
0	IO_L19N_0	B4		
0	IO_L19P_0	A4		
0	IO_L21N_0	B5		
0	IO_L21P_0/VREF_0	A5		
0	IO_L22N_0	B6		
0	IO_L22P_0	A6		
0	IO_L24N_0	A7		
0	IO_L24P_0	A8		
0	IO_L25N_0	E8	NC	NC
0	IO_L25P_0	D8	NC	NC
0	IO_L27N_0	G8	NC	NC
0	IO_L27P_0/VREF_0	F8	NC	NC
0	IO_L49N_0	C8		
0	IO_L49P_0	B8		
0	IO_L51N_0	D9		
0	IO_L51P_0/VREF_0	E9		
0	IO_L52N_0	F9		
0	IO_L52P_0	G9		
0	IO_L54N_0	B9		
0	IO_L54P_0	A9		
0	IO_L67N_0	C9		

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
6	IO_L52N_6	U1		
6	IO_L54P_6	U7		
6	IO_L54N_6	T7		
6	IO_L67P_6	U4		
6	IO_L67N_6	U3		
6	IO_L69P_6	U6		
6	IO_L69N_6/VREF_6	U5		
6	IO_L70P_6	T5		
6	IO_L70N_6	T6		
6	IO_L72P_6	T8		
6	IO_L72N_6	R8		
6	IO_L73P_6	T2	NC	
6	IO_L73N_6	T1	NC	
6	IO_L75P_6	T4	NC	
6	IO_L75N_6/VREF_6	T3	NC	
6	IO_L76P_6	R6	NC	
6	IO_L76N_6	R5	NC	
6	IO_L78P_6	R4	NC	
6	IO_L78N_6	R3	NC	
6	IO_L91P_6	R2		
6	IO_L91N_6	R1		
6	IO_L93P_6	R7		
6	IO_L93N_6/VREF_6	P7		
6	IO_L94P_6	P6		
6	IO_L94N_6	P5		
6	IO_L96P_6	P4		
6	IO_L96N_6	P3		
7	IO_L96P_7	P1		
7	IO_L96N_7	N1		
7	IO_L94P_7	N4		
7	IO_L94N_7	N5		
7	IO_L93P_7/VREF_7	N6		
7	IO_L93N_7	N7		
7	IO_L91P_7	P8		
7	IO_L91N_7	N8		
7	IO_L78P_7	M1	NC	

FG676/FGG676 Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A		2.25	2.60
A_1	0.40	0.50	0.60
D/E	27.00 BSC		
D_1/E_1	25.00 REF		
e	1.00 BSC		
øb	0.50	0.60	0.70
aaa			0.20
ccc			0.35
ddd			0.30
eee			0.10
M	26		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-AAL-1

676-BALL FINE PITCH BGA (FG676/FGG676)

Figure 4: **FG676/FGG676 Fine-Pitch BGA Package Specifications**

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
6	IO_L91N_6	P4		
6	IO_L93P_6	N4		
6	IO_L93N_6/VREF_6	N3		
6	IO_L94P_6	N6		
6	IO_L94N_6	N5		
6	IO_L96P_6	N8		
6	IO_L96N_6	N7		
7	IO_L96P_7	N2		
7	IO_L96N_7	M1		
7	IO_L94P_7	M2		
7	IO_L94N_7	M3		
7	IO_L93P_7/VREF_7	M4		
7	IO_L93N_7	M5		
7	IO_L91P_7	M6		
7	IO_L91N_7	M7		
7	IO_L73P_7	M8	NC	NC
7	IO_L73N_7	L8	NC	NC
7	IO_L72P_7	L1	NC	
7	IO_L72N_7	K1	NC	
7	IO_L70P_7	K2	NC	
7	IO_L70N_7	K3	NC	
7	IO_L69P_7/VREF_7	L3	NC	
7	IO_L69N_7	L4	NC	
7	IO_L67P_7	L5	NC	
7	IO_L67N_7	L7	NC	
7	IO_L54P_7	J1		
7	IO_L54N_7	H1		
7	IO_L52P_7	J2		
7	IO_L52N_7	J3		
7	IO_L51P_7/VREF_7	J4		
7	IO_L51N_7	J5		
7	IO_L49P_7	K5		
7	IO_L49N_7	K6		
7	IO_L48P_7	F1		
7	IO_L48N_7	F2		

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
NA	GND	Y5		
NA	GND	W19		
NA	GND	W6		
NA	GND	V24		
NA	GND	V18		
NA	GND	V7		
NA	GND	V1		
NA	GND	R21		
NA	GND	R4		
NA	GND	P14		
NA	GND	P13		
NA	GND	P12		
NA	GND	P11		
NA	GND	N14		
NA	GND	N13		
NA	GND	N12		
NA	GND	N11		
NA	GND	M14		
NA	GND	M13		
NA	GND	M12		
NA	GND	M11		
NA	GND	L14		
NA	GND	L13		
NA	GND	L12		
NA	GND	L11		
NA	GND	K21		
NA	GND	K4		
NA	GND	G24		
NA	GND	G18		
NA	GND	G7		
NA	GND	G1		
NA	GND	F19		
NA	GND	F6		
NA	GND	E20		
NA	GND	E5		
NA	GND	D21		

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
3	IO_L19N_3	AB26
3	IO_L19P_3	AB25
3	IO_L06N_3	AB24
3	IO_L06P_3	AB23
3	IO_L04N_3	AC27
3	IO_L04P_3	AC26
3	IO_L03N_3/VREF_3	AC25
3	IO_L03P_3	AC24
3	IO_L02N_3/VRP_3	AD27
3	IO_L02P_3/VRN_3	AE27
3	IO_L01N_3	AD26
3	IO_L01P_3	AD25
4	IO_L01N_4/BUSY/DOUT(1)	AF25
4	IO_L01P_4/INIT_B	AG25
4	IO_L02N_4/D0/DIN(1)	AF24
4	IO_L02P_4/D1	AG24
4	IO_L03N_4/D2/ALT_VRP_4	AD23
4	IO_L03P_4/D3/ALT_VRN_4	AE23
4	IO_L04N_4/VREF_4	AF23
4	IO_L04P_4	AG23
4	IO_L05N_4/VRP_4	AD22
4	IO_L05P_4/VRN_4	AE22
4	IO_L06N_4	AF22
4	IO_L06P_4	AG22
4	IO_L19N_4	AC21
4	IO_L19P_4	AB21
4	IO_L21N_4	AE21
4	IO_L21P_4/VREF_4	AE20
4	IO_L22N_4	AF21
4	IO_L22P_4	AG21
4	IO_L24N_4	AB20
4	IO_L24P_4	AA20
4	IO_L25N_4	AC20
4	IO_L25P_4	AD20
4	IO_L27N_4	AG20

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
7	IO_L27P_7/VREF_7	H5
7	IO_L27N_7	H6
7	IO_L25P_7	J7
7	IO_L25N_7	J8
7	IO_L24P_7	G1
7	IO_L24N_7	F1
7	IO_L22P_7	G2
7	IO_L22N_7	G3
7	IO_L21P_7/VREF_7	F2
7	IO_L21N_7	F3
7	IO_L19P_7	G5
7	IO_L19N_7	G6
7	IO_L06P_7	F4
7	IO_L06N_7	F5
7	IO_L04P_7	E1
7	IO_L04N_7	E2
7	IO_L03P_7/VREF_7	D1
7	IO_L03N_7	C1
7	IO_L02P_7/VRN_7	E3
7	IO_L02N_7/VRP_7	E4
7	IO_L01P_7	D2
7	IO_L01N_7	D3
0	VCCO_0	K13
0	VCCO_0	K12
0	VCCO_0	K11
0	VCCO_0	J11
0	VCCO_0	J10
0	VCCO_0	G12
0	VCCO_0	D7
0	VCCO_0	C12
1	VCCO_1	K17
1	VCCO_1	K16
1	VCCO_1	K15
1	VCCO_1	J18
1	VCCO_1	J17

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
NA	GND	F22
NA	GND	F6
NA	GND	E23
NA	GND	E17
NA	GND	E11
NA	GND	E5
NA	GND	D24
NA	GND	D14
NA	GND	D4
NA	GND	C25
NA	GND	C3
NA	GND	B27
NA	GND	B26
NA	GND	B20
NA	GND	B8
NA	GND	B2
NA	GND	B1
NA	GND	A27
NA	GND	A26
NA	GND	A14
NA	GND	A2

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
4	IO_L32P_4	AM14	NC	
4	IO_L33N_4	AT10	NC	
4	IO_L33P_4/VREF_4	AT9	NC	
4	IO_L34N_4	AV10	NC	
4	IO_L34P_4	AV9	NC	
4	IO_L35N_4	AH16	NC	
4	IO_L35P_4	AH17	NC	
4	IO_L36N_4	AP13	NC	
4	IO_L36P_4	AP12	NC	
4	IO_L49N_4	AU12		
4	IO_L49P_4	AU11		
4	IO_L50N_4	AK15		
4	IO_L50P_4	AJ16		
4	IO_L51N_4	AT12		
4	IO_L51P_4/VREF_4	AT11		
4	IO_L52N_4	AN15		
4	IO_L52P_4	AN14		
4	IO_L53N_4	AR12		
4	IO_L53P_4	AR13		
4	IO_L54N_4	AT14		
4	IO_L54P_4	AT13		
4	IO_L55N_4	AW11		
4	IO_L55P_4	AW10		
4	IO_L56N_4	AM15		
4	IO_L56P_4	AM16		
4	IO_L57N_4	AP15		
4	IO_L57P_4/VREF_4	AP14		
4	IO_L58N_4	AV13		
4	IO_L58P_4	AV12		
4	IO_L59N_4	AK16		
4	IO_L59P_4	AK17		
4	IO_L60N_4	AR16		
4	IO_L60P_4	AR15		
4	IO_L67N_4	AW13		
4	IO_L67P_4	AW12		
4	IO_L68N_4	AL16		