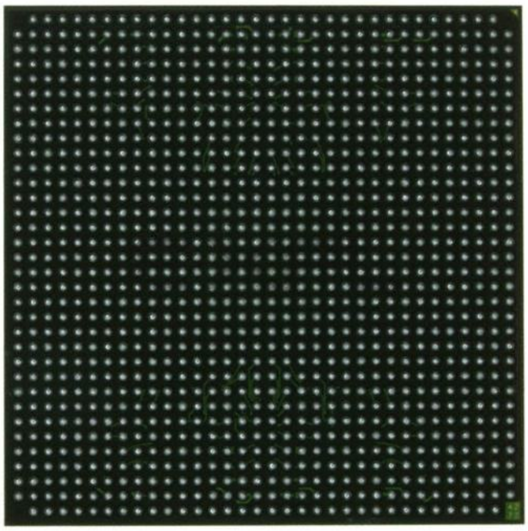

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 3584 |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 1769472 |
| Number of I/O | 720 |
| Number of Gates | 3000000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 1152-BBGA, FCBGA |
| Supplier Device Package | 1152-FCBGA (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc2v3000-4ffg1152i |

*Table 1:* **Virtex-II Field-Programmable Gate Array Family Members**

| Device | System Gates | CLB (1 CLB = 4 slices = Max 128 bits) | | | Multiplier Blocks | SelectRAM Blocks | | DCMs | Max I/O Pads(1) |
|---|---|---|---|---|---|---|---|---|---|
| | | Array Row x Col. | Slices | Maximum Distributed RAM Kbits | | 18 Kbit Blocks | Max RAM (Kbits) | | |
| XC2V40 | 40K | 8 x 8 | 256 | 8 | 4 | 4 | 72 | 4 | 88 |
| XC2V80 | 80K | 16 x 8 | 512 | 16 | 8 | 8 | 144 | 4 | 120 |
| XC2V250 | 250K | 24 x 16 | 1,536 | 48 | 24 | 24 | 432 | 8 | 200 |
| XC2V500 | 500K | 32 x 24 | 3,072 | 96 | 32 | 32 | 576 | 8 | 264 |
| XC2V1000 | 1M | 40 x 32 | 5,120 | 160 | 40 | 40 | 720 | 8 | 432 |
| XC2V1500 | 1.5M | 48 x 40 | 7,680 | 240 | 48 | 48 | 864 | 8 | 528 |
| XC2V2000 | 2M | 56 x 48 | 10,752 | 336 | 56 | 56 | 1,008 | 8 | 624 |
| XC2V3000 | 3M | 64 x 56 | 14,336 | 448 | 96 | 96 | 1,728 | 12 | 720 |
| XC2V4000 | 4M | 80 x 72 | 23,040 | 720 | 120 | 120 | 2,160 | 12 | 912 |
| XC2V6000 | 6M | 96 x 88 | 33,792 | 1,056 | 144 | 144 | 2,592 | 12 | 1,104 |
| XC2V8000 | 8M | 112 x 104 | 46,592 | 1,456 | 168 | 168 | 3,024 | 12 | 1,108 |

**Notes:**
1. See details in Table 2, "Maximum Number of User I/O Pads".

## General Description

The Virtex-II family is a platform FPGA developed for high performance from low-density to high-density designs that are based on IP cores and customized modules. The family delivers complete solutions for telecommunication, wireless, networking, video, and DSP applications, including PCI, LVDS, and DDR interfaces.

The leading-edge 0.15 µm / 0.12 µm CMOS 8-layer metal process and the Virtex-II architecture are optimized for high speed with low power consumption. Combining a wide variety of flexible features and a large range of densities up to 10 million system gates, the Virtex-II family enhances programmable logic design capabilities and is a powerful alternative to mask-programmed gates arrays. As shown in Table 1, the Virtex-II family comprises 11 members, ranging from 40K to 8M system gates.

### Packaging

Offerings include ball grid array (BGA) packages with 0.80 mm, 1.00 mm, and 1.27 mm pitches. In addition to traditional wire-bond interconnects, flip-chip interconnect is used in some of the BGA offerings. The use of flip-chip interconnect offers more I/Os than is possible in wire-bond versions of the similar packages. Flip-chip construction offers the combination of high pin count with high thermal capacity.

Wire-bond packages CS, FG, and BG are optionally availabe in Pb-free versions CSG, FGG, and BGG. See Virtex-II Ordering Examples, page 6.

Table 2 shows the maximum number of user I/Os available. The Virtex-II device/package combination table (Table 6 at the end of this section) details the maximum number of I/Os for each device and package using wire-bond or flip-chip technology.

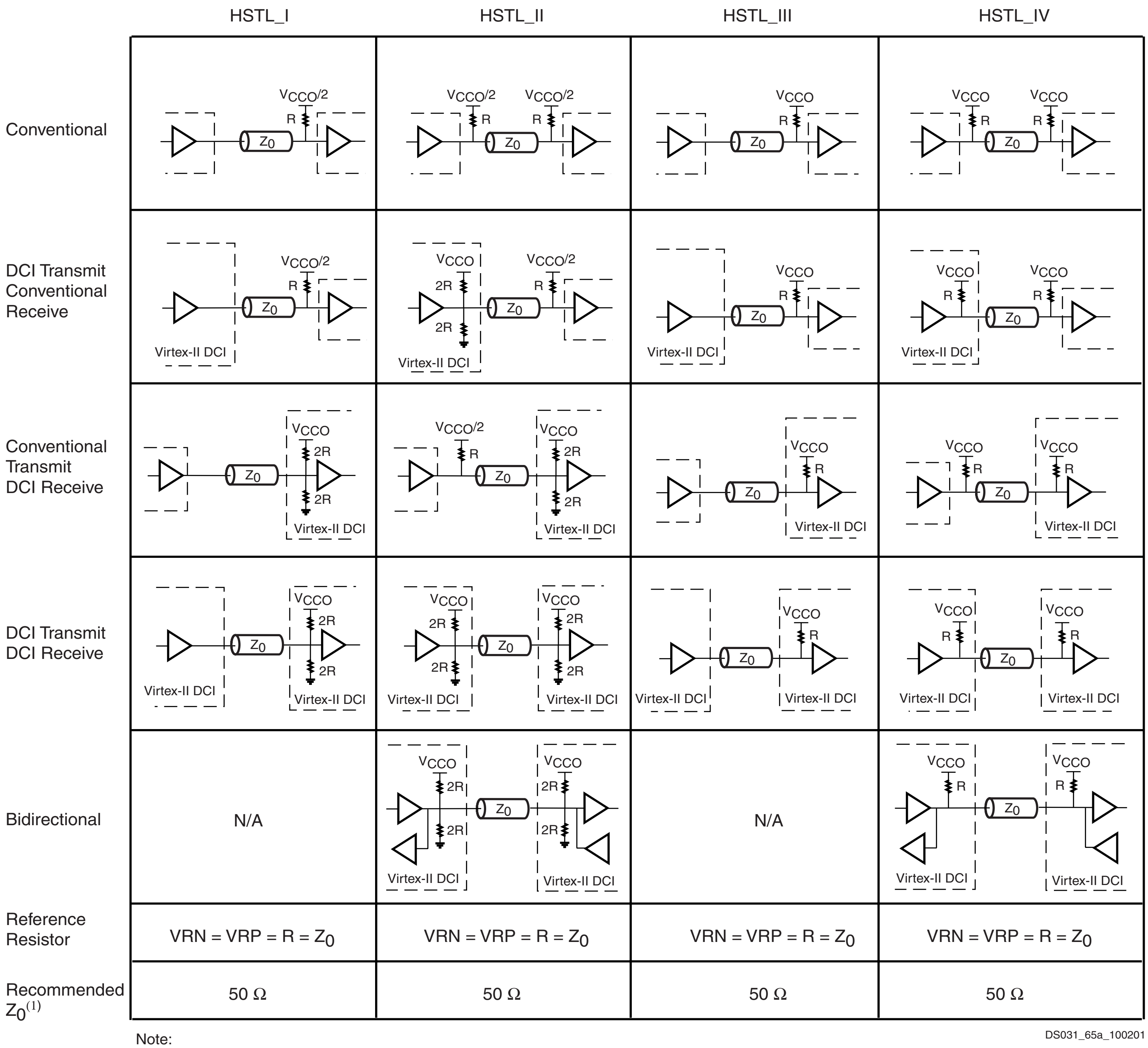
*Table 2:* **Maximum Number of User I/O Pads**

| Device | Wire-Bond | Flip-Chip |
|---|---|---|
| XC2V40 | 88 | - |
| XC2V80 | 120 | - |
| XC2V250 | 200 | - |
| XC2V500 | 264 | - |
| XC2V1000 | 328 | 432 |
| XC2V1500 | 392 | 528 |
| XC2V2000 | - | 624 |
| XC2V3000 | 516 | 720 |
| XC2V4000 | - | 912 |
| XC2V6000 | - | 1,104 |
| XC2V8000 | - | 1,108 |

*Table 8:* **SelectI/O-Ultra Differential Buffers With On-Chip Termination**

| I/O Standard Description | IOSTANDARD Attribute | |
|---|---|---|
| | External Termination | On-Chip Termination |
| LVDS 2.5V | LVDS_25 | LVDS_25_DCI |
| LVDS Extended 2.5V | LVDSEXT_25 | LVDSEXT_25_DCI |

Figure 11 provides examples illustrating the use of the HSTL_I_DCI, HSTL_II_DCI, HSTL_III_DCI, and HSTL_IV_DCI I/O standards. For a complete list, see the **Virtex-II Platform FPGA User Guide**.




Note:
1. $Z_0$ is the recommended PCB trace impedance.

*Figure 11:* **HSTL DCI Usage Examples**

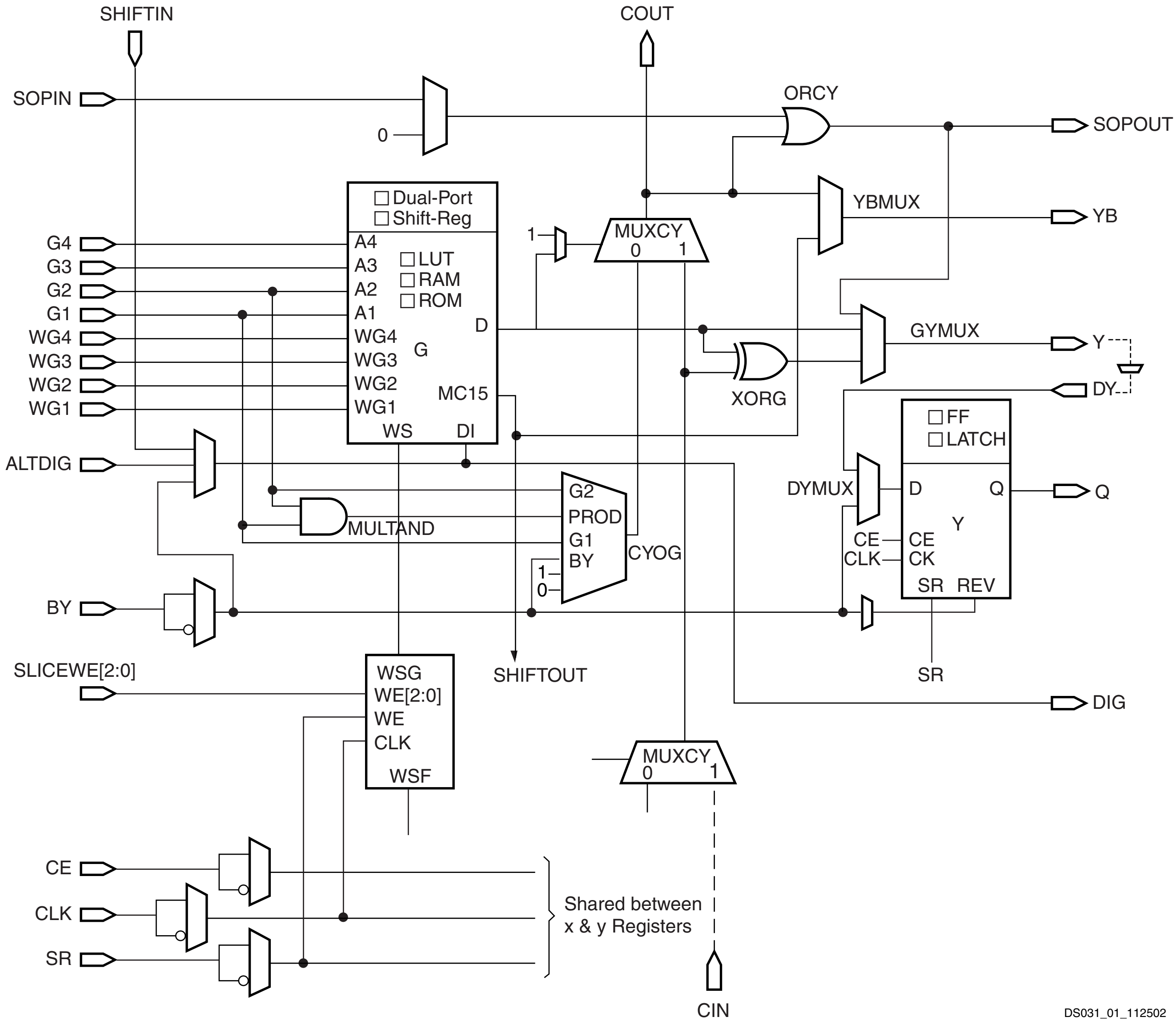



*Figure 16:* **Virtex-II Slice (Top Half)**

### Multiplexers

Virtex-II function generators and associated multiplexers can implement the following:

- 4:1 multiplexer in one slice
- 8:1 multiplexer in two slices
- 16:1 multiplexer in one CLB element (4 slices)
- 32:1 multiplexer in two CLB elements (8 slices)

Each Virtex-II slice has one MUXF5 multiplexer and one MUXFX multiplexer. The MUXFX multiplexer implements the MUXF6, MUXF7, or MUXF8, as shown in Figure 23. Each CLB element has two MUXF6 multiplexers, one MUXF7 multiplexer and one MUXF8 multiplexer. Examples of multiplexers are shown in the *Virtex-II Platform FPGA User Guide*. Any LUT can implement a 2:1 multiplexer.

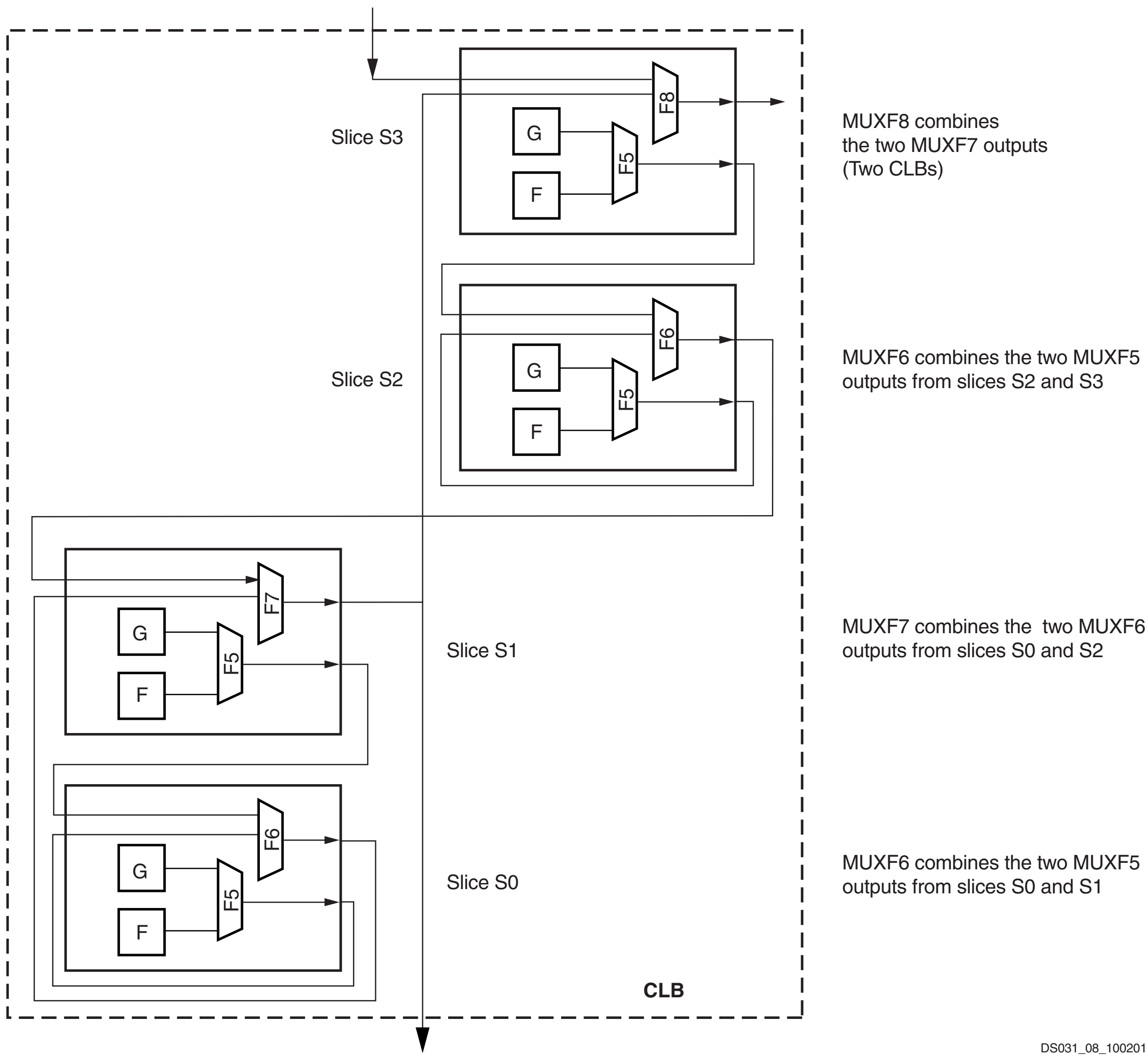



*Figure 23:* **MUXF5 and MUXFX multiplexers**

### Fast Lookahead Carry Logic

Dedicated carry logic provides fast arithmetic addition and subtraction. The Virtex-II CLB has two separate carry chains, as shown in the Figure 24.

The height of the carry chains is two bits per slice. The carry chain in the Virtex-II device is running upward. The dedicated carry path and carry multiplexer (MUXCY) can also be used to cascade function generators for implementing wide logic functions.

### Arithmetic Logic

The arithmetic logic includes an XOR gate that allows a 2-bit full adder to be implemented within a slice. In addition, a dedicated AND (MULT_AND) gate (shown in Figure 16) improves the efficiency of multiplier implementation.

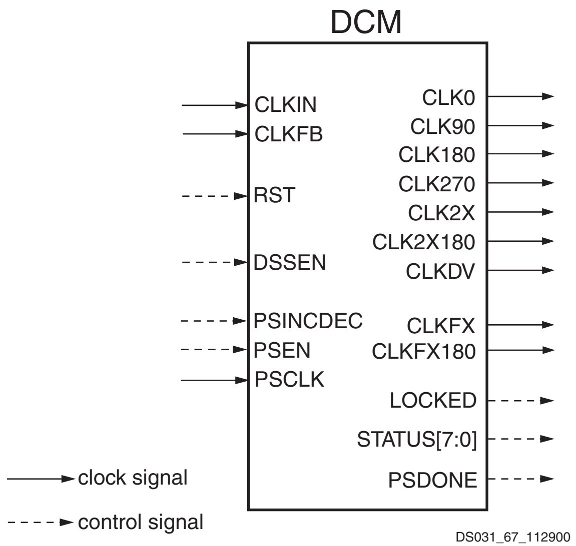



*Figure 45:* **Digital Clock Manager**

The DCM can be configured to delay the completion of the Virtex-II configuration process until after the DCM has achieved lock. This guarantees that the chip does not begin operating until after the system clocks generated by the DCM have stabilized.

The DCM has the following general control signals:

- RST input pin: resets the entire DCM
- LOCKED output pin: asserted High when all enabled DCM circuits have locked.
- STATUS output pins (active High): shown in Table 21.

*Table 21:* **DCM Status Pins**

| Status Pin | Function |
|---|---|
| 0 | Phase Shift Overflow |
| 1 | CLKIN Stopped |
| 2 | CLKFX Stopped |
| 3 | N/A |
| 4 | N/A |
| 5 | N/A |
| 6 | N/A |
| 7 | N/A |

### Clock De-Skew

The DCM de-skews the output clocks relative to the input clock by automatically adjusting a digital delay line. Additional delay is introduced so that clock edges arrive at internal registers and block RAMs simultaneously with the clock edges arriving at the input clock pad. Alternatively, external clocks, which are also de-skewed relative to the input clock, can be generated for board-level routing. All DCM output clocks are phase-aligned to CLK0 and, therefore, are also phase-aligned to the input clock.

To achieve clock de-skew, the CLKFB input must be connected, and its source must be either CLK0 or CLK2X. Note that CLKFB must always be connected, unless only the CLKFX or CLKFX180 outputs are used and de-skew is not required.

### Frequency Synthesis

The DCM provides flexible methods for generating new clock frequencies. Each method has a different operating frequency range and different AC characteristics. The CLK2X and CLK2X180 outputs double the clock frequency. The CLKDV output creates divided output clocks with division options of 1.5, 2, 2.5, 3, 3.5, 4, 4.5, 5, 5.5, 6, 6.5, 7, 7.5, 8, 9, 10, 11, 12, 13, 14, 15, and 16.

The CLKFX and CLKFX180 outputs can be used to produce clocks at the following frequency:

$$FREQ_{CLKFX} = (M/D) * FREQ_{CLKIN}$$

where M and D are two integers. Specifications for M and D are provided under DCM Timing Parameters in Module 3. By default, M=4 and D=1, which results in a clock output frequency four times faster than the clock input frequency (CLKIN).

CLK2X180 is phase shifted 180 degrees relative to CLK2X. CLKFX180 is phase shifted 180 degrees relative to CLKFX. All frequency synthesis outputs automatically have 50/50 duty cycles (with the exception of the CLKDV output when performing a non-integer divide in high-frequency mode).

Note that CLK2X and CLK2X180 are not available in high-frequency mode.

### Phase Shifting

The DCM provides additional control over clock skew through either coarse or fine-grained phase shifting. The CLK0, CLK90, CLK180, and CLK270 outputs are each phase shifted by ¼ of the input clock period relative to each other, providing coarse phase control. Note that CLK90 and CLK270 are not available in high-frequency mode.

Fine-phase adjustment affects all nine DCM output clocks. When activated, the phase shift between the rising edges of CLKIN and CLKFB is a specified fraction of the input clock period.

In variable mode, the PHASE_SHIFT value can also be dynamically incremented or decremented as determined by PSINCDEC synchronously to PSCLK, when the PSEN input is active. Figure 46 illustrates the effects of fine-phase shifting. For more information on DCM features, see the Virtex-II *User Guide*.

# Virtex-II Electrical Characteristics

Virtex-II™ devices are provided in -6, -5, and -4 speed grades, with -6 having the highest performance.

Virtex-II DC and AC characteristics are specified for both commercial and industrial grades. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -4 speed grade industrial device are the same as for a -4 speed grade commercial device). However, only selected speed grades and/or devices might be available in the industrial range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications. Contact Xilinx for design considerations requiring more detailed information.

All specifications are subject to change without notice.

## Virtex-II DC Characteristics

*Table 1:* **Absolute Maximum Ratings**

| Symbol | Description(1) | | | Units |
|---|---|---|---|---|
| $V_{CCINT}$ | Internal supply voltage relative to GND | | –0.5 to 1.65 | V |
| $V_{CCAUX}$ | Auxiliary supply voltage relative to GND | | –0.5 to 4.0 | V |
| $V_{CCO}$ | Output drivers supply voltage relative to GND | | –0.5 to 4.0 | V |
| $V_{BATT}$ | Key memory battery backup supply | | –0.5 to 4.0 | V |
| $V_{REF}$ | Input reference voltage | | –0.5 to $V_{CCO}$ + 0.5 | V |
| $V_{IN}$(3) | Input voltage relative to GND (user and dedicated I/Os) | | –0.5 to $V_{CCO}$ + 0.5 | V |
| $V_{TS}$ | Voltage applied to 3-state output (user and dedicated I/Os) | | –0.5 to 4.0 | V |
| $T_{STG}$ | Storage temperature (ambient) | | –65 to +150 | °C |
| $T_{SOL}$ | Maximum soldering temperature(2) | All regular FF/BF flip-chip and FG/BG/CS wire-bond packages | +220 | °C |
| | | Pb-free FGG456, FGG676, BGG575, and BGG728 wire-bond packages | +250 | °C |
| | | Pb-free FGG256 and CSG144 wire-bond packages | +260 | °C |
| $T_J$ | Maximum junction temperature(2) | | +125 | °C |

**Notes:**
1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. For soldering guidelines and thermal considerations, see the **Device Packaging and Thermal Characteristics Guide** information on the Xilinx website.
3. Inputs configured as PCI are fully PCI compliant. This statement takes precedence over any specification that would imply that the device is not PCI compliant.

*Table 19:* **Output Delay Measurement Methodology**

| Description | IOSTANDARD Attribute | $R_{REF}$ (Ω) | $C_{REF}$(1) (pF) | $V_{MEAS}$ (V) | $V_{REF}$ (V) |
|---|---|---|---|---|---|
| SSTL (Stub Series Terminated Logic), Class I, 1.8V | SSTL18_I | 50 | 0 | $V_{REF}$ | 0.9 |
| SSTL, Class II, 1.8V | SSTL18_II | 25 | 0 | $V_{REF}$ | 0.9 |
| SSTL, Class I, 2.5V | SSTL2_I | 50 | 0 | $V_{REF}$ | 1.25 |
| SSTL, Class II, 2.5V | SSTL2_II | 25 | 0 | $V_{REF}$ | 1.25 |
| SSTL, Class I, 3.3V | SSTL3_I | 50 | 0 | $V_{REF}$ | 1.5 |
| SSTL, Class II, 3.3V | SSTL3_II | 25 | 0 | $V_{REF}$ | 1.5 |
| AGP-2X/AGP (Accelerated Graphics Port) | AGP-2X/AGP (rising edge) | 50 | 0 | 0.94 | 0 |
| | AGP-2X/AGP (falling edge) | 50 | 0 | 2.03 | 3.3 |
| LVDS (Low-Voltage Differential Signaling), 2.5V | LVDS_25 | 50 | 0 | $V_{REF}$ | 1.2 |
| LVDS, 3.3V | LVDSEXT_25 | 50 | 0 | $V_{REF}$ | 1.2 |
| LVDSEXT (LVDS Extended Mode), 2.5V | LVDS_33 | 50 | 0 | $V_{REF}$ | 1.2 |
| LVDSEXT, 3.3V | LVDSEXT_33 | 50 | 0 | $V_{REF}$ | 1.2 |
| BLVDS (Bus LVDS), 2.5V | BLVDS_25 | 1M | 0 | 1.2 | 0 |
| LDT (HyperTransport), 2.5V | LDT_25 | 50 | 0 | $V_{REF}$ | 0.6 |
| LVPECL (Low-Voltage Positive Electron-Coupled Logic), 3.3V | LVPECL_33 | 1M | 0 | 1.23 | 0 |
| LVDCI/HSLVDCI (Low-Voltage Digitally Controlled Impedance), 3.3V | LVDCI_33, HSLVDCI_33 | 1M | 0 | 1.65 | 0 |
| LVDCI/HSLVDCI, 2.5V | LVDCI_25, HSLVDCI_25 | 1M | 0 | 1.25 | 0 |
| LVDCI/HSLVDCI, 1.8V | LVDCI_18, HSLVDCI_18 | 1M | 0 | 0.9 | 0 |
| LVDCI/HSLVDCI, 1.5V | LVDCI_15, HSLVDCI_15 | 1M | 0 | 0.75 | 0 |
| HSTL (High-Speed Transceiver Logic), Class I & II, with DCI | HSTL_I_DCI, HSTL_II_DCI | 50 | 0 | $V_{REF}$ | 0.75 |
| HSTL, Class III & IV, with DCI | HSTL_III_DCI, HSTL_IV_DCI | 50 | 0 | 0.9 | 1.5 |
| HSTL, Class I & II, 1.8V, with DCI | HSTL_I_DCI_18, HSTL_II_DCI_18 | 50 | 0 | $V_{REF}$ | 0.9 |
| HSTL, Class III & IV, 1.8V, with DCI | HSTL_III_DCI_18, HSTL_IV_DCI_18 | 50 | 0 | 1.1 | 1.8 |
| SSTL (Stub Series Termi.Logic), Class I & II, 1.8V, with DCI | SSTL18_I_DCI, SSTL18_II_DCI | 50 | 0 | $V_{REF}$ | 0.9 |
| SSTL, Class I & II, 2.5V, with DCI | SSTL2_I_DCI, SSTL2_II_DCI | 50 | 0 | $V_{REF}$ | 1.25 |
| SSTL, Class I & II, 3.3V, with DCI | SSTL3_I_DCI, SSTL3_II_DCI | 50 | 0 | $V_{REF}$ | 1.5 |
| GTL (Gunning Transceiver Logic) with DCI | GTL_DCI | 50 | 0 | 0.8 | 1.2 |
| GTL Plus with DCI | GTLP_DCI | 50 | 0 | 1.0 | 1.5 |

**Notes:**
1. $C_{REF}$ is the capacitance of the probe, nominally 0 pF.
2. Per PCI specifications.
3. Per PCI-X specifications.

## Clock Distribution Switching Characteristics

*Table 20:* **Clock Distribution Switching Characteristics**

| Description | Symbol | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -6 | -5 | -4 | |
| Global Clock Buffer I input to O output | $T_{GIO}$ | 0.47 | 0.52 | 0.59 | ns, Max |
| Global Clock Buffer S input Setup/Hold to I1 an I2 inputs | $T_{GSI}/T_{GIS}$ | 0.55/ 0 | 0.61/ 0 | 0.70/ 0 | ns, Max |

## CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used (see Figure 16 in Module 2). The values listed below are worst-case. Precise values are provided by the timing analyzer.

*Table 21:* **CLB Switching Characteristics**

| Description | Symbol | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -6 | -5 | -4 | |
| **Combinatorial Delays** | | | | | |
| 4-input function: F/G inputs to X/Y outputs | $T_{ILO}$ | 0.35 | 0.39 | 0.44 | ns, Max |
| 5-input function: F/G inputs to F5 output | $T_{IF5}$ | 0.57 | 0.63 | 0.72 | ns, Max |
| 5-input function: F/G inputs to X output | $T_{IF5X}$ | 0.76 | 0.83 | 0.95 | ns, Max |
| FXINA or FXINB inputs to Y output via MUXFX | $T_{IFXY}$ | 0.36 | 0.39 | 0.45 | ns, Max |
| FXINA input to FX output via MUXFX | $T_{INAFX}$ | 0.26 | 0.28 | 0.32 | ns, Max |
| FXINB input to FX output via MUXFX | $T_{INBFX}$ | 0.26 | 0.28 | 0.32 | ns, Max |
| SOPIN input to SOPOUT output via ORCY | $T_{SOPSOP}$ | 0.35 | 0.38 | 0.44 | ns, Max |
| Incremental delay routing through transparent latch to XQ/YQ outputs | $T_{IFNCTL}$ | 0.41 | 0.45 | 0.51 | ns, Max |
| **Sequential Delays** | | | | | |
| FF Clock CLK to XQ/YQ outputs | $T_{CKO}$ | 0.45 | 0.50 | 0.57 | ns, Max |
| Latch Clock CLK to XQ/YQ outputs | $T_{CKLO}$ | 0.54 | 0.59 | 0.68 | ns, Max |
| **Setup and Hold Times Before/After Clock CLK** | | | | | |
| BX/BY inputs | $T_{DICK}/T_{CKDI}$ | 0.30/–0.07 | 0.33/–0.08 | 0.37/–0.09 | ns, Min |
| DY inputs | $T_{DYCK}/T_{CKDY}$ | 0.30/–0.07 | 0.33/–0.08 | 0.37/–0.09 | ns, Min |
| DX inputs | $T_{DXCK}/T_{CKDX}$ | 0.30/–0.07 | 0.33/–0.08 | 0.37/–0.09 | ns, Min |
| CE input | $T_{CECK}/T_{CKCE}$ | 0.19/–0.06 | 0.21/–0.07 | 0.24/–0.08 | ns, Min |
| SR/BY inputs (synchronous) | $T_{SRCK}/T_{SCKR}$ | 0.21/–0.02 | 0.23/–0.03 | 0.26/–0.03 | ns, Min |
| **Clock CLK** | | | | | |
| Minimum Pulse Width, High | $T_{CH}$ | 0.61 | 0.67 | 0.77 | ns, Min |
| Minimum Pulse Width, Low | $T_{CL}$ | 0.61 | 0.67 | 0.77 | ns, Min |
| **Set/Reset** | | | | | |
| Minimum Pulse Width, SR/BY inputs (asynchronous) | $T_{RPW}$ | 0.61 | 0.67 | 0.77 | ns, Min |
| Delay from SR/BY inputs to XQ/YQ outputs (asynchronous) | $T_{RQ}$ | 1.06 | 1.17 | 1.34 | ns, Max |
| Toggle Frequency (MHz) (for export control) | $F_{TOG}$ | 820 | 750 | 650 | MHz |

| Date | Version | Revision |
|---|---|---|
| 03/01/05 (*cont'd*) | 3.4 (*cont'd*) | • Table 15, Table 17, Table 18, and Table 19: Restructured these I/O-related tables to include descriptions, as well as the actual IOSTANDARD attributes (used in Xilinx ISE™ software) for all I/O standards.<br>• Table 15: Added data for the following I/O standards: SSTL18_I, SSTL18_II, SSTL18_I_DCI, SSTL18_II_DCI, HSTL_I_18, HSTL_II_18, HSTL_III_18, HSTL_IV_18, LVDSEXT_25, LVDSEXT_33, BLVDS_25, LVDS_25_DCI, LVDS_33_DCI, LVDSEXT_25_DCI, LVDSEXT_33_DCI, HSLVDCI_15, HSLVDCI_18, HSLVDCI_25, HSLVDCI_33. Rearranged I/O standards in a more logical order.<br>• Table 16: Added parameter $T_{RPW}$ (Minimum Pulse Width, SR Input).<br>• Table 17: Added data for the following I/O standards: SSTL18_I, SSTL18_II, SSTL18_I_DCI, SSTL18_II_DCI, HSLVDCI_15, HSLVDCI_18, HSLVDCI_25, HSLVDCI_33. Changed "Csl" to "$C_{REF}$" to agree with Figure 1 and Table 19. Rearranged I/O standards in a more logical order.<br>• Table 18: Added data for the following I/O standards: SSTL18_I, SSTL18_II, HSTL_I_18, HSTL_II_18, HSTL_III_18, HSTL_IV_18. Added footnote defining equivalents for DCI standards.<br>• Table 19: Added Footnotes (2) and (3) to PCI/PCI-X capacitive load ($C_{REF}$) values. Added HSLVDCI callouts to LVDCI parameter rows (same values).<br>• Table 28: Added parameter $T_{BCCS}$, CLKA to CLKB Setup Time.<br>• Table 31: Added Footnote (1) indicating that $F_{CC\_SERIAL}$ should not exceed $F_{CC\_STARTUP}$ if no provision is made to adjust the speed of CCLK.<br>• Table 33: $T_{TCKTDO}$ corrected from a "Min" to a "Max" specification. |
| 11/05/07 | 3.5 | • Updated copyright notice and legal disclaimer. |

## Notice of Disclaimer

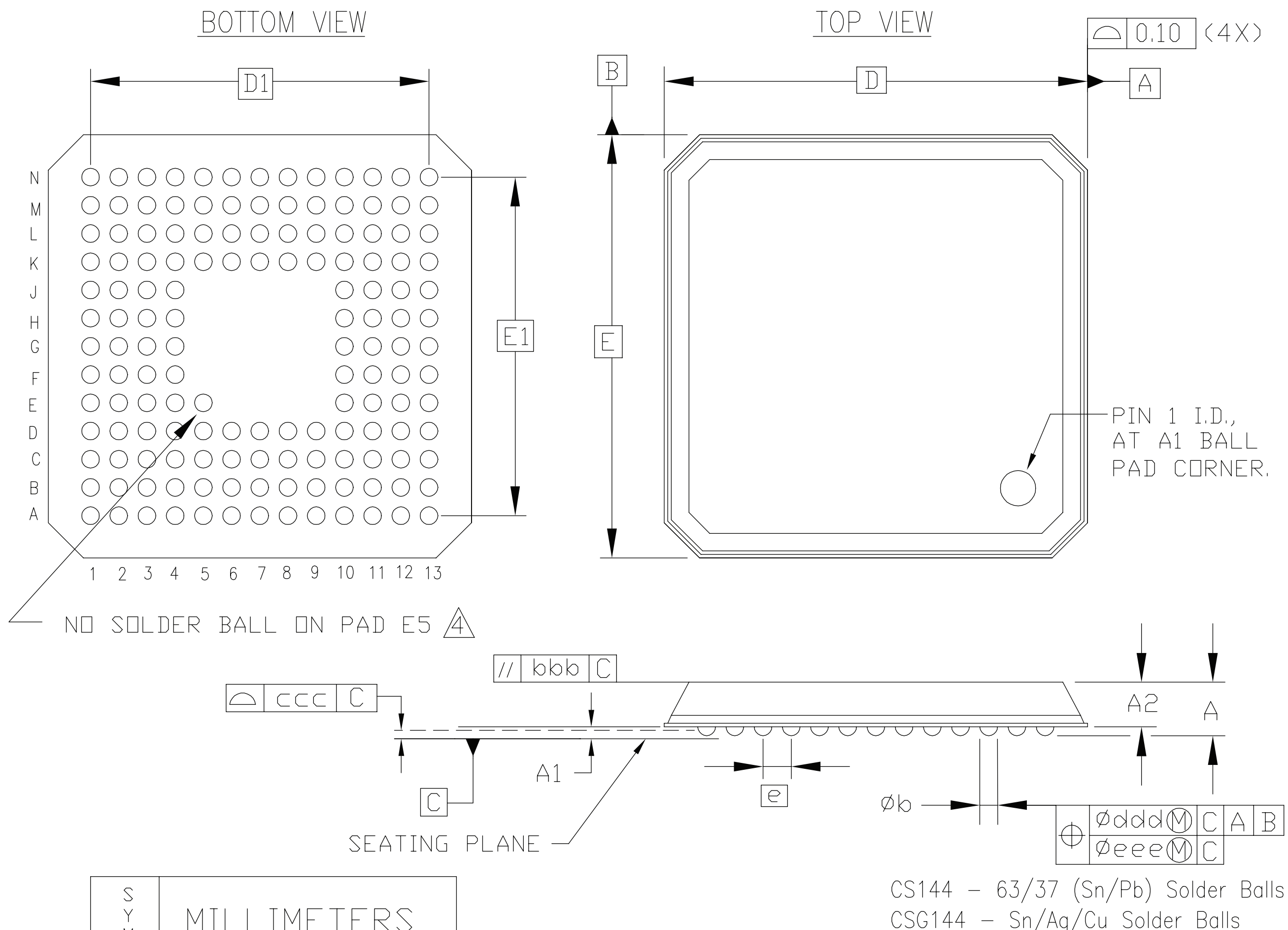


## Virtex-II Data Sheet

The Virtex-II Data Sheet contains the following modules:

- Virtex-II Platform FPGAs: Introduction and Overview (Module 1)
- Virtex-II Platform FPGAs: Functional Description (Module 2)
- Virtex-II Platform FPGAs: DC and Switching Characteristics (Module 3)
- Virtex-II Platform FPGAs: Pinout Information (Module 4)

## CS144/CSG144 Chip-Scale BGA Package Specifications (0.80mm pitch)




| SYMBOL | MILLIMETERS MIN. | NOM. | MAX. |
|---|---|---|---|
| A | – | – | 1.20 |
| $A_1$ | 0.20 | – | – |
| $A_2$ | 0.65 | – | – |
| D/E | 12.00 BSC | | |
| $D_1/E_1$ | 9.60 BSC | | |
| e | 0.80 BSC | | |
| Øb | 0.40 | 0.45 | 0.50 |
| bbb | – | – | 0.20 |
| ccc | – | – | 0.12 |
| ddd | – | – | 0.15 |
| eee | – | – | 0.08 |
| M | 13 | | |

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MO–216–BAG–2 (DEPOPULATED).
4. (4) PAD 'E5' IS FOR PAD 'A1' CORNER INDICATION.

144–BALL CHIP SCALE BGA (CS144/CSG144)

*Figure 1:* **CS144/CSG144 Chip-Scale BGA Package Specifications**

*Table 8:* **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

| Bank | Pin Description | Pin Number | No Connect in XC2V1500 | No Connect in XC2V2000 |
|---|---|---|---|---|
| NA | GND | R12 | | |
| NA | GND | R11 | | |
| NA | GND | R10 | | |
| NA | GND | P25 | | |
| NA | GND | P17 | | |
| NA | GND | P16 | | |
| NA | GND | P15 | | |
| NA | GND | P14 | | |
| NA | GND | P13 | | |
| NA | GND | P12 | | |
| NA | GND | P11 | | |
| NA | GND | P10 | | |
| NA | GND | P2 | | |
| NA | GND | N25 | | |
| NA | GND | N17 | | |
| NA | GND | N16 | | |
| NA | GND | N15 | | |
| NA | GND | N14 | | |
| NA | GND | N13 | | |
| NA | GND | N12 | | |
| NA | GND | N11 | | |
| NA | GND | N10 | | |
| NA | GND | N2 | | |
| NA | GND | M17 | | |
| NA | GND | M16 | | |
| NA | GND | M15 | | |
| NA | GND | M14 | | |
| NA | GND | M13 | | |
| NA | GND | M12 | | |
| NA | GND | M11 | | |
| NA | GND | M10 | | |
| NA | GND | L17 | | |
| NA | GND | L16 | | |
| NA | GND | L15 | | |
| NA | GND | L14 | | |
| NA | GND | L13 | | |
| NA | GND | L12 | | |

*Table 9:* **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

| Bank | Pin Description | Pin Number | No Connect in XC2V1000 | No Connect in XC2V1500 |
|---|---|---|---|---|
| 6 | IO_L91N_6 | P4 | | |
| 6 | IO_L93P_6 | N4 | | |
| 6 | IO_L93N_6/VREF_6 | N3 | | |
| 6 | IO_L94P_6 | N6 | | |
| 6 | IO_L94N_6 | N5 | | |
| 6 | IO_L96P_6 | N8 | | |
| 6 | IO_L96N_6 | N7 | | |
| | | | | |
| 7 | IO_L96P_7 | N2 | | |
| 7 | IO_L96N_7 | M1 | | |
| 7 | IO_L94P_7 | M2 | | |
| 7 | IO_L94N_7 | M3 | | |
| 7 | IO_L93P_7/VREF_7 | M4 | | |
| 7 | IO_L93N_7 | M5 | | |
| 7 | IO_L91P_7 | M6 | | |
| 7 | IO_L91N_7 | M7 | | |
| 7 | IO_L73P_7 | M8 | NC | NC |
| 7 | IO_L73N_7 | L8 | NC | NC |
| 7 | IO_L72P_7 | L1 | NC | |
| 7 | IO_L72N_7 | K1 | NC | |
| 7 | IO_L70P_7 | K2 | NC | |
| 7 | IO_L70N_7 | K3 | NC | |
| 7 | IO_L69P_7/VREF_7 | L3 | NC | |
| 7 | IO_L69N_7 | L4 | NC | |
| 7 | IO_L67P_7 | L5 | NC | |
| 7 | IO_L67N_7 | L7 | NC | |
| 7 | IO_L54P_7 | J1 | | |
| 7 | IO_L54N_7 | H1 | | |
| 7 | IO_L52P_7 | J2 | | |
| 7 | IO_L52N_7 | J3 | | |
| 7 | IO_L51P_7/VREF_7 | J4 | | |
| 7 | IO_L51N_7 | J5 | | |
| 7 | IO_L49P_7 | K5 | | |
| 7 | IO_L49N_7 | K6 | | |
| 7 | IO_L48P_7 | F1 | | |
| 7 | IO_L48N_7 | F2 | | |

*Table 10:* **BG728 BGA — XC2V3000**

| Bank | Pin Description | Pin Number |
|---|---|---|
| 1 | VCCO_1 | G16 |
| 1 | VCCO_1 | D21 |
| 1 | VCCO_1 | C16 |
| 2 | VCCO_2 | N18 |
| 2 | VCCO_2 | M25 |
| 2 | VCCO_2 | M21 |
| 2 | VCCO_2 | M18 |
| 2 | VCCO_2 | L19 |
| 2 | VCCO_2 | L18 |
| 2 | VCCO_2 | K19 |
| 2 | VCCO_2 | G24 |
| 3 | VCCO_3 | AA24 |
| 3 | VCCO_3 | V19 |
| 3 | VCCO_3 | U19 |
| 3 | VCCO_3 | U18 |
| 3 | VCCO_3 | T25 |
| 3 | VCCO_3 | T21 |
| 3 | VCCO_3 | T18 |
| 3 | VCCO_3 | R18 |
| 4 | VCCO_4 | AE16 |
| 4 | VCCO_4 | AD21 |
| 4 | VCCO_4 | AA16 |
| 4 | VCCO_4 | W18 |
| 4 | VCCO_4 | W17 |
| 4 | VCCO_4 | V17 |
| 4 | VCCO_4 | V16 |
| 4 | VCCO_4 | V15 |
| 5 | VCCO_5 | AE12 |
| 5 | VCCO_5 | AD7 |
| 5 | VCCO_5 | AA12 |
| 5 | VCCO_5 | W11 |
| 5 | VCCO_5 | W10 |
| 5 | VCCO_5 | V13 |
| 5 | VCCO_5 | V12 |
| 5 | VCCO_5 | V11 |
| 6 | VCCO_6 | AA4 |

## FF896 Flip-Chip Fine-Pitch BGA Package

As shown in Table 11, XC2V1000, XC2V1500, and XC2V2000 Virtex-II devices are available in the FF896 flip-chip fine-pitch BGA package. Pins in the XC2V1000, XC2V1500, and XC2V2000 devices are the same, except for the pin differences in the XC2V1000 and XC2V1500 devices shown in the No Connect columns. Following this table are the FF896 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch).

*Table 11:* **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

| Bank | Pin Description | Pin Number | No Connect in the XC2V1000 | No Connect in the XC2V1500 |
|---|---|---|---|---|
| 0 | IO_L01N_0 | B27 | | |
| 0 | IO_L01P_0 | A27 | | |
| 0 | IO_L02N_0 | F24 | | |
| 0 | IO_L02P_0 | E24 | | |
| 0 | IO_L03N_0/VRP_0 | C26 | | |
| 0 | IO_L03P_0/VRN_0 | C25 | | |
| 0 | IO_L04N_0/VREF_0 | A26 | | |
| 0 | IO_L04P_0 | A25 | | |
| 0 | IO_L05N_0 | F23 | | |
| 0 | IO_L05P_0 | F22 | | |
| 0 | IO_L06N_0 | C24 | | |
| 0 | IO_L06P_0 | D25 | | |
| 0 | IO_L19N_0 | A24 | | |
| 0 | IO_L19P_0 | B25 | | |
| 0 | IO_L20N_0 | G22 | | |
| 0 | IO_L20P_0 | G21 | | |
| 0 | IO_L21N_0 | D24 | | |
| 0 | IO_L21P_0/VREF_0 | D23 | | |
| 0 | IO_L22N_0 | B23 | | |
| 0 | IO_L22P_0 | B24 | | |
| 0 | IO_L23N_0 | H21 | | |
| 0 | IO_L23P_0 | H20 | | |
| 0 | IO_L24N_0 | E22 | | |
| 0 | IO_L24P_0 | E23 | | |
| 0 | IO_L49N_0 | A22 | | |
| 0 | IO_L49P_0 | B22 | | |
| 0 | IO_L50N_0 | F21 | | |
| 0 | IO_L50P_0 | F20 | | |
| 0 | IO_L51N_0 | C23 | | |
| 0 | IO_L51P_0/VREF_0 | C22 | | |
| 0 | IO_L52N_0 | B20 | | |
| 0 | IO_L52P_0 | B21 | | |

*Table 11:* **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

| Bank | Pin Description | Pin Number | No Connect in the XC2V1000 | No Connect in the XC2V1500 |
|---|---|---|---|---|
| 7 | IO_L52P_7 | J29 | | |
| 7 | IO_L52N_7 | K29 | | |
| 7 | IO_L51P_7/VREF_7 | K27 | | |
| 7 | IO_L51N_7 | J27 | | |
| 7 | IO_L50P_7 | L24 | | |
| 7 | IO_L50N_7 | K24 | | |
| 7 | IO_L49P_7 | H27 | | |
| 7 | IO_L49N_7 | J28 | | |
| 7 | IO_L48P_7 | H26 | | |
| 7 | IO_L48N_7 | J26 | | |
| 7 | IO_L47P_7 | K25 | | |
| 7 | IO_L47N_7 | J25 | | |
| 7 | IO_L46P_7 | H28 | | |
| 7 | IO_L46N_7 | H29 | | |
| 7 | IO_L45P_7/VREF_7 | G28 | | |
| 7 | IO_L45N_7 | F28 | | |
| 7 | IO_L44P_7 | L23 | | |
| 7 | IO_L44N_7 | K23 | | |
| 7 | IO_L43P_7 | F30 | | |
| 7 | IO_L43N_7 | G30 | | |
| 7 | IO_L24P_7 | F26 | | |
| 7 | IO_L24N_7 | G27 | | |
| 7 | IO_L23P_7 | J24 | | |
| 7 | IO_L23N_7 | H24 | | |
| 7 | IO_L22P_7 | F29 | | |
| 7 | IO_L22N_7 | G29 | | |
| 7 | IO_L21P_7/VREF_7 | G26 | | |
| 7 | IO_L21N_7 | G25 | | |
| 7 | IO_L20P_7 | H25 | | |
| 7 | IO_L20N_7 | G24 | | |
| 7 | IO_L19P_7 | D30 | | |
| 7 | IO_L19N_7 | E30 | | |
| 7 | IO_L06P_7 | E27 | | |
| 7 | IO_L06N_7 | F27 | | |
| 7 | IO_L05P_7 | J23 | | |
| 7 | IO_L05N_7 | H22 | | |
| 7 | IO_L04P_7 | C29 | | |

*Table 12:* **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

| Bank | Pin Description | Pin Number | No Connect in the XC2V3000 |
|---|---|---|---|
| 1 | IO_L22P_1 | A5 | |
| 1 | IO_L21N_1/VREF_1 | F10 | |
| 1 | IO_L21P_1 | G9 | |
| 1 | IO_L20N_1 | J12 | |
| 1 | IO_L20P_1 | J11 | |
| 1 | IO_L19N_1 | B4 | |
| 1 | IO_L19P_1 | B5 | |
| 1 | IO_L06N_1 | D6 | |
| 1 | IO_L06P_1 | C6 | |
| 1 | IO_L05N_1 | H11 | |
| 1 | IO_L05P_1 | J10 | |
| 1 | IO_L04N_1 | D8 | |
| 1 | IO_L04P_1/VREF_1 | E7 | |
| 1 | IO_L03N_1/VRP_1 | F9 | |
| 1 | IO_L03P_1/VRN_1 | F8 | |
| 1 | IO_L02N_1 | H10 | |
| 1 | IO_L02P_1 | H9 | |
| 1 | IO_L01N_1 | C2 | |
| 1 | IO_L01P_1 | B3 | |
| | | | |
| 2 | IO_L01N_2 | E2 | |
| 2 | IO_L01P_2 | D2 | |
| 2 | IO_L02N_2/VRP_2 | K11 | |
| 2 | IO_L02P_2/VRN_2 | K10 | |
| 2 | IO_L03N_2 | F5 | |
| 2 | IO_L03P_2/VREF_2 | G5 | |
| 2 | IO_L04N_2 | E3 | |
| 2 | IO_L04P_2 | D3 | |
| 2 | IO_L05N_2 | J9 | |
| 2 | IO_L05P_2 | K9 | |
| 2 | IO_L06N_2 | F4 | |
| 2 | IO_L06P_2 | E4 | |
| 2 | IO_L19N_2 | E1 | |
| 2 | IO_L19P_2 | D1 | |
| 2 | IO_L20N_2 | J8 | |
| 2 | IO_L20P_2 | K8 | |

*Table 12:* **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

| Bank | Pin Description | Pin Number | No Connect in the XC2V3000 |
|---|---|---|---|
| 2 | IO_L21N_2 | H7 | |
| 2 | IO_L21P_2/VREF_2 | J7 | |
| 2 | IO_L22N_2 | H6 | |
| 2 | IO_L22P_2 | G6 | |
| 2 | IO_L23N_2 | L10 | |
| 2 | IO_L23P_2 | L9 | |
| 2 | IO_L24N_2 | G3 | |
| 2 | IO_L24P_2 | F3 | |
| 2 | IO_L25N_2 | G2 | |
| 2 | IO_L25P_2 | F2 | |
| 2 | IO_L26N_2 | M10 | |
| 2 | IO_L26P_2 | N10 | |
| 2 | IO_L27N_2 | J6 | |
| 2 | IO_L27P_2/VREF_2 | K6 | |
| 2 | IO_L28N_2 | J5 | |
| 2 | IO_L28P_2 | H5 | |
| 2 | IO_L29N_2 | L7 | |
| 2 | IO_L29P_2 | K7 | |
| 2 | IO_L30N_2 | J4 | |
| 2 | IO_L30P_2 | H4 | |
| 2 | IO_L43N_2 | G1 | |
| 2 | IO_L43P_2 | F1 | |
| 2 | IO_L44N_2 | L8 | |
| 2 | IO_L44P_2 | M8 | |
| 2 | IO_L45N_2 | J1 | |
| 2 | IO_L45P_2/VREF_2 | H2 | |
| 2 | IO_L46N_2 | J3 | |
| 2 | IO_L46P_2 | H3 | |
| 2 | IO_L47N_2 | M9 | |
| 2 | IO_L47P_2 | N9 | |
| 2 | IO_L48N_2 | L5 | |
| 2 | IO_L48P_2 | K5 | |
| 2 | IO_L49N_2 | K2 | |
| 2 | IO_L49P_2 | J2 | |
| 2 | IO_L50N_2 | N7 | |
| 2 | IO_L50P_2 | M7 | |

*Table 12:* **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

| Bank | Pin Description | Pin Number | No Connect in the XC2V3000 |
|---|---|---|---|
| NA | VCCINT | AB17 | |
| NA | VCCINT | AB16 | |
| NA | VCCINT | AB15 | |
| NA | VCCINT | AB14 | |
| NA | VCCINT | AB13 | |
| NA | VCCINT | AA22 | |
| NA | VCCINT | AA13 | |
| NA | VCCINT | Y22 | |
| NA | VCCINT | Y13 | |
| NA | VCCINT | W22 | |
| NA | VCCINT | W13 | |
| NA | VCCINT | V22 | |
| NA | VCCINT | V13 | |
| NA | VCCINT | U22 | |
| NA | VCCINT | U13 | |
| NA | VCCINT | T22 | |
| NA | VCCINT | T13 | |
| NA | VCCINT | R22 | |
| NA | VCCINT | R13 | |
| NA | VCCINT | P22 | |
| NA | VCCINT | P13 | |
| NA | VCCINT | N22 | |
| NA | VCCINT | N21 | |
| NA | VCCINT | N20 | |
| NA | VCCINT | N19 | |
| NA | VCCINT | N18 | |
| NA | VCCINT | N17 | |
| NA | VCCINT | N16 | |
| NA | VCCINT | N15 | |
| NA | VCCINT | N14 | |
| NA | VCCINT | N13 | |
| NA | VCCINT | M23 | |
| NA | VCCINT | M12 | |
| NA | VCCINT | L24 | |
| NA | VCCINT | L11 | |
| | | | |

*Table 13:* **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

| Bank | Pin Description | Pin Number | No Connect in the XC2V4000 | No Connect in the XC2V6000 |
|---|---|---|---|---|
| 7 | IO_L02P_7/VRN_7 | M27 | | |
| 7 | IO_L02N_7/VRP_7 | L27 | | |
| 7 | IO_L01P_7 | D38 | | |
| 7 | IO_L01N_7 | E37 | | |
| | | | | |
| 0 | VCCO_0 | P25 | | |
| 0 | VCCO_0 | P24 | | |
| 0 | VCCO_0 | P23 | | |
| 0 | VCCO_0 | P22 | | |
| 0 | VCCO_0 | P21 | | |
| 0 | VCCO_0 | N26 | | |
| 0 | VCCO_0 | N25 | | |
| 0 | VCCO_0 | N24 | | |
| 0 | VCCO_0 | N23 | | |
| 0 | VCCO_0 | N22 | | |
| 0 | VCCO_0 | N21 | | |
| 0 | VCCO_0 | L23 | | |
| 0 | VCCO_0 | J25 | | |
| 0 | VCCO_0 | G27 | | |
| 0 | VCCO_0 | E29 | | |
| 0 | VCCO_0 | C22 | | |
| 0 | VCCO_0 | B26 | | |
| 1 | VCCO_1 | P19 | | |
| 1 | VCCO_1 | P18 | | |
| 1 | VCCO_1 | P17 | | |
| 1 | VCCO_1 | P16 | | |
| 1 | VCCO_1 | P15 | | |
| 1 | VCCO_1 | N19 | | |
| 1 | VCCO_1 | N18 | | |
| 1 | VCCO_1 | N17 | | |
| 1 | VCCO_1 | N16 | | |
| 1 | VCCO_1 | N15 | | |
| 1 | VCCO_1 | N14 | | |
| 1 | VCCO_1 | L17 | | |
| 1 | VCCO_1 | J15 | | |
| 1 | VCCO_1 | G13 | | |

*Table 14:* **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

| Bank | Pin Description | Pin Number | No Connect in XC2V2000 |
|---|---|---|---|
| 0 | IO_L92N_0 | F17 | |
| 0 | IO_L92P_0 | F16 | |
| 0 | IO_L93N_0 | B18 | |
| 0 | IO_L93P_0 | B17 | |
| 0 | IO_L94N_0/VREF_0 | J17 | |
| 0 | IO_L94P_0 | J16 | |
| 0 | IO_L95N_0/GCLK7P | E17 | |
| 0 | IO_L95P_0/GCLK6S | E16 | |
| 0 | IO_L96N_0/GCLK5P | A18 | |
| 0 | IO_L96P_0/GCLK4S | A17 | |
| | | | |
| 1 | IO_L96N_1/GCLK3P | C16 | |
| 1 | IO_L96P_1/GCLK2S | C15 | |
| 1 | IO_L95N_1/GCLK1P | H16 | |
| 1 | IO_L95P_1/GCLK0S | H15 | |
| 1 | IO_L94N_1 | A15 | |
| 1 | IO_L94P_1/VREF_1 | A14 | |
| 1 | IO_L93N_1 | F15 | |
| 1 | IO_L93P_1 | F14 | |
| 1 | IO_L92N_1 | G15 | |
| 1 | IO_L92P_1 | G14 | |
| 1 | IO_L91N_1 | B15 | |
| 1 | IO_L91P_1/VREF_1 | B14 | |
| 1 | IO_L78N_1 | D15 | |
| 1 | IO_L78P_1 | E15 | |
| 1 | IO_L77N_1 | J15 | |
| 1 | IO_L77P_1 | K14 | |
| 1 | IO_L76N_1 | D14 | |
| 1 | IO_L76P_1 | D13 | |
| 1 | IO_L75N_1/VREF_1 | E14 | |
| 1 | IO_L75P_1 | E13 | |
| 1 | IO_L74N_1 | A13 | |
| 1 | IO_L74P_1 | A12 | |
| 1 | IO_L73N_1 | F13 | |
| 1 | IO_L73P_1 | F12 | |
| 1 | IO_L72N_1 | J14 | |
| 1 | IO_L72P_1 | J13 | |
| 1 | IO_L71N_1 | B13 | |