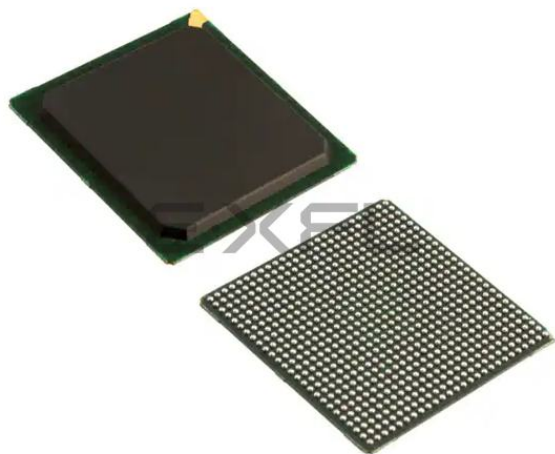




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	3584
Number of Logic Elements/Cells	-
Total RAM Bits	1769472
Number of I/O	484
Number of Gates	3000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v3000-4fgg676i

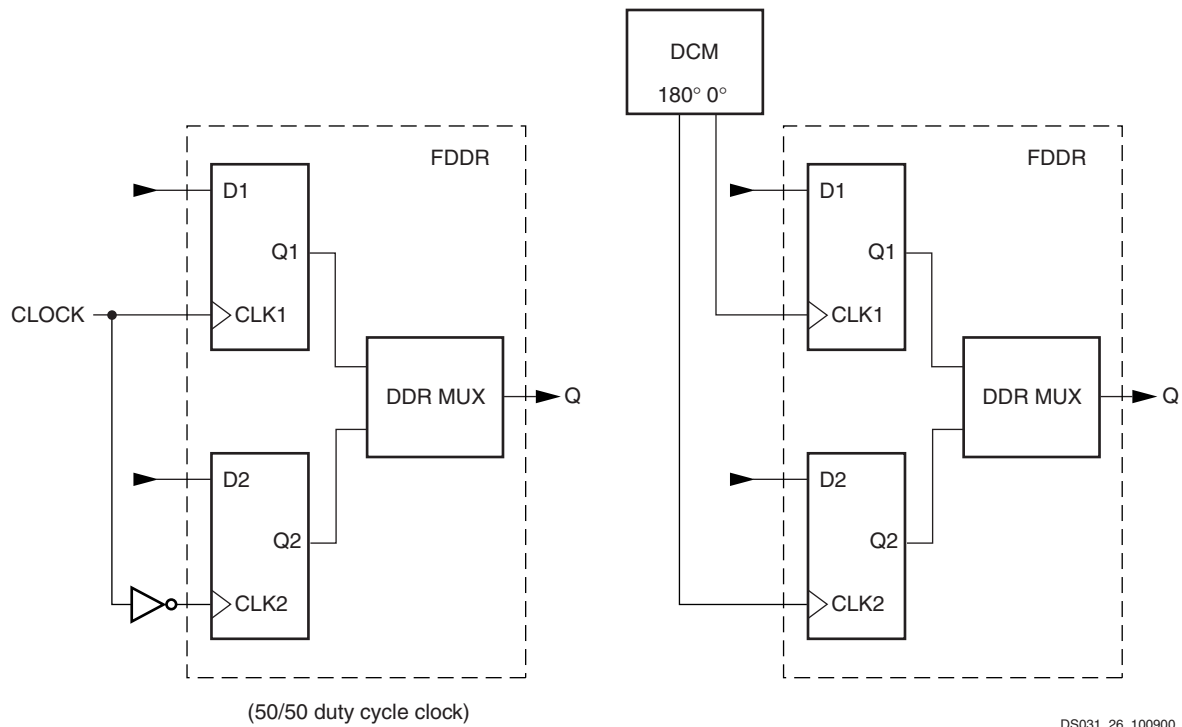


Figure 3: Double Data Rate Registers

The DDR mechanism shown in Figure 3 can be used to mirror a copy of the clock on the output. This is useful for propagating a clock along the data that has an identical delay. It is also useful for multiple clock generation, where there is a unique clock driver for every clock load. Virtex-II devices can produce many copies of a clock with very little skew.

Each group of two registers has a clock enable signal (ICE for the input registers, OCE for the output registers, and TCE for the 3-state registers). The clock enable signals are active High by default. If left unconnected, the clock enable for that storage element defaults to the active state.

Each IOB block has common synchronous or asynchronous set and reset (SR and REV signals).

SR forces the storage element into the state specified by the SRHIGH or SRLOW attribute. SRHIGH forces a logic "1". SRLOW forces a logic "0". When SR is used, a second input (REV) forces the storage element into the opposite state. The reset condition predominates over the set condition. The initial state after configuration or global initialization state is defined by a separate INIT0 and INIT1 attribute. By default, the SRLOW attribute forces INIT0, and the SRHIGH attribute forces INIT1.

For each storage element, the SRHIGH, SRLOW, INIT0, and INIT1 attributes are independent. Synchronous or asynchronous set / reset is consistent in an IOB block.

All the control signals have independent polarity. Any inverter placed on a control input is automatically absorbed.

Each register or latch (independent of all other registers or latches) (see Figure 4) can be configured as follows:

- No set or reset
- Synchronous set
- Synchronous reset
- Synchronous set and reset
- Asynchronous set (preset)
- Asynchronous reset (clear)
- Asynchronous set and reset (preset and clear)

The synchronous reset overrides a set, and an asynchronous clear overrides a preset.

IOB Input Switching Characteristics Standard Adjustments

Table 15 gives all standard-specific data input delay adjustments.

Table 15: IOB Input Switching Characteristics Standard Adjustments

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-6	-5	-4	
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL	T_{ILVTTL}	0.00	0.00	0.00	ns
LVC MOS (Low-Voltage CMOS), 3.3V	LVC MOS33	$T_{ILVCMOS33}$	0.00	0.00	0.00	ns
LVC MOS, 2.5V	LVC MOS25	$T_{ILVCMOS25}$	0.11	0.11	0.12	ns
LVC MOS, 1.8V	LVC MOS18	$T_{ILVCMOS18}$	0.42	0.43	0.49	ns
LVC MOS, 1.5V	LVC MOS15	$T_{ILVCMOS15}$	0.98	1.00	1.15	ns
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	T_{ILVDS_25}	0.60	0.60	0.69	ns
LVDS, 3.3V	LVDS_33	T_{ILVDS_33}	0.60	0.60	0.69	ns
LVDSEXT (Extended Mode), 2.5V	LVDSEXT_25	$T_{ILVDSEXT_25}$	0.68	0.69	0.79	ns
LVDSEXT, 3.3V	LVDSEXT_33	$T_{ILVDSEXT_33}$	0.56	0.56	0.65	ns
ULVDS (Ultra LVDS), 2.5V	ULVDS_25	T_{IULVDS_25}	0.48	0.49	0.56	ns
BLVDS (Bus LVDS), 2.5V	BLVDS_25	T_{IBLVDS_25}	0.68	0.69	0.79	ns
LDT (HyperTransport), 2.5V	LDT_25	$T_{ILD T_25}$	0.48	0.49	0.56	ns
LVPECL (Low-Voltage Positive Electron-Coupled Logic), 3.3V	LVPECL_33	$T_{ILVPECL_33}$	0.60	0.60	0.69	ns
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3	T_{IPCI33_3}	0.00	0.00	0.00	ns
PCI, 66 MHz, 3.3V	PCI66_3	T_{IPCI66_3}	0.00	0.00	0.00	ns
PCI-X, 133 MHz, 3.3V	PCIX	$T_{IPCI X}$	0.00	0.00	0.00	ns
GTL (Gunning Transceiver Logic)	GTL	T_{IGTL}	0.42	0.42	0.48	ns
GTL Plus	GTLP	T_{IGTLP}	0.42	0.42	0.48	ns
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	T_{IHSTL_I}	0.42	0.42	0.48	ns
HSTL, Class II	HSTL_II	T_{IHSTL_II}	0.42	0.42	0.48	ns
HSTL, Class III	HSTL_III	T_{IHSTL_III}	0.42	0.42	0.48	ns
HSTL, Class IV	HSTL_IV	T_{IHSTL_IV}	0.42	0.42	0.48	ns
HSTL, Class I, 1.8V	HSTL_I_18	$T_{IHSTL_I_18}$	0.42	0.42	0.48	ns
HSTL, Class II, 1.8V	HSTL_II_18	$T_{IHSTL_II_18}$	0.42	0.42	0.48	ns
HSTL, Class III, 1.8V	HSTL_III_18	$T_{IHSTL_III_18}$	0.42	0.42	0.48	ns
HSTL, Class IV, 1.8V	HSTL_IV_18	$T_{IHSTL_IV_18}$	0.42	0.42	0.48	ns
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	$T_{ISSTL18_I}$	0.42	0.42	0.48	ns
SSTL, Class II, 1.8V	SSTL18_II	$T_{ISSTL18_II}$	0.42	0.42	0.48	ns
SSTL, Class I, 2.5V	SSTL2_I	T_{ISSTL2_I}	0.42	0.42	0.48	ns
SSTL, Class II, 2.5V	SSTL2_II	T_{ISSTL2_II}	0.42	0.42	0.48	ns
SSTL, Class I, 3.3V	SSTL3_I	T_{ISSTL3_I}	0.35	0.35	0.40	ns
SSTL, Class II, 3.3V	SSTL3_II	T_{ISSTL3_II}	0.35	0.35	0.40	ns
AGP-2X/AGP (Accelerated Graphics Port)	AGP	T_{IAGP}	0.35	0.35	0.40	ns
LVDCI (Low-Voltage Digitally Controlled Impedance), 3.3V	LVDCI_33	T_{ILVDCI_33}	0.00	0.00	0.00	ns
LVDCI, 2.5V	LVDCI_25	T_{ILVDCI_25}	0.11	0.11	0.12	ns
LVDCI, 1.8V	LVDCI_18	T_{ILVDCI_18}	0.42	0.43	0.49	ns
LVDCI, 1.5V	LVDCI_15	T_{ILVDCI_15}	0.98	1.00	1.14	ns

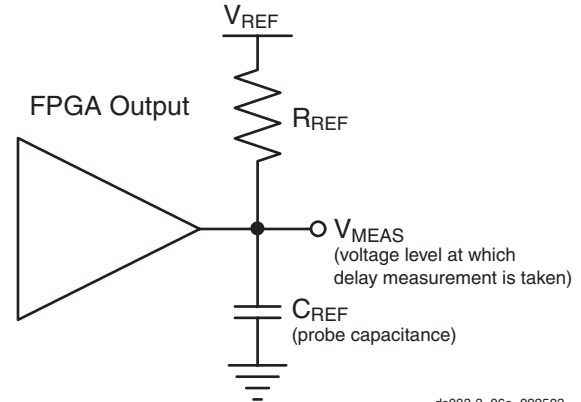
Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. (See [Virtex-II Platform FPGA User Guide](#) for details.) The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setup shown in [Figure 1](#).

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. (IBIS models can be found on the web at http://support.xilinx.com/support/sw_ibis.htm.) Parameters V_{REF} , R_{REF} , C_{REF} , and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from [Table 19](#).
2. Record the time to V_{MEAS} .
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.

4. Record the time to V_{MEAS} .
5. Compare the results of steps 2 and 4. The increase or decrease in delay should be added to or subtracted from the I/O Output Standard Adjustment value ([Table 17](#)) to yield the actual worst-case propagation delay (clock-to-input) of the PCB trace.



ds083-3_06a_092503

Figure 1: Generalized Test Setup

Table 19: Output Delay Measurement Methodology

Description	IOSTANDARD Attribute	R_{REF} (Ω)	$C_{REF}^{(1)}$ (pF)	V_{MEAS} (V)	V_{REF} (V)
LVTTTL (Low-Voltage Transistor-Transistor Logic)	LVTTTL (all)	1M	0	1.4	0
LVC MOS (Low-Voltage CMOS), 3.3V	LVC MOS33	1M	0	1.65	0
LVC MOS, 2.5V	LVC MOS25	1M	0	1.25	0
LVC MOS, 1.8V	LVC MOS18	1M	0	0.9	0
LVC MOS, 1.5V	LVC MOS15	1M	0	0.75	0
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3 (rising edge)	25	$10^{(2)}$	0.94	0
	PCI33_3 (falling edge)	25	$10^{(2)}$	2.03	3.3
PCI, 66 MHz, 3.3V	PCI66_3 (rising edge)	25	$10^{(2)}$	0.94	0
	PCI66_3 (falling edge)	25	$10^{(2)}$	2.03	3.3
PCI-X, 133 MHz, 3.3V	PCIX (rising edge)	25	$10^{(3)}$	0.94	
	PCIX (falling edge)	25	$10^{(3)}$	2.03	3.3
GTL (Gunning Transceiver Logic)	GTL	25	0	0.8	1.2
GTL Plus	GTLP	25	0	1.0	1.5
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class III	HSTL_III	50	0	0.9	1.5
HSTL, Class IV	HSTL_IV	25	0	0.9	1.5
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSTL, Class III, 1.8V	HSTL_III_18	50	0	1.1	1.8
HSTL, Class IV, 1.8V	HSTL_IV_18	25	0	1.1	1.8

Table 25: Pipelined Multiplier Switching Characteristics

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Setup and Hold Times Before/After Clock					
Data Inputs	T _{MULIDCK} /T _{MULCKID}	3.00/ 0.00	3.45/ 0.00	3.89/ 0.00	ns, Max
Clock Enable	T _{MULIDCK_CE} /T _{MULCKID_CE}	0.72/ 0.00	0.80/ 0.00	0.86/ 0.00	ns, Max
Reset	T _{MULIDCK_RST} /T _{MULCKID_RST}	0.72/ 0.00	0.80/ 0.00	0.86/ 0.00	ns, Max
Clock to Output Pin					
Clock to Pin 35	T _{MULTCK_P35}	3.05	6.91	8.12	ns, Max
Clock to Pin 34	T _{MULTCK_P34}	2.95	6.75	7.93	ns, Max
Clock to Pin 33	T _{MULTCK_P33}	2.85	6.59	7.74	ns, Max
Clock to Pin 32	T _{MULTCK_P32}	2.76	6.43	7.56	ns, Max
Clock to Pin 31	T _{MULTCK_P31}	2.66	6.27	7.37	ns, Max
Clock to Pin 30	T _{MULTCK_P30}	2.56	6.11	7.19	ns, Max
Clock to Pin 29	T _{MULTCK_P29}	2.47	5.95	7.00	ns, Max
Clock to Pin 28	T _{MULTCK_P28}	2.37	5.79	6.81	ns, Max
Clock to Pin 27	T _{MULTCK_P27}	2.27	5.63	6.63	ns, Max
Clock to Pin 26	T _{MULTCK_P26}	2.17	5.47	6.44	ns, Max
Clock to Pin 25	T _{MULTCK_P25}	2.08	5.31	6.26	ns, Max
Clock to Pin 24	T _{MULTCK_P24}	1.98	5.15	6.07	ns, Max
Clock to Pin 23	T _{MULTCK_P23}	1.88	4.99	5.88	ns, Max
Clock to Pin 22	T _{MULTCK_P22}	1.79	4.83	5.70	ns, Max
Clock to Pin 21	T _{MULTCK_P21}	1.69	4.67	5.51	ns, Max
Clock to Pin 20	T _{MULTCK_P20}	1.59	4.51	5.33	ns, Max
Clock to Pin 19	T _{MULTCK_P19}	1.50	4.35	5.14	ns, Max
Clock to Pin 18	T _{MULTCK_P18}	1.40	4.19	4.95	ns, Max
Clock to Pin 17	T _{MULTCK_P17}	1.30	4.03	4.77	ns, Max
Clock to Pin 16	T _{MULTCK_P16}	1.20	3.87	4.58	ns, Max
Clock to Pin 15	T _{MULTCK_P15}	1.11	3.71	4.40	ns, Max
Clock to Pin 14	T _{MULTCK_P14}	1.01	3.55	4.21	ns, Max
Clock to Pin 13	T _{MULTCK_P13}	0.91	3.39	4.02	ns, Max
Clock to Pin 12	T _{MULTCK_P12}	0.91	3.23	3.84	ns, Max
Clock to Pin 11	T _{MULTCK_P11}	0.91	3.07	3.65	ns, Max
Clock to Pin 10	T _{MULTCK_P10}	0.91	2.91	3.47	ns, Max
Clock to Pin 9	T _{MULTCK_P9}	0.91	2.75	3.28	ns, Max
Clock to Pin 8	T _{MULTCK_P8}	0.91	2.59	3.09	ns, Max
Clock to Pin 7	T _{MULTCK_P7}	0.91	2.43	2.91	ns, Max
Clock to Pin 6	T _{MULTCK_P6}	0.91	2.27	2.72	ns, Max
Clock to Pin 5	T _{MULTCK_P5}	0.91	2.11	2.54	ns, Max
Clock to Pin 4	T _{MULTCK_P4}	0.91	1.95	2.35	ns, Max
Clock to Pin 3	T _{MULTCK_P3}	0.91	1.79	2.16	ns, Max
Clock to Pin 2	T _{MULTCK_P2}	0.91	1.63	1.98	ns, Max
Clock to Pin 1	T _{MULTCK_P1}	0.91	1.47	1.79	ns, Max
Clock to Pin 0	T _{MULTCK_P0}	0.91	1.31	1.61	ns, Max

Table 7: FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
4	IO_L02N_4/D0/DIN ⁽¹⁾	V18		
4	IO_L02P_4/D1	V17		
4	IO_L03N_4/D2/ALT_VRP_4	W18		
4	IO_L03P_4/D3/ALT_VRN_4	Y18		
4	IO_L04N_4/VREF_4	AA18		
4	IO_L04P_4	AB18		
4	IO_L05N_4/VRP_4	W17		
4	IO_L05P_4/VRN_4	Y17		
4	IO_L06N_4	AA17		
4	IO_L06P_4	AB17		
4	IO_L19N_4	V16	NC	NC
4	IO_L19P_4	V15	NC	NC
4	IO_L21N_4	W16	NC	NC
4	IO_L21P_4/VREF_4	Y16	NC	NC
4	IO_L22N_4	AA16	NC	NC
4	IO_L22P_4	AB16	NC	NC
4	IO_L24N_4	W15	NC	NC
4	IO_L24P_4	Y15	NC	NC
4	IO_L49N_4	AA15	NC	
4	IO_L49P_4	AB15	NC	
4	IO_L51N_4	U14	NC	
4	IO_L51P_4/VREF_4	V14	NC	
4	IO_L52N_4	W14	NC	
4	IO_L52P_4	Y14	NC	
4	IO_L54N_4	AA14	NC	
4	IO_L54P_4	AB14	NC	
4	IO_L91N_4/VREF_4	U13		
4	IO_L91P_4	V13		
4	IO_L92N_4	W13		
4	IO_L92P_4	Y13		
4	IO_L93N_4	AA13		
4	IO_L93P_4	AB13		
4	IO_L94N_4/VREF_4	U12		
4	IO_L94P_4	V12		

Table 7: FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
6	IO_L46P_6	R2		
6	IO_L46N_6	R1		
6	IO_L48P_6	P6		
6	IO_L48N_6	P5		
6	IO_L49P_6	P4	NC	
6	IO_L49N_6	P3	NC	
6	IO_L51P_6	P2	NC	
6	IO_L51N_6/VREF_6	P1	NC	
6	IO_L52P_6	N6	NC	
6	IO_L52N_6	N5	NC	
6	IO_L54P_6	N4	NC	
6	IO_L54N_6	N3	NC	
6	IO_L91P_6	N2		
6	IO_L91N_6	N1		
6	IO_L93P_6	M6		
6	IO_L93N_6/VREF_6	M5		
6	IO_L94P_6	M4		
6	IO_L94N_6	M3		
6	IO_L96P_6	M2		
6	IO_L96N_6	M1		
7	IO_L96P_7	L2		
7	IO_L96N_7	L3		
7	IO_L94P_7	L4		
7	IO_L94N_7	L5		
7	IO_L93P_7/VREF_7	K1		
7	IO_L93N_7	K2		
7	IO_L91P_7	K3		
7	IO_L91N_7	K4		
7	IO_L54P_7	L6	NC	
7	IO_L54N_7	K6	NC	
7	IO_L52P_7	K5	NC	
7	IO_L52N_7	J5	NC	
7	IO_L51P_7/VREF_7	J1	NC	

Table 8: FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
4	IO_L06P_4	Y21		
4	IO_L19N_4	AE24		
4	IO_L19P_4	AF24		
4	IO_L21N_4	AE23		
4	IO_L21P_4/VREF_4	AF23		
4	IO_L22N_4	AE22		
4	IO_L22P_4	AF22		
4	IO_L24N_4	AF21		
4	IO_L24P_4	AF20		
4	IO_L25N_4	AA19	NC	NC
4	IO_L25P_4	AB19	NC	NC
4	IO_L27N_4	AD20	NC	NC
4	IO_L27P_4/VREF_4	AC20	NC	NC
4	IO_L28N_4	AC19	NC	NC
4	IO_L28P_4	AD19	NC	NC
4	IO_L49N_4	AE19		
4	IO_L49P_4	AF19		
4	IO_L51N_4	AA18		
4	IO_L51P_4/VREF_4	AB18		
4	IO_L52N_4	Y18		
4	IO_L52P_4	Y17		
4	IO_L54N_4	AC18		
4	IO_L54P_4	AD18		
4	IO_L67N_4	AE18		
4	IO_L67P_4	AF18		
4	IO_L69N_4	AA17		
4	IO_L69P_4/VREF_4	AB17		
4	IO_L70N_4	AC17		
4	IO_L70P_4	AD17		
4	IO_L72N_4	AF17		
4	IO_L72P_4	AF16		
4	IO_L73N_4	AB16	NC	
4	IO_L73P_4	AC16	NC	
4	IO_L75N_4	AA16	NC	
4	IO_L75P_4/VREF_4	Y16	NC	
4	IO_L76N_4	AD16	NC	
4	IO_L76P_4	AE16	NC	

Table 9: BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
2	IO_L69P_2/VREF_2	L18	NC	
2	IO_L70N_2	K23	NC	
2	IO_L70P_2	L24	NC	
2	IO_L72N_2	K22	NC	
2	IO_L72P_2	L22	NC	
2	IO_L73N_2	L21	NC	NC
2	IO_L73P_2	L20	NC	NC
2	IO_L91N_2	M23		
2	IO_L91P_2	N24		
2	IO_L93N_2	M21		
2	IO_L93P_2/VREF_2	M22		
2	IO_L94N_2	M19		
2	IO_L94P_2	M20		
2	IO_L96N_2	M17		
2	IO_L96P_2	M18		
3	IO_L96N_3	N23		
3	IO_L96P_3	N22		
3	IO_L94N_3	N20		
3	IO_L94P_3	N21		
3	IO_L93N_3/VREF_3	N19		
3	IO_L93P_3	N18		
3	IO_L91N_3	N17		
3	IO_L91P_3	P17		
3	IO_L73N_3	P24	NC	NC
3	IO_L73P_3	R24	NC	NC
3	IO_L72N_3	R23	NC	
3	IO_L72P_3	R22	NC	
3	IO_L70N_3	P22	NC	
3	IO_L70P_3	P21	NC	
3	IO_L69N_3/VREF_3	P20	NC	
3	IO_L69P_3	P18	NC	
3	IO_L67N_3	T24	NC	
3	IO_L67P_3	U24	NC	
3	IO_L54N_3	T23		
3	IO_L54P_3	T22		

Table 10: BG728 BGA — XC2V3000

Bank	Pin Description	Pin Number
4	IO_L27P_4/VREF_4	AG19
4	IO_L28N_4	AB19
4	IO_L28P_4	AA19
4	IO_L30N_4	AC19
4	IO_L30P_4	AD19
4	IO_L49N_4	AE19
4	IO_L49P_4	AF19
4	IO_L51N_4	AA18
4	IO_L51P_4/VREF_4	Y18
4	IO_L52N_4	AB18
4	IO_L52P_4	AC18
4	IO_L54N_4	AD18
4	IO_L54P_4	AE18
4	IO_L67N_4	AF18
4	IO_L67P_4	AG18
4	IO_L69N_4	AA17
4	IO_L69P_4/VREF_4	Y17
4	IO_L70N_4	AB17
4	IO_L70P_4	AB16
4	IO_L72N_4	AD17
4	IO_L72P_4	AE17
4	IO_L73N_4	AF17
4	IO_L73P_4	AG17
4	IO_L75N_4	Y16
4	IO_L75P_4/VREF_4	W16
4	IO_L76N_4	AC16
4	IO_L76P_4	AD16
4	IO_L78N_4	AF16
4	IO_L78P_4	AG16
4	IO_L91N_4/VREF_4	W15
4	IO_L91P_4	Y15
4	IO_L92N_4	AB15
4	IO_L92P_4	AA15
4	IO_L93N_4	AC15
4	IO_L93P_4	AD15
4	IO_L94N_4/VREF_4	AE15

Table 11: FF896 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
2	IO_L78P_2	P5	NC	NC
2	IO_L91N_2	R2		
2	IO_L91P_2	P2		
2	IO_L92N_2	P8		
2	IO_L92P_2	R8		
2	IO_L93N_2	P4		
2	IO_L93P_2/VREF_2	R4		
2	IO_L94N_2	R1		
2	IO_L94P_2	T2		
2	IO_L95N_2	R7		
2	IO_L95P_2	R6		
2	IO_L96N_2	R3		
2	IO_L96P_2	P3		
3	IO_L96N_3	T7		
3	IO_L96P_3	T6		
3	IO_L95N_3	U1		
3	IO_L95P_3	V1		
3	IO_L94N_3	T3		
3	IO_L94P_3	U3		
3	IO_L93N_3/VREF_3	T8		
3	IO_L93P_3	U8		
3	IO_L92N_3	U2		
3	IO_L92P_3	V2		
3	IO_L91N_3	T4		
3	IO_L91P_3	U4		
3	IO_L78N_3	U9	NC	NC
3	IO_L78P_3	T9	NC	NC
3	IO_L77N_3	W1	NC	NC
3	IO_L77P_3	Y1	NC	NC
3	IO_L76N_3	T5	NC	NC
3	IO_L76P_3	U5	NC	NC
3	IO_L75N_3/VREF_3	U6	NC	NC
3	IO_L75P_3	V6	NC	NC
3	IO_L74N_3	W2	NC	NC
3	IO_L74P_3	Y2	NC	NC
3	IO_L73N_3	V4	NC	NC

Table 11: FF896 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
6	VCCO_6	AF29		
6	VCCO_6	AA22		
6	VCCO_6	Y22		
6	VCCO_6	Y21		
6	VCCO_6	W22		
6	VCCO_6	W21		
6	VCCO_6	V28		
6	VCCO_6	V22		
6	VCCO_6	V21		
6	VCCO_6	U21		
6	VCCO_6	T21		
7	VCCO_7	R21		
7	VCCO_7	P21		
7	VCCO_7	N28		
7	VCCO_7	N22		
7	VCCO_7	N21		
7	VCCO_7	M22		
7	VCCO_7	M21		
7	VCCO_7	L22		
7	VCCO_7	L21		
7	VCCO_7	K22		
7	VCCO_7	E29		
NA	CCLK	AF6		
NA	PROG_B	B28		
NA	DONE	AG5		
NA	M0	AF25		
NA	M1	AG26		
NA	M2	AH27		
NA	HSWAP_EN	C27		
NA	TCK	D5		
NA	TDI	A29		
NA	TDO	B3		
NA	TMS	C4		
NA	PWRDWN_B	AH4		
NA	DXN	D26		
NA	DXP	E25		

Table 11: FF896 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
NA	GND	M5		
NA	GND	K28		
NA	GND	K3		
NA	GND	H30		
NA	GND	H1		
NA	GND	G17		
NA	GND	G14		
NA	GND	F25		
NA	GND	F6		
NA	GND	E26		
NA	GND	E19		
NA	GND	E12		
NA	GND	E5		
NA	GND	D27		
NA	GND	D4		
NA	GND	C28		
NA	GND	C21		
NA	GND	C10		
NA	GND	C3		
NA	GND	B29		
NA	GND	B2		
NA	GND	A23		
NA	GND	A8		

Notes:

1. See Table 4 for an explanation of the signals available on this pin.

Table 12: FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
2	IO_L81N_2	R7	NC
2	IO_L81P_2/VREF_2	R6	NC
2	IO_L82N_2	U5	NC
2	IO_L82P_2	T5	NC
2	IO_L83N_2	T10	NC
2	IO_L83P_2	U10	NC
2	IO_L84N_2	U4	NC
2	IO_L84P_2	T4	NC
2	IO_L91N_2	T2	
2	IO_L91P_2	R1	
2	IO_L92N_2	U7	
2	IO_L92P_2	T7	
2	IO_L93N_2	T6	
2	IO_L93P_2/VREF_2	U6	
2	IO_L94N_2	U1	
2	IO_L94P_2	U2	
2	IO_L95N_2	U9	
2	IO_L95P_2	U8	
2	IO_L96N_2	U3	
2	IO_L96P_2	V4	
3	IO_L96N_3	V6	
3	IO_L96P_3	W6	
3	IO_L95N_3	V5	
3	IO_L95P_3	W5	
3	IO_L94N_3	V7	
3	IO_L94P_3	W7	
3	IO_L93N_3/VREF_3	V10	
3	IO_L93P_3	W10	
3	IO_L92N_3	V1	
3	IO_L92P_3	V2	
3	IO_L91N_3	W3	
3	IO_L91P_3	Y3	
3	IO_L84N_3	V9	NC
3	IO_L84P_3	V8	NC
3	IO_L83N_3	W4	NC

Table 12: FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
NA	GND	B34	
NA	GND	B33	
NA	GND	B20	
NA	GND	B15	
NA	GND	B2	
NA	GND	B1	
NA	GND	A33	
NA	GND	A32	
NA	GND	A27	
NA	GND	A8	
NA	GND	A3	
NA	GND	A2	

Notes:

1. See Table 4 for an explanation of the signals available on this pin.

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
1	VCCO_1	E11		
1	VCCO_1	C18		
1	VCCO_1	B14		
2	VCCO_2	W14		
2	VCCO_2	W13		
2	VCCO_2	V14		
2	VCCO_2	V13		
2	VCCO_2	V3		
2	VCCO_2	U14		
2	VCCO_2	U13		
2	VCCO_2	U11		
2	VCCO_2	T14		
2	VCCO_2	T13		
2	VCCO_2	R14		
2	VCCO_2	R13		
2	VCCO_2	R9		
2	VCCO_2	P13		
2	VCCO_2	P2		
2	VCCO_2	N7		
2	VCCO_2	L5		
3	VCCO_3	AJ5		
3	VCCO_3	AG7		
3	VCCO_3	AF13		
3	VCCO_3	AF2		
3	VCCO_3	AE14		
3	VCCO_3	AE13		
3	VCCO_3	AE9		
3	VCCO_3	AD14		
3	VCCO_3	AD13		
3	VCCO_3	AC14		
3	VCCO_3	AC13		
3	VCCO_3	AC11		
3	VCCO_3	AB14		
3	VCCO_3	AB13		
3	VCCO_3	AB3		
3	VCCO_3	AA14		

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
6	VCCO_6	AG33		
6	VCCO_6	AF38		
6	VCCO_6	AF27		
6	VCCO_6	AE31		
6	VCCO_6	AE27		
6	VCCO_6	AE26		
6	VCCO_6	AD27		
6	VCCO_6	AD26		
6	VCCO_6	AC29		
6	VCCO_6	AC27		
6	VCCO_6	AC26		
6	VCCO_6	AB37		
6	VCCO_6	AB27		
6	VCCO_6	AB26		
6	VCCO_6	AA27		
6	VCCO_6	AA26		
7	VCCO_7	W27		
7	VCCO_7	W26		
7	VCCO_7	V37		
7	VCCO_7	V27		
7	VCCO_7	V26		
7	VCCO_7	U29		
7	VCCO_7	U27		
7	VCCO_7	U26		
7	VCCO_7	T27		
7	VCCO_7	T26		
7	VCCO_7	R31		
7	VCCO_7	R27		
7	VCCO_7	R26		
7	VCCO_7	P38		
7	VCCO_7	P27		
7	VCCO_7	N33		
7	VCCO_7	L35		
NA	CCLK	AT5		
NA	PROG_B	H31		

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	GND	AR26		
NA	GND	AR14		
NA	GND	AR5		
NA	GND	AP34		
NA	GND	AP6		
NA	GND	AN33		
NA	GND	AN20		
NA	GND	AN7		
NA	GND	AM32		
NA	GND	AM23		
NA	GND	AM17		
NA	GND	AM8		
NA	GND	AL31		
NA	GND	AL9		
NA	GND	AK30		
NA	GND	AK20		
NA	GND	AK10		
NA	GND	AJ38		
NA	GND	AJ29		
NA	GND	AJ11		
NA	GND	AJ2		
NA	GND	AF35		
NA	GND	AF5		
NA	GND	AD23		
NA	GND	AD22		
NA	GND	AD21		
NA	GND	AD20		
NA	GND	AD19		
NA	GND	AD18		
NA	GND	AD17		
NA	GND	AC36		
NA	GND	AC32		
NA	GND	AC24		
NA	GND	AC23		
NA	GND	AC22		
NA	GND	AC21		

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	GND	AC20		
NA	GND	AC19		
NA	GND	AC18		
NA	GND	AC17		
NA	GND	AC16		
NA	GND	AC8		
NA	GND	AC4		
NA	GND	AB24		
NA	GND	AB23		
NA	GND	AB22		
NA	GND	AB21		
NA	GND	AB20		
NA	GND	AB19		
NA	GND	AB18		
NA	GND	AB17		
NA	GND	AB16		
NA	GND	AA24		
NA	GND	AA23		
NA	GND	AA22		
NA	GND	AA21		
NA	GND	AA20		
NA	GND	AA19		
NA	GND	AA18		
NA	GND	AA17		
NA	GND	AA16		
NA	GND	Y39		
NA	GND	Y36		
NA	GND	Y33		
NA	GND	Y30		
NA	GND	Y24		
NA	GND	Y23		
NA	GND	Y22		
NA	GND	Y21		
NA	GND	Y20		
NA	GND	Y19		
NA	GND	Y18		

Table 14: BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000

Bank	Pin Description	Pin Number	No Connect in XC2V2000
7	IO_L96N_7	R27	
7	IO_L95P_7	R24	
7	IO_L95N_7	N24	
7	IO_L94P_7	T29	
7	IO_L94N_7	R29	
7	IO_L93P_7/VREF_7	R31	
7	IO_L93N_7	P31	
7	IO_L92P_7	R26	
7	IO_L92N_7	P26	
7	IO_L91P_7	R30	
7	IO_L91N_7	P30	
7	IO_L78P_7	R25	
7	IO_L78N_7	P25	
7	IO_L77P_7	R28	
7	IO_L77N_7	P28	
7	IO_L76P_7	N31	
7	IO_L76N_7	M31	
7	IO_L75P_7/VREF_7	R23	
7	IO_L75N_7	P23	
7	IO_L74P_7	N30	
7	IO_L74N_7	M30	
7	IO_L73P_7	P27	
7	IO_L73N_7	N27	
7	IO_L72P_7	P22	
7	IO_L72N_7	N22	
7	IO_L71P_7	N29	
7	IO_L71N_7	M29	
7	IO_L70P_7	N28	
7	IO_L70N_7	M28	
7	IO_L69P_7/VREF_7	N26	
7	IO_L69N_7	M26	
7	IO_L68P_7	L31	
7	IO_L68N_7	K31	
7	IO_L67P_7	M27	
7	IO_L67N_7	L27	
7	IO_L54P_7	N23	
7	IO_L54N_7	M23	
7	IO_L53P_7	L30	

Table 14: BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000

Bank	Pin Description	Pin Number	No Connect in XC2V2000
NA	GND	D10	
NA	GND	D16	
NA	GND	D22	
NA	GND	D28	
NA	GND	E5	
NA	GND	E27	
NA	GND	F6	
NA	GND	F26	
NA	GND	G7	
NA	GND	G13	
NA	GND	G16	
NA	GND	G19	
NA	GND	G25	
NA	GND	H2	
NA	GND	H8	
NA	GND	H24	
NA	GND	H30	
NA	GND	J9	
NA	GND	J23	
NA	GND	K4	
NA	GND	K16	
NA	GND	K28	
NA	GND	N7	
NA	GND	N25	
NA	GND	P14	
NA	GND	P15	
NA	GND	P16	
NA	GND	P17	
NA	GND	P18	
NA	GND	R14	
NA	GND	R15	
NA	GND	R16	
NA	GND	R17	
NA	GND	R18	
NA	GND	T1	
NA	GND	T4	
NA	GND	T7	
NA	GND	T10	