AMD Xilinx - XC2V3000-5BF957C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	3584
Number of Logic Elements/Cells	-
Total RAM Bits	1769472
Number of I/O	684
Number of Gates	3000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	957-BBGA, FCBGA
Supplier Device Package	957-FCBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v3000-5bf957c

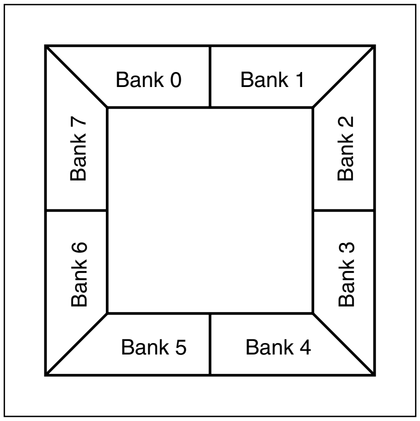

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Figure 7: **Virtex-II I/O Banks: Top View for Wire-Bond Packages (CS/CSG, FG/FGG, & BG/BGG)**

Some input standards require a user-supplied threshold voltage (V_{REF}), and certain user-I/O pins are automatically configured as V_{REF} inputs. Approximately one in six of the I/O pins in the bank assume this role.

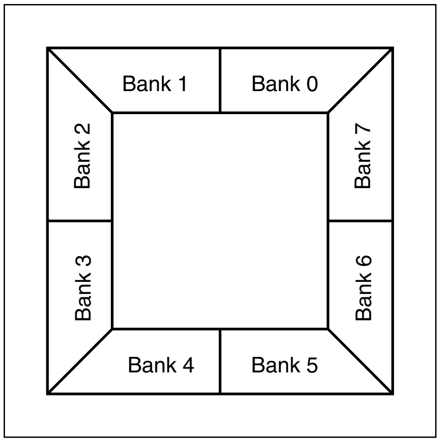

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Figure 8: **Virtex-II I/O Banks: Top View for Flip-Chip Packages (FF & BF)**

V_{REF} pins within a bank are interconnected internally, and consequently only one V_{REF} voltage can be used within each bank. However, for correct operation, all V_{REF} pins in the bank must be connected to the external reference voltage source.

The V_{CCO} and the V_{REF} pins for each bank appear in the device pinout tables. Within a given package, the number of V_{REF} and V_{CCO} pins can vary depending on the size of device. In larger devices, more I/O pins convert to V_{REF} pins. Since these are always a superset of the V_{REF} pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device if necessary.

All V_{REF} pins for the largest device anticipated must be connected to the V_{REF} voltage and not used for I/O. In smaller devices, some V_{CCO} pins used in larger devices do not connect within the package. These unconnected pins can be left unconnected externally, or, if necessary, they can be connected to V_{CCO} to permit migration to a larger device.

Rules for Combining I/O Standards in the Same Bank

The following rules must be obeyed to combine different input, output, and bi-directional standards in the same bank:

1. **Combining output standards only.** Output standards with the same output V_{CCO} requirement can be combined in the same bank.

   Compatible example:
   SSTL2_I and LVDS_25_DCI outputs

   Incompatible example:
   SSTL2_I (output V_{CCO} = 2.5V) and
   LVCMOS33 (output V_{CCO} = 3.3V) outputs

2. **Combining input standards only.** Input standards with the same input V_{CCO} and input V_{REF} requirements can be combined in the same bank.

   Compatible example:
   LVCMOS15 and HSTL_IV inputs

   Incompatible example:
   LVCMOS15 (input V_{CCO} = 1.5V) and
   LVCMOS18 (input V_{CCO} = 1.8V) inputs

   Incompatible example:
   HSTL_I_DCI_18 (V_{REF} = 0.9V) and
   HSTL_IV_DCI_18 (V_{REF} = 1.1V) inputs

3. **Combining input standards and output standards.** Input standards and output standards with the same input V_{CCO} and output V_{CCO} requirement can be combined in the same bank.

   Compatible example:
   LVDS_25 output and HSTL_I input

   Incompatible example:
   LVDS_25 output (output V_{CCO} = 2.5V) and
   HSTL_I_DCI_18 input (input V_{CCO} = 1.8V)

4. **Combining bi-directional standards with input or output standards.** When combining bi-directional I/O with other standards, make sure the bi-directional standard can meet rules 1 through 3 above.

5. **Additional rules for combining DCI I/O standards.**
   a. No more than one Single Termination type (input or output) is allowed in the same bank.

      Incompatible example:
      HSTL_IV_DCI input and HSTL_III_DCI input

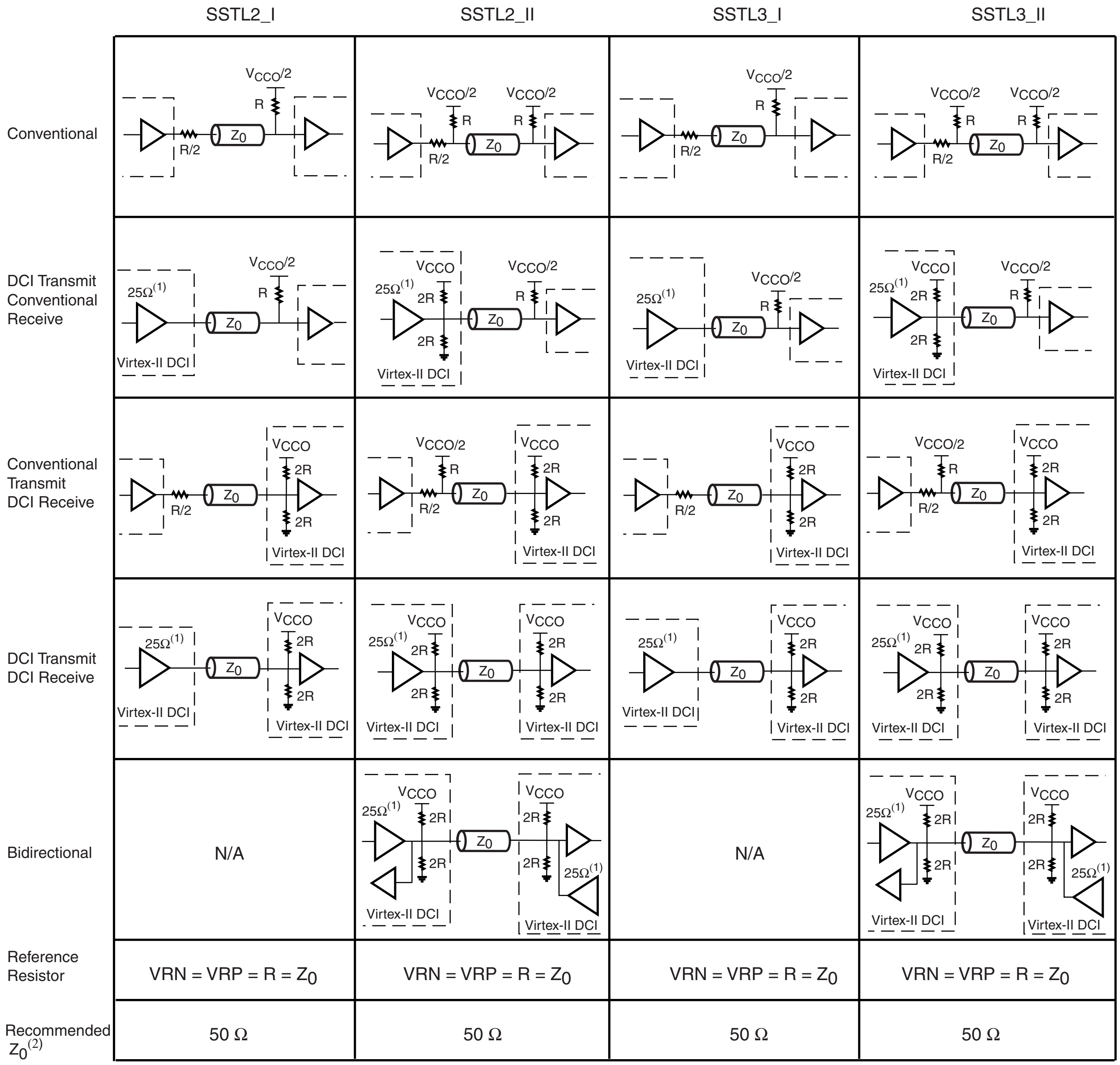
   b. No more than one Split Termination type (input or output) is allowed in the same bank.

      Incompatible example:
      HSTL_I_DCI input and HSTL_II_DCI input

The implementation tools will enforce these design rules.

Table 5 summarizes all standards and voltage supplies.

Figure 12 provides examples illustrating the use of the SSTL2_I_DCI, SSTL2_II_DCI, SSTL3_I_DCI, and SSTL3_II_DCI I/O standards. For a complete list, see the **Virtex-II Platform FPGA User Guide**.



Notes:

1. The SSTL-compatible 25Ω series resistor is accounted for in the DCI buffer, and it is not DCI controlled.
2. Z_0 is the recommended PCB trace impedance.

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Figure 12: **SSTL DCI Usage Examples**

Figure 13 provides examples illustrating the use of the LVDS_DCI and LVDSEXT_DCI I/O standards. For a complete list, see the **Virtex-II Platform FPGA User Guide**.

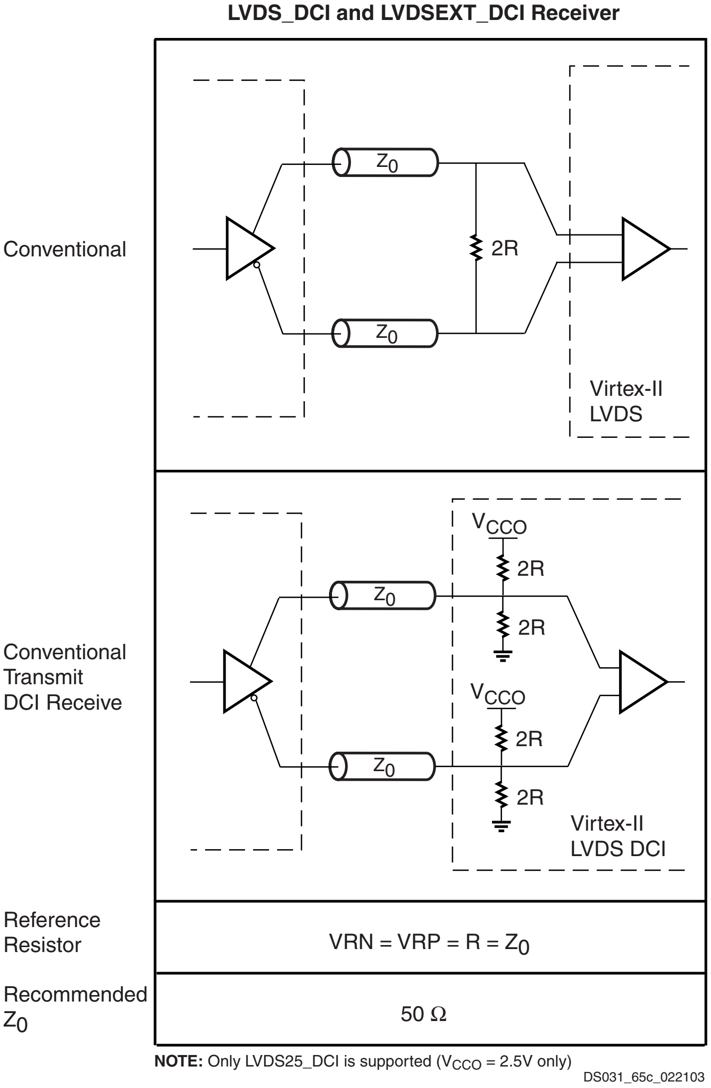


Figure 13: **LVDS DCI Usage Examples**

Multiplexers

Virtex-II function generators and associated multiplexers can implement the following:

- 4:1 multiplexer in one slice
- 8:1 multiplexer in two slices
- 16:1 multiplexer in one CLB element (4 slices)
- 32:1 multiplexer in two CLB elements (8 slices)

Each Virtex-II slice has one MUXF5 multiplexer and one MUXFX multiplexer. The MUXFX multiplexer implements the MUXF6, MUXF7, or MUXF8, as shown in Figure 23. Each CLB element has two MUXF6 multiplexers, one MUXF7 multiplexer and one MUXF8 multiplexer. Examples of multiplexers are shown in the *Virtex-II Platform FPGA User Guide*. Any LUT can implement a 2:1 multiplexer.

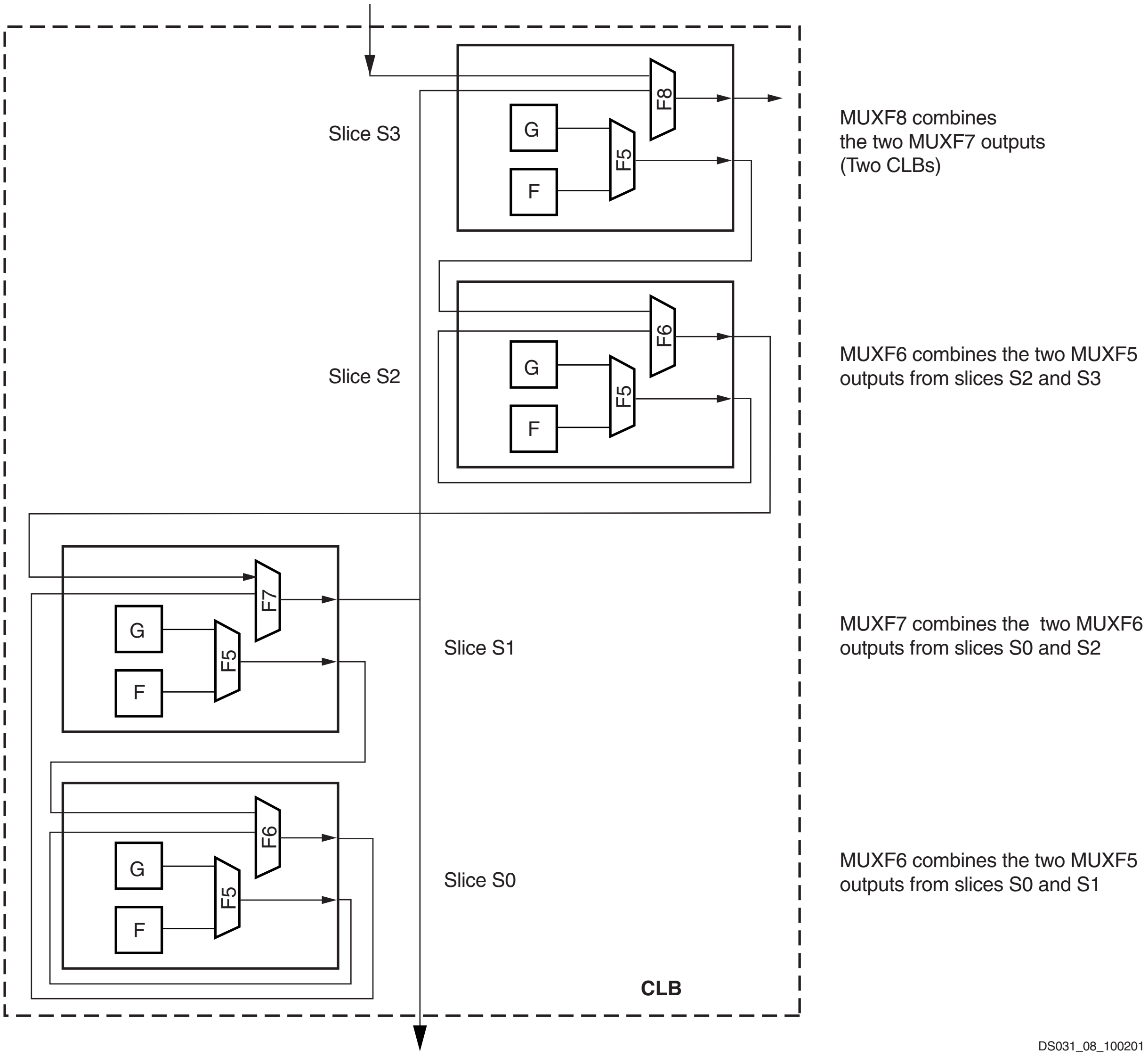


Figure 23: **MUXF5 and MUXFX multiplexers**

Fast Lookahead Carry Logic

Dedicated carry logic provides fast arithmetic addition and subtraction. The Virtex-II CLB has two separate carry chains, as shown in the Figure 24.

The height of the carry chains is two bits per slice. The carry chain in the Virtex-II device is running upward. The dedicated carry path and carry multiplexer (MUXCY) can also be used to cascade function generators for implementing wide logic functions.

Arithmetic Logic

The arithmetic logic includes an XOR gate that allows a 2-bit full adder to be implemented within a slice. In addition, a dedicated AND (MULT_AND) gate (shown in Figure 16) improves the efficiency of multiplier implementation.

3-State Buffers

Introduction

Each Virtex-II CLB contains two 3-state drivers (TBUFs) that can drive on-chip busses. Each 3-state buffer has its own 3-state control pin and its own input pin.

Each of the four slices have access to the two 3-state buffers through the switch matrix, as shown in Figure 27. TBUFs in neighboring CLBs can access slice outputs by direct connects. The outputs of the 3-state buffers drive horizontal routing resources used to implement 3-state busses.

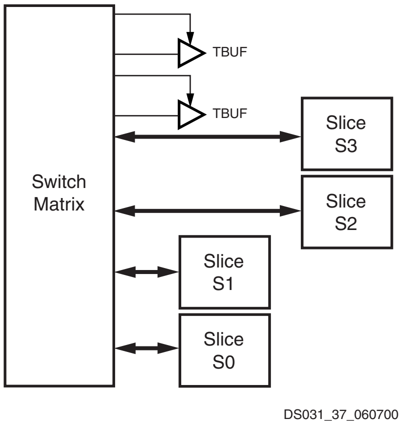


Figure 27: **Virtex-II 3-State Buffers**

The 3-state buffer logic is implemented using AND-OR logic rather than 3-state drivers, so that timing is more predictable and less load dependant especially with larger devices.

Locations / Organization

Four horizontal routing resources per CLB are provided for on-chip 3-state busses. Each 3-state buffer has access alternately to two horizontal lines, which can be partitioned as shown in Figure 28. The switch matrices corresponding to SelectRAM memory and multiplier or I/O blocks are skipped.

Number of 3-State Buffers

Table 11 shows the number of 3-state buffers available in each Virtex-II device. The number of 3-state buffers is twice the number of CLB elements.

Table 11: **Virtex-II 3-State Buffers**

Device	3-State Buffers per Row	Total Number of 3-State Buffers
XC2V40	16	128
XC2V80	16	256
XC2V250	32	768
XC2V500	48	1,536
XC2V1000	64	2,560
XC2V1500	80	3,840
XC2V2000	96	5,376
XC2V3000	112	7,168
XC2V4000	144	11,520
XC2V6000	176	16,896
XC2V8000	208	23,296

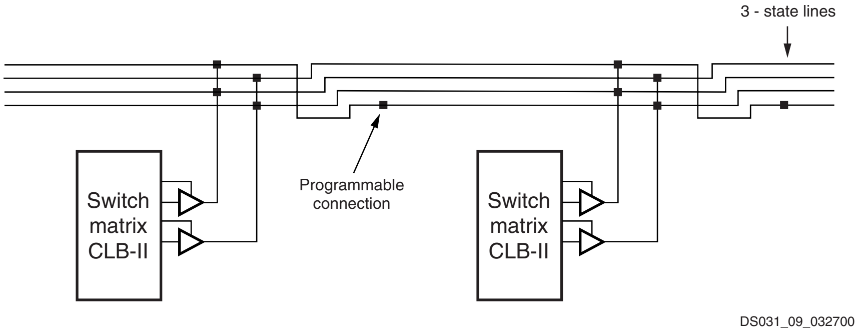


Figure 28: **3-State Buffer Connection to Horizontal Lines**

CLB/Slice Configurations

Table 12 summarizes the logic resources in one CLB. All of the CLBs are identical and each CLB or slice can be implemented in one of the configurations listed. Table 13 shows the available resources in all CLBs.

Table 12: **Logic Resources in One CLB**

Slices	LUTs	Flip-Flops	MULT_ANDs	Arithmetic & Carry-Chains	SOP Chains	Distributed SelectRAM	Shift Registers	TBUF
4	8	8	8	2	2	128 bits	128 bits	2

Notice of Disclaimer

Virtex-II Data Sheet

The Virtex-II Data Sheet contains the following modules:

- Virtex-II Platform FPGAs: Introduction and Overview (Module 1)
- Virtex-II Platform FPGAs: Functional Description (Module 2)
- Virtex-II Platform FPGAs: DC and Switching Characteristics (Module 3)
- Virtex-II Platform FPGAs: Pinout Information (Module 4)

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *Without* DCM

Table 35: **Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *Without* DCM**

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
LVTTL Global Clock Input to Output Delay using Output flip-flop, 12 mA, Fast Slew Rate, *without* DCM. For data *output* with different standards, adjust the delays with the values shown in IOB Output Switching Characteristics Standard Adjustments, page 14.						
Global Clock and OFF without DCM	T_{ICKOF}	XC2V40	3.46	3.58	3.69	ns
		XC2V80	3.62	3.58	3.69	ns
		XC2V250	3.79	3.88	4.47	ns
		XC2V500	3.85	3.88	4.47	ns
		XC2V1000	4.02	4.28	4.62	ns
		XC2V1500	4.16	4.28	4.62	ns
		XC2V2000	4.30	4.43	5.10	ns
		XC2V3000	4.49	4.64	5.34	ns
		XC2V4000	4.82	4.99	5.74	ns
		XC2V6000	5.19	5.38	5.93	ns
		XC2V8000		6.09	7.00	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with test setup shown in Figure 1. For other I/O standards, see Table 19.

Global Clock Setup and Hold for LVTTL Standard, *Without* DCM

Table 37: **Global Clock Setup and Hold for LVTTL Standard, *Without* DCM**

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard.[2] For data input with different standards, adjust the setup time delay by the values shown in IOB Input Switching Characteristics Standard Adjustments, page 11.						
Full Delay Global Clock and IFF[1] without DCM	T_{PSFD}/T_{PHFD}	XC2V40	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V80	2.10/ 0.00	2.10/ 0.00	2.21/ 0.00	ns
		XC2V250	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V500	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V1000	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V1500	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V2000	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V3000	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V4000	2.00/ 0.00	2.00/ 0.00	2.30/ 0.00	ns
		XC2V6000	1.92/ 0.50	1.92/ 0.50	2.21/ 0.50	ns
		XC2V8000		2.38/ 0.00	2.60/ 0.00	ns

Notes:

1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. These values are parametrically measured.

Virtex-II Platform FPGAs: Pinout Information

DS031-4 (v3.5) November 5, 2007 **Product Specification**

This document provides Virtex-II™ Device/Package Combinations, Maximum I/Os Available, and Virtex-II Pin Definitions, followed by pinout tables for the following packages:

- CS144/CSG144 Chip-Scale BGA Package
- FG256/FGG256 Fine-Pitch BGA Package
- FG456/FGG456 Fine-Pitch BGA Package
- FG676/FGG676 Fine-Pitch BGA Package
- BG575/BGG575 Standard BGA Package
- BG728/BGG728 Standard BGA Package
- FF896 Flip-Chip Fine-Pitch BGA Package
- FF1152 Flip-Chip Fine-Pitch BGA Package
- FF1517 Flip-Chip Fine-Pitch BGA Package
- BF957 Flip-Chip BGA Package

For device pinout diagrams and layout guidelines, refer to the ***Virtex-II Platform FPGA User Guide***. ASCII package pinout files are also available for download from the Xilinx website (**www.xilinx.com**).

Virtex-II Device/Package Combinations and Maximum I/Os Available

Wire-bond and flip-chip packages are available. Table 1 and Table 2 show the maximum number of user I/Os possible in wire-bond and flip-chip packages, respectively.

Table 3 shows the number of user I/Os available for all device/package combinations.

- CS denotes wire-bond chip-scale ball grid array (BGA) (0.80 mm pitch).
- CSG denotes Pb-free wire-bond chip-scale ball grid array (BGA) (0.80 mm pitch).
- FG denotes wire-bond fine-pitch BGA (1.00 mm pitch).
- FGG denotes Pb-free wire-bond fine-pitch BGA (1.00 mm pitch).
- BG denotes standard BGA (1.27 mm pitch).
- BGG denotes Pb-free standard BGA (1.27 mm pitch).
- FF denotes flip-chip fine-pitch BGA (1.00 mm pitch).
- BF denotes flip-chip BGA (1.27 mm pitch).

The number of I/Os per package include all user I/Os except the 15 control pins (CCLK, DONE, M0, M1, M2, PROG_B, PWRDWN_B, TCK, TDI, TDO, TMS, HSWAP_EN, DXN, DXP, AND RSVD).

Table 1: **Wire-Bond Packages Information**

Package(1)	CS144/ CSG144	FG256/ FGG256	FG456/ FGG456	FG676/ FGG676	BG575/ BGG575	BG728/ BGG728
Pitch (mm)	0.80	1.00	1.00	1.00	1.27	1.27
Size (mm)	12 x 12	17 x 17	23 x 23	27 x 27	31 x 31	35 x 35
I/Os	92	172	324	484	408	516

Notes:
1. Wire-bond packages include FGG*nnn* Pb-free versions. See Virtex-II Ordering Examples (Module 1).

Table 2: **Flip-Chip Packages Information**

Package	FF896	FF1152	FF1517	BF957
Pitch (mm)	1.00	1.00	1.00	1.27
Size (mm)	31 x 31	35 x 35	40 x 40	40 x 40
I/Os	624	824	1,108	684

Table 6: **FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
7	IO_L45N_7	F5	NC	NC
7	IO_L43P_7	F1	NC	NC
7	IO_L43N_7	F2	NC	NC
7	IO_L06P_7	F3	NC	
7	IO_L06N_7	F4	NC	
7	IO_L04P_7	E1	NC	
7	IO_L04N_7	E2	NC	
7	IO_L03P_7/VREF_7	E3		
7	IO_L03N_7	E4		
7	IO_L02P_7/VRN_7	D2		
7	IO_L02N_7/VRP_7	D3		
7	IO_L01P_7	D1		
7	IO_L01N_7	C1		
0	VCCO_0	F8		
0	VCCO_0	F7		
0	VCCO_0	E8		
1	VCCO_1	F10		
1	VCCO_1	F9		
1	VCCO_1	E9		
2	VCCO_2	H12		
2	VCCO_2	H11		
2	VCCO_2	G11		
3	VCCO_3	K11		
3	VCCO_3	J12		
3	VCCO_3	J11		
4	VCCO_4	M9		
4	VCCO_4	L10		
4	VCCO_4	L9		
5	VCCO_5	M8		
5	VCCO_5	L8		
5	VCCO_5	L7		
6	VCCO_6	K6		
6	VCCO_6	J6		

Table 6: **FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
6	VCCO_6	J5		
7	VCCO_7	H6		
7	VCCO_7	H5		
7	VCCO_7	G6		
NA	CCLK	P15		
NA	PROG_B	A2		
NA	DONE	R14		
NA	M0	T2		
NA	M1	P2		
NA	M2	R3		
NA	HSWAP_EN	B3		
NA	TCK	A15		
NA	TDI	C2		
NA	TDO	C15		
NA	TMS	B14		
NA	PWRDWN_B	T15		
NA	RSVD	A4		
NA	RSVD	A3		
NA	VBATT	A14		
NA	RSVD	A13		
NA	VCCAUX	R16		
NA	VCCAUX	R1		
NA	VCCAUX	B16		
NA	VCCAUX	B1		
NA	VCCINT	N13		
NA	VCCINT	N4		
NA	VCCINT	M12		
NA	VCCINT	M5		
NA	VCCINT	E12		
NA	VCCINT	E5		
NA	VCCINT	D13		
NA	VCCINT	D4		

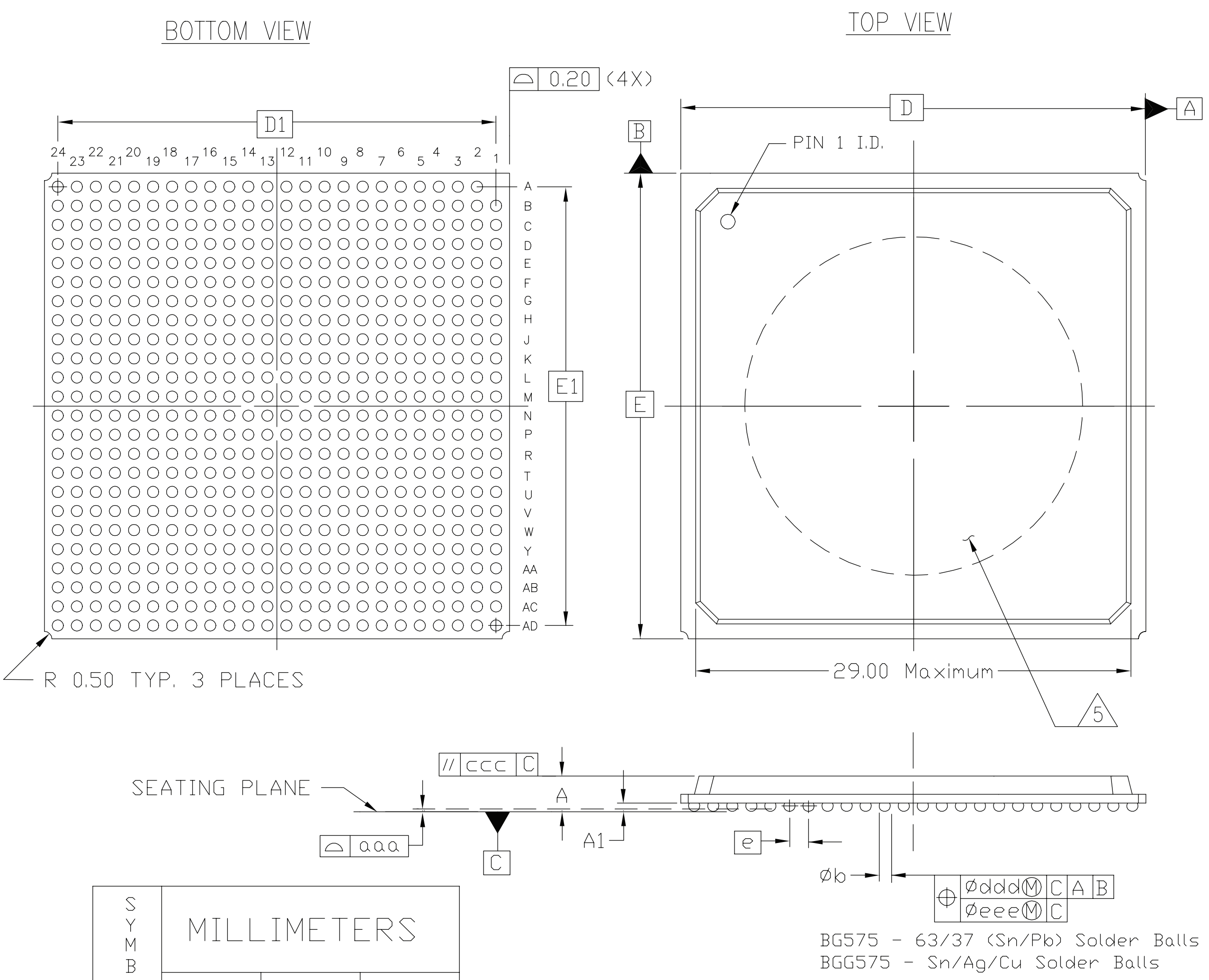
Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
1	IO_L19N_1	E20		
1	IO_L19P_1	F20		
1	IO_L06N_1	B21		
1	IO_L06P_1	B22		
1	IO_L05N_1	A22		
1	IO_L05P_1	A23		
1	IO_L04N_1	C21		
1	IO_L04P_1/VREF_1	D21		
1	IO_L03N_1/VRP_1	C20		
1	IO_L03P_1/VRN_1	D20		
1	IO_L02N_1	A24		
1	IO_L02P_1	A25		
1	IO_L01N_1	B23		
1	IO_L01P_1	B24		
2	IO_L01N_2	B26		
2	IO_L01P_2	C26		
2	IO_L02N_2/VRP_2	G20		
2	IO_L02P_2/VRN_2	H20		
2	IO_L03N_2	C25		
2	IO_L03P_2/VREF_2	D25		
2	IO_L04N_2	E23		
2	IO_L04P_2	E24		
2	IO_L06N_2	G21		
2	IO_L06P_2	G22		
2	IO_L19N_2	D26		
2	IO_L19P_2	E26		
2	IO_L21N_2	F23		
2	IO_L21P_2/VREF_2	F24		
2	IO_L22N_2	E25		
2	IO_L22P_2	F25		
2	IO_L24N_2	H22		
2	IO_L24P_2	H21		
2	IO_L25N_2	G23	NC	NC
2	IO_L25P_2	G24	NC	NC
2	IO_L43N_2	F26		
2	IO_L43P_2	G26		

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
5	IO_L70N_5	W11		
5	IO_L70P_5	Y10		
5	IO_L69N_5/VREF_5	Y11		
5	IO_L69P_5	AA11		
5	IO_L67N_5	AF9		
5	IO_L67P_5	AF8		
5	IO_L54N_5	AE9		
5	IO_L54P_5	AD9		
5	IO_L52N_5	AB10		
5	IO_L52P_5	AA10		
5	IO_L51N_5/VREF_5	AD10		
5	IO_L51P_5	AC10		
5	IO_L49N_5	AE8		
5	IO_L49P_5	AF7		
5	IO_L28N_5	AD8	NC	NC
5	IO_L28P_5	AC8	NC	NC
5	IO_L27N_5/VREF_5	AB9	NC	NC
5	IO_L27P_5	AC9	NC	NC
5	IO_L25N_5	AA9	NC	NC
5	IO_L25P_5	Y9	NC	NC
5	IO_L24N_5	AF6		
5	IO_L24P_5	AE6		
5	IO_L22N_5	AB8		
5	IO_L22P_5	AA8		
5	IO_L21N_5/VREF_5	AC7		
5	IO_L21P_5	AD7		
5	IO_L19N_5	AF5		
5	IO_L19P_5	AE5		
5	IO_L06N_5	AF4		
5	IO_L06P_5	AE4		
5	IO_L05N_5/VRP_5	AF3		
5	IO_L05P_5/VRN_5	AE3		
5	IO_L04N_5	Y8		
5	IO_L04P_5/VREF_5	Y7		
5	IO_L03N_5/D4/ALT_VRP_5	AB7		
5	IO_L03P_5/D5/ALT_VRN_5	AA7		
5	IO_L02N_5/D6	AD6		

BG575/BGG575 Standard BGA Package Specifications (1.27mm pitch)



BG575 - 63/37 (Sn/Pb) Solder Balls
BGG575 - Sn/Ag/Cu Solder Balls

SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A	—	2.33	2.60
A_1	0.50	0.60	0.70
D/E	31.00 BSC		
D_1/E_1	29.21 REF		
e	1.27BSC		
Øb	0.60	0.75	0.90
aaa	—	—	0.20
ccc	—	—	0.35
ddd	—	—	0.30
eee	—	—	0.15
M	24		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-BAN-1 (DEPOPULATED)
4. NO SOLDER BALL AND LAND ON A1.

△5 HEAT SINK OPTION

575-BALL MOLDED BGA (BG575/BGG575)

Figure 5: **BG575/BGG575 Standard BGA Package Specifications**

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
7	IO_L95N_7	R24		
7	IO_L94P_7	R29		
7	IO_L94N_7	T29		
7	IO_L93P_7/VREF_7	R27		
7	IO_L93N_7	P27		
7	IO_L92P_7	R23		
7	IO_L92N_7	P23		
7	IO_L91P_7	N30		
7	IO_L91N_7	P30		
7	IO_L78P_7	P26	NC	NC
7	IO_L78N_7	R26	NC	NC
7	IO_L77P_7	R22	NC	NC
7	IO_L77N_7	P22	NC	NC
7	IO_L76P_7	N29	NC	NC
7	IO_L76N_7	P29	NC	NC
7	IO_L75P_7/VREF_7	N27	NC	NC
7	IO_L75N_7	N26	NC	NC
7	IO_L74P_7	P25	NC	NC
7	IO_L74N_7	N25	NC	NC
7	IO_L73P_7	L30	NC	NC
7	IO_L73N_7	M30	NC	NC
7	IO_L72P_7	L28	NC	
7	IO_L72N_7	M28	NC	
7	IO_L71P_7	N24	NC	
7	IO_L71N_7	M24	NC	
7	IO_L70P_7	L29	NC	
7	IO_L70N_7	M29	NC	
7	IO_L69P_7/VREF_7	M27	NC	
7	IO_L69N_7	L27	NC	
7	IO_L68P_7	N23	NC	
7	IO_L68N_7	M23	NC	
7	IO_L67P_7	J30	NC	
7	IO_L67N_7	K30	NC	
7	IO_L54P_7	K26		
7	IO_L54N_7	L26		
7	IO_L53P_7	M25		
7	IO_L53N_7	L25		

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
0	IO_L77N_0	J20	
0	IO_L77P_0	K19	
0	IO_L78N_0	D20	
0	IO_L78P_0	D21	
0	IO_L79N_0	A21	NC
0	IO_L79P_0	A22	NC
0	IO_L80N_0	L19	NC
0	IO_L80P_0	L18	NC
0	IO_L81N_0	B19	NC
0	IO_L81P_0/VREF_0	A20	NC
0	IO_L82N_0	A18	NC
0	IO_L82P_0	B18	NC
0	IO_L83N_0	H19	NC
0	IO_L83P_0	H18	NC
0	IO_L84N_0	C20	NC
0	IO_L84P_0	C21	NC
0	IO_L91N_0/VREF_0	D19	
0	IO_L91P_0	D18	
0	IO_L92N_0	G18	
0	IO_L92P_0	G19	
0	IO_L93N_0	F18	
0	IO_L93P_0	F19	
0	IO_L94N_0/VREF_0	C19	
0	IO_L94P_0	C18	
0	IO_L95N_0/GCLK7P	K18	
0	IO_L95P_0/GCLK6S	J18	
0	IO_L96N_0/GCLK5P	E19	
0	IO_L96P_0/GCLK4S	E18	
1	IO_L96N_1/GCLK3P	E17	
1	IO_L96P_1/GCLK2S	E16	
1	IO_L95N_1/GCLK1P	H17	
1	IO_L95P_1/GCLK0S	H16	
1	IO_L94N_1	D17	
1	IO_L94P_1/VREF_1	D16	
1	IO_L93N_1	F16	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	VCCINT	AE18		
NA	VCCINT	AE17		
NA	VCCINT	AE16		
NA	VCCINT	AE15		
NA	VCCINT	AD25		
NA	VCCINT	AD24		
NA	VCCINT	AD16		
NA	VCCINT	AD15		
NA	VCCINT	AC25		
NA	VCCINT	AC15		
NA	VCCINT	AB25		
NA	VCCINT	AB15		
NA	VCCINT	AA25		
NA	VCCINT	AA15		
NA	VCCINT	Y27		
NA	VCCINT	Y26		
NA	VCCINT	Y25		
NA	VCCINT	Y15		
NA	VCCINT	Y14		
NA	VCCINT	Y13		
NA	VCCINT	W25		
NA	VCCINT	W15		
NA	VCCINT	V25		
NA	VCCINT	V15		
NA	VCCINT	U25		
NA	VCCINT	U15		
NA	VCCINT	T25		
NA	VCCINT	T24		
NA	VCCINT	T16		
NA	VCCINT	T15		
NA	VCCINT	R25		
NA	VCCINT	R24		
NA	VCCINT	R23		
NA	VCCINT	R22		
NA	VCCINT	R21		
NA	VCCINT	R20		

BF957 Flip-Chip BGA Package

As shown in Table 14, XC2V2000, XC2V3000, XC2V4000, and XC2V6000 Virtex-II devices are available in the BF957 package. Pins in each of these devices are the same, except for the pin differences in the XC2V2000 device shown in the No Connect column. Following this table are the BF957 Flip-Chip BGA Package Specifications (1.27mm pitch).

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
0	IO_L01N_0	H23	
0	IO_L01P_0	H22	
0	IO_L02N_0	G24	
0	IO_L02P_0	E25	
0	IO_L03N_0/VRP_0	B29	
0	IO_L03P_0/VRN_0	C27	
0	IO_L04N_0/VREF_0	F24	
0	IO_L04P_0	F23	
0	IO_L05N_0	D26	
0	IO_L05P_0	D25	
0	IO_L06N_0	A28	
0	IO_L06P_0	A27	
0	IO_L19N_0	J22	
0	IO_L19P_0	J21	
0	IO_L20N_0	G23	
0	IO_L20P_0	G22	
0	IO_L21N_0	B27	
0	IO_L21P_0/VREF_0	B26	
0	IO_L22N_0	K20	
0	IO_L22P_0	K19	
0	IO_L23N_0	C26	
0	IO_L23P_0	C24	
0	IO_L24N_0	D24	
0	IO_L24P_0	D23	
0	IO_L25N_0	E24	NC
0	IO_L25P_0	E23	NC
0	IO_L26N_0	G21	NC
0	IO_L26P_0	G20	NC
0	IO_L27N_0	A26	NC
0	IO_L27P_0/VREF_0	A25	NC
0	IO_L29N_0	H21	NC
0	IO_L29P_0	H20	NC
0	IO_L30N_0	B25	NC
0	IO_L30P_0	B23	NC

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
0	IO_L49N_0	C23	
0	IO_L49P_0	C22	
0	IO_L50N_0	E22	
0	IO_L50P_0	E21	
0	IO_L51N_0	F21	
0	IO_L51P_0/VREF_0	F20	
0	IO_L52N_0	A24	
0	IO_L52P_0	A23	
0	IO_L53N_0	E20	
0	IO_L53P_0	E19	
0	IO_L54N_0	B22	
0	IO_L54P_0	B21	
0	IO_L67N_0	D21	
0	IO_L67P_0	D20	
0	IO_L68N_0	J20	
0	IO_L68P_0	J19	
0	IO_L69N_0	F19	
0	IO_L69P_0/VREF_0	F18	
0	IO_L70N_0	A22	
0	IO_L70P_0	A21	
0	IO_L71N_0	H19	
0	IO_L71P_0	H17	
0	IO_L72N_0	C21	
0	IO_L72P_0	C20	
0	IO_L73N_0	B20	
0	IO_L73P_0	B19	
0	IO_L74N_0	G18	
0	IO_L74P_0	G17	
0	IO_L75N_0	E18	
0	IO_L75P_0/VREF_0	D17	
0	IO_L76N_0	A20	
0	IO_L76P_0	A19	
0	IO_L77N_0	D19	
0	IO_L77P_0	D18	
0	IO_L78N_0	C19	
0	IO_L78P_0	C17	
0	IO_L91N_0/VREF_0	K18	
0	IO_L91P_0	J18	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
5	IO_L24P_5	AG23	
5	IO_L23N_5	AE22	
5	IO_L23P_5	AE23	
5	IO_L22N_5	AK25	
5	IO_L22P_5	AK26	
5	IO_L21N_5/VREF_5	AH25	
5	IO_L21P_5	AG25	
5	IO_L20N_5	AB21	
5	IO_L20P_5	AC22	
5	IO_L19N_5	AL27	
5	IO_L19P_5	AL28	
5	IO_L06N_5	AK27	
5	IO_L06P_5	AJ27	
5	IO_L05N_5/VRP_5	AD23	
5	IO_L05P_5/VRN_5	AE24	
5	IO_L04N_5	AJ26	
5	IO_L04P_5/VREF_5	AH26	
5	IO_L03N_5/D4/ALT_VRP_5	AF23	
5	IO_L03P_5/D5/ALT_VRN_5	AF24	
5	IO_L02N_5/D6	AG24	
5	IO_L02P_5/D7	AF25	
5	IO_L01N_5/RDWR_B	AK28	
5	IO_L01P_5/CS_B	AK29	
6	IO_L01P_6	AF27	
6	IO_L01N_6	AF28	
6	IO_L02P_6/VRN_6	AE26	
6	IO_L02N_6/VRP_6	AE27	
6	IO_L03P_6	AH29	
6	IO_L03N_6/VREF_6	AH30	
6	IO_L04P_6	AB22	
6	IO_L04N_6	AB23	
6	IO_L05P_6	AG28	
6	IO_L05N_6	AG29	
6	IO_L06P_6	AH31	
6	IO_L06N_6	AG31	
6	IO_L19P_6	AA22	
6	IO_L19N_6	Y22	