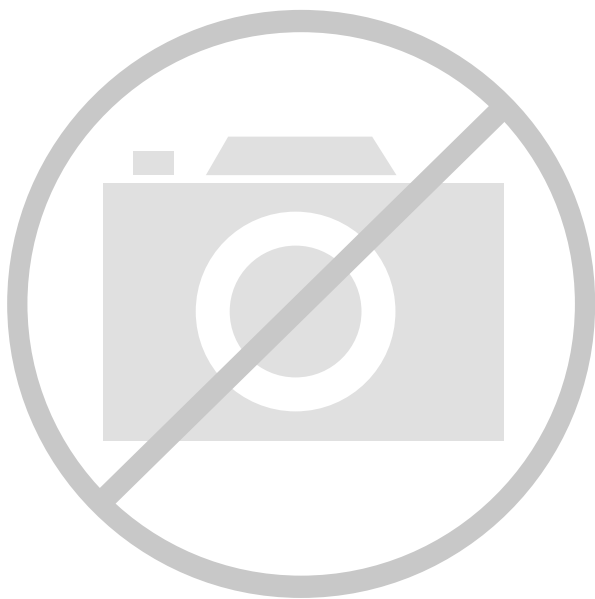




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	3584
Number of Logic Elements/Cells	-
Total RAM Bits	1769472
Number of I/O	684
Number of Gates	3000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	957-BBGA, FCBGA
Supplier Device Package	957-FCBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v3000-5bfg957i

Architecture

Virtex-II Array Overview

Virtex-II devices are user-programmable gate arrays with various configurable elements. The Virtex-II architecture is optimized for high-density and high-performance logic designs. As shown in **Figure 1**, the programmable device is comprised of input/output blocks (IOBs) and internal configurable logic blocks (CLBs).

Programmable I/O blocks provide the interface between package pins and the internal configurable logic. Most popular and leading-edge I/O standards are supported by the programmable IOBs.

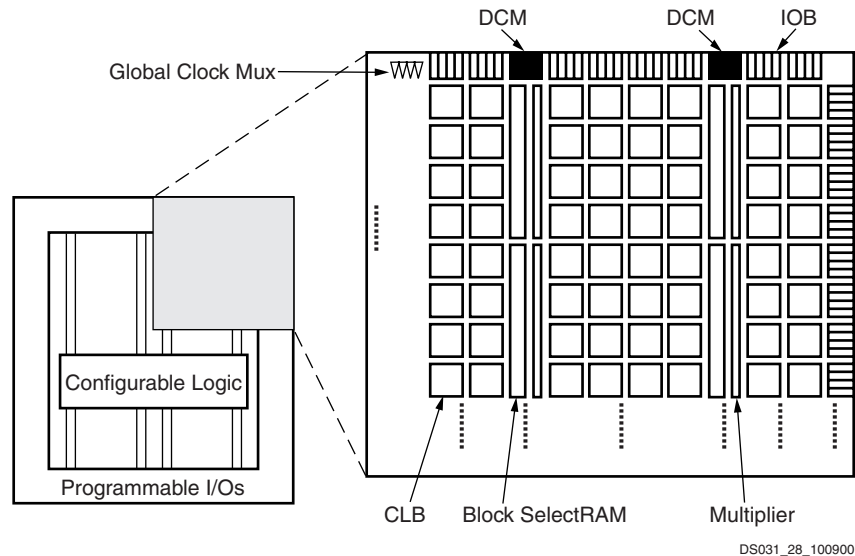


Figure 1: Virtex-II Architecture Overview

The internal configurable logic includes four major elements organized in a regular array.

- Configurable Logic Blocks (CLBs) provide functional elements for combinatorial and synchronous logic, including basic storage elements. BUFTs (3-state buffers) associated with each CLB element drive dedicated segmentable horizontal routing resources.
- Block SelectRAM memory modules provide large 18 Kbit storage elements of dual-port RAM.
- Multiplier blocks are 18-bit x 18-bit dedicated multipliers.
- DCM (Digital Clock Manager) blocks provide self-calibrating, fully digital solutions for clock distribution delay compensation, clock multiplication and division, coarse- and fine-grained clock phase shifting.

A new generation of programmable routing resources called Active Interconnect Technology interconnects all of these elements. The general routing matrix (GRM) is an array of routing switches. Each programmable element is tied to a switch matrix, allowing multiple connections to the general routing matrix. The overall programmable interconnection is hierarchical and designed to support high-speed designs.

All programmable elements, including the routing resources, are controlled by values stored in static memory cells. These values are loaded in the memory cells during

configuration and can be reloaded to change the functions of the programmable elements.

Virtex-II Features

This section briefly describes Virtex-II features.

Input/Output Blocks (IOBs)

IOBs are programmable and can be categorized as follows:

- Input block with an optional single-data-rate or double-data-rate (DDR) register
- Output block with an optional single-data-rate or DDR register, and an optional 3-state buffer, to be driven directly or through a single or DDR register
- Bidirectional block (any combination of input and output configurations)

These registers are either edge-triggered D-type flip-flops or level-sensitive latches.

IOBs support the following single-ended I/O standards:

- LVTTL, LVCMOS (3.3V, 2.5V, 1.8V, and 1.5V)
- PCI-X compatible (133 MHz and 66 MHz) at 3.3V
- PCI compliant (66 MHz and 33 MHz) at 3.3V
- CardBus compliant (33 MHz) at 3.3V
- GTL and GTLP

Table 25: Pipelined Multiplier Switching Characteristics

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Setup and Hold Times Before/After Clock					
Data Inputs	T _{MULIDCK} /T _{MULCKID}	3.00/ 0.00	3.45/ 0.00	3.89/ 0.00	ns, Max
Clock Enable	T _{MULIDCK_CE} /T _{MULCKID_CE}	0.72/ 0.00	0.80/ 0.00	0.86/ 0.00	ns, Max
Reset	T _{MULIDCK_RST} /T _{MULCKID_RST}	0.72/ 0.00	0.80/ 0.00	0.86/ 0.00	ns, Max
Clock to Output Pin					
Clock to Pin 35	T _{MULTCK_P35}	3.05	6.91	8.12	ns, Max
Clock to Pin 34	T _{MULTCK_P34}	2.95	6.75	7.93	ns, Max
Clock to Pin 33	T _{MULTCK_P33}	2.85	6.59	7.74	ns, Max
Clock to Pin 32	T _{MULTCK_P32}	2.76	6.43	7.56	ns, Max
Clock to Pin 31	T _{MULTCK_P31}	2.66	6.27	7.37	ns, Max
Clock to Pin 30	T _{MULTCK_P30}	2.56	6.11	7.19	ns, Max
Clock to Pin 29	T _{MULTCK_P29}	2.47	5.95	7.00	ns, Max
Clock to Pin 28	T _{MULTCK_P28}	2.37	5.79	6.81	ns, Max
Clock to Pin 27	T _{MULTCK_P27}	2.27	5.63	6.63	ns, Max
Clock to Pin 26	T _{MULTCK_P26}	2.17	5.47	6.44	ns, Max
Clock to Pin 25	T _{MULTCK_P25}	2.08	5.31	6.26	ns, Max
Clock to Pin 24	T _{MULTCK_P24}	1.98	5.15	6.07	ns, Max
Clock to Pin 23	T _{MULTCK_P23}	1.88	4.99	5.88	ns, Max
Clock to Pin 22	T _{MULTCK_P22}	1.79	4.83	5.70	ns, Max
Clock to Pin 21	T _{MULTCK_P21}	1.69	4.67	5.51	ns, Max
Clock to Pin 20	T _{MULTCK_P20}	1.59	4.51	5.33	ns, Max
Clock to Pin 19	T _{MULTCK_P19}	1.50	4.35	5.14	ns, Max
Clock to Pin 18	T _{MULTCK_P18}	1.40	4.19	4.95	ns, Max
Clock to Pin 17	T _{MULTCK_P17}	1.30	4.03	4.77	ns, Max
Clock to Pin 16	T _{MULTCK_P16}	1.20	3.87	4.58	ns, Max
Clock to Pin 15	T _{MULTCK_P15}	1.11	3.71	4.40	ns, Max
Clock to Pin 14	T _{MULTCK_P14}	1.01	3.55	4.21	ns, Max
Clock to Pin 13	T _{MULTCK_P13}	0.91	3.39	4.02	ns, Max
Clock to Pin 12	T _{MULTCK_P12}	0.91	3.23	3.84	ns, Max
Clock to Pin 11	T _{MULTCK_P11}	0.91	3.07	3.65	ns, Max
Clock to Pin 10	T _{MULTCK_P10}	0.91	2.91	3.47	ns, Max
Clock to Pin 9	T _{MULTCK_P9}	0.91	2.75	3.28	ns, Max
Clock to Pin 8	T _{MULTCK_P8}	0.91	2.59	3.09	ns, Max
Clock to Pin 7	T _{MULTCK_P7}	0.91	2.43	2.91	ns, Max
Clock to Pin 6	T _{MULTCK_P6}	0.91	2.27	2.72	ns, Max
Clock to Pin 5	T _{MULTCK_P5}	0.91	2.11	2.54	ns, Max
Clock to Pin 4	T _{MULTCK_P4}	0.91	1.95	2.35	ns, Max
Clock to Pin 3	T _{MULTCK_P3}	0.91	1.79	2.16	ns, Max
Clock to Pin 2	T _{MULTCK_P2}	0.91	1.63	1.98	ns, Max
Clock to Pin 1	T _{MULTCK_P1}	0.91	1.47	1.79	ns, Max
Clock to Pin 0	T _{MULTCK_P0}	0.91	1.31	1.61	ns, Max

Virtex-II Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, With DCM

Table 34: Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, With DCM

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
LVTTL Global Clock Input to Output delay using Output flip-flop, 12 mA, Fast Slew Rate, <i>with</i> DCM. For data <i>output</i> with different standards, adjust the delays with the values shown in IOB Output Switching Characteristics Standard Adjustments, page 14.						
Global Clock and OFF with DCM	T _{ICKOFFDCM}	XC2V40	1.10	1.28	1.48	ns
		XC2V80	1.10	1.28	1.48	ns
		XC2V250	1.10	1.28	1.48	ns
		XC2V500	1.10	1.28	1.48	ns
		XC2V1000	1.10	1.28	1.48	ns
		XC2V1500	1.10	1.28	1.48	ns
		XC2V2000	1.10	1.28	1.48	ns
		XC2V3000	1.19	1.38	1.59	ns
		XC2V4000	1.19	1.38	1.59	ns
		XC2V6000	1.64	1.88	2.17	ns
		XC2V8000		1.88	2.17	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with test setup shown in [Figure 1](#). For other I/O standards, see [Table 19](#).

DCM Timing Parameters

All devices are 100% functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values

across the recommended operating conditions. All output jitter and phase specifications are determined through statistical measurement at the package pins.

Operating Frequency Ranges

Table 38: Operating Frequency Ranges

Description	Symbol	Constraint s	Speed Grade			Unit s
			-6	-5	-4	
Output Clocks (Low Frequency Mode)						
CLK0, CLK90, CLK180, CLK270	CLKOUT_FREQ_1X_LF_Min		24.00	24.00	24.00	MHz
	CLKOUT_FREQ_1X_LF_Max		230.00	210.00	180.00	MHz
CLK2X, CLK2X180	CLKOUT_FREQ_2X_LF_Min		48.00	48.00	48.00	MHz
	CLKOUT_FREQ_2X_LF_Max		450.00	420.00	360.00	MHz
CLKDV	CLKOUT_FREQ_DV_LF_Min		1.50	1.50	1.50	MHz
	CLKOUT_FREQ_DV_LF_Max		150.00	140.00	120.00	MHz
CLKFX, CLKFX180	CLKOUT_FREQ_FX_LF_Min		24.00	24.00	24.00	MHz
	CLKOUT_FREQ_FX_LF_Max		260.00	240.00	210.00	MHz
Input Clocks (Low Frequency Mode)						
CLKIN (using DLL outputs) ^(1,3,4)	CLKIN_FREQ_DLL_LF_Min		24.00	24.00	24.00	MHz
	CLKIN_FREQ_DLL_LF_Max		230.00	210.00	180.00	MHz
CLKIN (using CLKFX outputs) ^(2,3,4)	CLKIN_FREQ_FX_LF_Min		1.00	1.00	1.00	MHz
	CLKIN_FREQ_FX_LF_Max		260.00	240.00	210.00	MHz
PSCLK	PSCLK_FREQ_LF_Min		0.01	0.01	0.01	MHz
	PSCLK_FREQ_LF_Max		450.00	420.00	360.00	MHz
Output Clocks (High Frequency Mode)						
CLK0, CLK180	CLKOUT_FREQ_1X_HF_Min		48.00	48.00	48.00	MHz
	CLKOUT_FREQ_1X_HF_Max		450.00	420.00	360.00	MHz
CLKDV	CLKOUT_FREQ_DV_HF_Min		3.00	3.00	3.00	MHz
	CLKOUT_FREQ_DV_HF_Max		300.00	280.00	240.00	MHz
CLKFX, CLKFX180	CLKOUT_FREQ_FX_HF_Min		210.00	210.00	210.00	MHz
	CLKOUT_FREQ_FX_HF_Max		350.00	320.00	270.00	MHz
Input Clocks (High Frequency Mode)						
CLKIN (using DLL outputs) ^(1,3,4)	CLKIN_FREQ_DLL_HF_Min		48.00	48.00	48.00	MHz
	CLKIN_FREQ_DLL_HF_Max		450.00	420.00	360.00	MHz
CLKIN (using CLKFX outputs) ^(2,3,4)	CLKIN_FRQ_FX_HF_Min		50.00	50.00	50.00	MHz
	CLKIN_FRQ_FX_HF_Max		350.00	320.00	270.00	MHz
PSCLK	PSCLK_FREQ_HF_Min		0.01	0.01	0.01	MHz
	PSCLK_FREQ_HF_Max		450.00	420.00	360.00	MHz

Notes:

1. "DLL outputs" is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. If both DLL and CLKFX outputs are used, follow the more restrictive specification.
3. If the CLKIN_DIVIDE_BY_2 attribute of the DCM is used, then double these values.
4. If the CLKIN_DIVIDE_BY_2 attribute of the DCM is used and CLKIN frequency > 400 MHz, CLKIN duty cycle must be within $\pm 5\%$ (45/55 to 55/45).

Table 4: Virtex-II Pin Definitions (Continued)

Pin Name	Direction	Description
PROG_B	Input	Active Low asynchronous reset to configuration logic. This pin has a permanent weak pull-up resistor.
DONE	Input/Output	DONE is a bidirectional signal with an optional internal pull-up resistor. As an output, this pin indicates completion of the configuration process. As an input, a Low level on DONE can be configured to delay the start-up sequence.
M2, M1, M0	Input	Configuration mode selection.
HSWAP_EN	Input	Enable I/O pull-ups during configuration.
TCK	Input	Boundary Scan Clock.
TDI	Input	Boundary Scan Data Input.
TDO	Output	Boundary Scan Data Output.
TMS	Input	Boundary Scan Mode Select.
PWRDWN_B	Input (unsupported)	Active Low power-down pin (unsupported). <i>Driving this pin Low can adversely affect device operation and configuration.</i> PWRDWN_B is internally pulled High, which is its default state. It does not require an external pull-up.
Other Pins		
DXN, DXP	N/A	Temperature-sensing diode pins (Anode: DXP, Cathode: DXN).
V _{BATT}	Input	Decryptor key memory backup supply. Connect V _{BATT} to V _{CCAUX} or GND if battery is not used.
RSVD	N/A	Reserved pin - do not connect.
V _{CCO}	Input	Power-supply pins for the output drivers (per bank).
V _{CCAUX}	Input	Power-supply pins for auxiliary circuits.
V _{CCINT}	Input	Power-supply pins for the internal core logic.
GND	Input	Ground.

Notes:

1. All dedicated pins (JTAG and configuration) are powered by V_{CCAUX} (independent of the bank V_{CCO} voltage).

Table 7: FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
5	IO_L06P_5	W6		
5	IO_L05N_5/VRP_5	V7		
5	IO_L05P_5/VRN_5	V6		
5	IO_L04N_5	AB5		
5	IO_L04P_5/VREF_5	AA5		
5	IO_L03N_5/D4/ALT_VRP_5	Y5		
5	IO_L03P_5/D5/ALT_VRN_5	W5		
5	IO_L02N_5/D6	AB4		
5	IO_L02P_5/D7	AA4		
5	IO_L01N_5/RDWR_B	Y4		
5	IO_L01P_5/CS_B	AA3		
6	IO_L01P_6	V5		
6	IO_L01N_6	U5		
6	IO_L02P_6/VRN_6	Y2		
6	IO_L02N_6/VRP_6	Y1		
6	IO_L03P_6	V4		
6	IO_L03N_6/VREF_6	V3		
6	IO_L04P_6	W2		
6	IO_L04N_6	W1		
6	IO_L06P_6	U4		
6	IO_L06N_6	U3		
6	IO_L19P_6	V2	NC	NC
6	IO_L19N_6	V1	NC	NC
6	IO_L21P_6	U2	NC	NC
6	IO_L21N_6/VREF_6	U1	NC	NC
6	IO_L22P_6	T5	NC	NC
6	IO_L22N_6	R5	NC	NC
6	IO_L24P_6	T4	NC	NC
6	IO_L24N_6	T3	NC	NC
6	IO_L43P_6	T2		
6	IO_L43N_6	T1		
6	IO_L45P_6	R4		
6	IO_L45N_6/VREF_6	R3		

Table 8: FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
2	IO_L96P_2	N23		
3	IO_L96N_3	N26		
3	IO_L96P_3	P26		
3	IO_L94N_3	P23		
3	IO_L94P_3	P22		
3	IO_L93N_3/VREF_3	P19		
3	IO_L93P_3	N19		
3	IO_L91N_3	P21		
3	IO_L91P_3	P20		
3	IO_L78N_3	R26	NC	
3	IO_L78P_3	R25	NC	
3	IO_L76N_3	R20	NC	
3	IO_L76P_3	R19	NC	
3	IO_L75N_3/VREF_3	R24	NC	
3	IO_L75P_3	R23	NC	
3	IO_L73N_3	R22	NC	
3	IO_L73P_3	R21	NC	
3	IO_L72N_3	T26		
3	IO_L72P_3	T25		
3	IO_L70N_3	T20		
3	IO_L70P_3	T19		
3	IO_L69N_3/VREF_3	T24		
3	IO_L69P_3	T23		
3	IO_L67N_3	T22		
3	IO_L67P_3	T21		
3	IO_L54N_3	U26		
3	IO_L54P_3	V26		
3	IO_L52N_3	U24		
3	IO_L52P_3	U23		
3	IO_L51N_3/VREF_3	U22		
3	IO_L51P_3	U21		
3	IO_L49N_3	V25		
3	IO_L49P_3	V24		
3	IO_L48N_3	V23		
3	IO_L48P_3	V22		
3	IO_L46N_3	W26		

Table 8: FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
NA	GND	L11		
NA	GND	L10		
NA	GND	K17		
NA	GND	K16		
NA	GND	K15		
NA	GND	K14		
NA	GND	K13		
NA	GND	K12		
NA	GND	K11		
NA	GND	K10		
NA	GND	F21		
NA	GND	F6		
NA	GND	E22		
NA	GND	E5		
NA	GND	D23		
NA	GND	D4		
NA	GND	C24		
NA	GND	C3		
NA	GND	B25		
NA	GND	B14		
NA	GND	B13		
NA	GND	B2		
NA	GND	A26		
NA	GND	A1		

Notes:

1. See Table 4 for an explanation of the signals available on this pin.

Table 9: BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
4	IO_L91P_4	AB14		
4	IO_L92N_4	V14		
4	IO_L92P_4	Y14		
4	IO_L93N_4	AB13		
4	IO_L93P_4	AC13		
4	IO_L94N_4/VREF_4	Y13		
4	IO_L94P_4	AA13		
4	IO_L95N_4/GCLK3S	V13		
4	IO_L95P_4/GCLK2P	W13		
4	IO_L96N_4/GCLK1S	U14		
4	IO_L96P_4/GCLK0P	U13		
5	IO_L96N_5/GCLK7S	AD12		
5	IO_L96P_5/GCLK6P	AD11		
5	IO_L95N_5/GCLK5S	AC12		
5	IO_L95P_5/GCLK4P	AB12		
5	IO_L94N_5	AA12		
5	IO_L94P_5/VREF_5	Y12		
5	IO_L93N_5	W12		
5	IO_L93P_5	V12		
5	IO_L92N_5	U12		
5	IO_L92P_5	U11		
5	IO_L91N_5	AB11		
5	IO_L91P_5/VREF_5	AA11		
5	IO_L73N_5	Y11	NC	NC
5	IO_L73P_5	V11	NC	NC
5	IO_L72N_5	AD10	NC	
5	IO_L72P_5	AD9	NC	
5	IO_L70N_5	AC10	NC	
5	IO_L70P_5	AB10	NC	
5	IO_L69N_5/VREF_5	Y10	NC	
5	IO_L69P_5	W10	NC	
5	IO_L67N_5	V10	NC	
5	IO_L67P_5	U10	NC	
5	IO_L54N_5	AC9		
5	IO_L54P_5	AB9		

Table 9: BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
7	IO_L46P_7	H2		
7	IO_L46N_7	G2		
7	IO_L45P_7/VREF_7	H3		
7	IO_L45N_7	H4		
7	IO_L43P_7	G3		
7	IO_L43N_7	G4		
7	IO_L24P_7	H5		
7	IO_L24N_7	H6		
7	IO_L22P_7	J6		
7	IO_L22N_7	J7		
7	IO_L21P_7/VREF_7	K7		
7	IO_L21N_7	K8		
7	IO_L19P_7	E1		
7	IO_L19N_7	E2		
7	IO_L06P_7	D2		
7	IO_L06N_7	D3		
7	IO_L04P_7	E3		
7	IO_L04N_7	E4		
7	IO_L03P_7/VREF_7	F4		
7	IO_L03N_7	F5		
7	IO_L02P_7/VRN_7	G5		
7	IO_L02N_7/VRP_7	G6		
7	IO_L01P_7	H7		
7	IO_L01N_7	J8		
0	VCCO_0	J12		
0	VCCO_0	J11		
0	VCCO_0	J10		
0	VCCO_0	F11		
0	VCCO_0	C6		
0	VCCO_0	B11		
1	VCCO_1	J15		
1	VCCO_1	J14		
1	VCCO_1	J13		
1	VCCO_1	F14		
1	VCCO_1	C19		

Table 10: BG728 BGA — XC2V3000

Bank	Pin Description	Pin Number
1	IO_L27N_1/VREF_1	F19
1	IO_L27P_1	G19
1	IO_L25N_1	J19
1	IO_L25P_1	J20
1	IO_L24N_1	C20
1	IO_L24P_1	C21
1	IO_L22N_1	D20
1	IO_L22P_1	E21
1	IO_L21N_1/VREF_1	E20
1	IO_L21P_1	F20
1	IO_L19N_1	A21
1	IO_L19P_1	B21
1	IO_L06N_1	A22
1	IO_L06P_1	B22
1	IO_L05N_1	C22
1	IO_L05P_1	C23
1	IO_L04N_1	D22
1	IO_L04P_1/VREF_1	E22
1	IO_L03N_1/VRP_1	A23
1	IO_L03P_1/VRN_1	B23
1	IO_L02N_1	A24
1	IO_L02P_1	B24
1	IO_L01N_1	A25
1	IO_L01P_1	B25
2	IO_L01N_2	C27
2	IO_L01P_2	D27
2	IO_L02N_2/VRP_2	D25
2	IO_L02P_2/VRN_2	D26
2	IO_L03N_2	E24
2	IO_L03P_2/VREF_2	E25
2	IO_L04N_2	E26
2	IO_L04P_2	E27
2	IO_L06N_2	F23
2	IO_L06P_2	F24
2	IO_L19N_2	F25

Table 10: BG728 BGA — XC2V3000

Bank	Pin Description	Pin Number
NA	VCCINT	K10
NA	GND	AG27
NA	GND	AG26
NA	GND	AG14
NA	GND	AG2
NA	GND	AG1
NA	GND	AF27
NA	GND	AF26
NA	GND	AF20
NA	GND	AF8
NA	GND	AF2
NA	GND	AF1
NA	GND	AE25
NA	GND	AE3
NA	GND	AD24
NA	GND	AD14
NA	GND	AD4
NA	GND	AC23
NA	GND	AC17
NA	GND	AC11
NA	GND	AC5
NA	GND	AB22
NA	GND	AB6
NA	GND	AA21
NA	GND	AA7
NA	GND	Y26
NA	GND	Y20
NA	GND	Y8
NA	GND	Y2
NA	GND	W14
NA	GND	U23
NA	GND	U5
NA	GND	T16
NA	GND	T15
NA	GND	T14
NA	GND	T13

Table 11: FF896 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
4	IO_L73P_4	AJ12	NC	NC
4	IO_L74N_4	AE13	NC	NC
4	IO_L74P_4	AE14	NC	NC
4	IO_L75N_4	AF13	NC	NC
4	IO_L75P_4/VREF_4	AG13	NC	NC
4	IO_L76N_4	AK13	NC	NC
4	IO_L76P_4	AK12	NC	NC
4	IO_L77N_4	AB14	NC	NC
4	IO_L77P_4	AB15	NC	NC
4	IO_L78N_4	AF15	NC	NC
4	IO_L78P_4	AF14	NC	NC
4	IO_L91N_4/VREF_4	AJ14		
4	IO_L91P_4	AJ15		
4	IO_L92N_4	AC14		
4	IO_L92P_4	AC15		
4	IO_L93N_4	AG15		
4	IO_L93P_4	AG14		
4	IO_L94N_4/VREF_4	AK14		
4	IO_L94P_4	AK15		
4	IO_L95N_4/GCLK3S	AD15		
4	IO_L95P_4/GCLK2P	AE15		
4	IO_L96N_4/GCLK1S	AH14		
4	IO_L96P_4/GCLK0P	AH15		
5	IO_L96N_5/GCLK7S	AH16		
5	IO_L96P_5/GCLK6P	AH17		
5	IO_L95N_5/GCLK5S	AE16		
5	IO_L95P_5/GCLK4P	AD16		
5	IO_L94N_5	AJ16		
5	IO_L94P_5/VREF_5	AJ17		
5	IO_L93N_5	AG17		
5	IO_L93P_5	AG16		
5	IO_L92N_5	AC16		
5	IO_L92P_5	AC17		
5	IO_L91N_5	AK17		
5	IO_L91P_5/VREF_5	AK18		
5	IO_L78N_5	AF17	NC	NC

Table 11: FF896 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
5	IO_L78P_5	AF16	NC	NC
5	IO_L77N_5	AB16	NC	NC
5	IO_L77P_5	AB17	NC	NC
5	IO_L76N_5	AJ19	NC	NC
5	IO_L76P_5	AJ18	NC	NC
5	IO_L75N_5/VREF_5	AG18	NC	NC
5	IO_L75P_5	AF18	NC	NC
5	IO_L74N_5	AE17	NC	NC
5	IO_L74P_5	AE18	NC	NC
5	IO_L73N_5	AK20	NC	NC
5	IO_L73P_5	AK19	NC	NC
5	IO_L72N_5	AH20	NC	
5	IO_L72P_5	AH19	NC	
5	IO_L71N_5	AD18	NC	
5	IO_L71P_5	AD19	NC	
5	IO_L70N_5	AJ21	NC	
5	IO_L70P_5	AJ20	NC	
5	IO_L69N_5/VREF_5	AG19	NC	
5	IO_L69P_5	AG20	NC	
5	IO_L68N_5	AC18	NC	
5	IO_L68P_5	AC19	NC	
5	IO_L67N_5	AK22	NC	
5	IO_L67P_5	AK21	NC	
5	IO_L54N_5	AF21		
5	IO_L54P_5	AF20		
5	IO_L53N_5	AH22		
5	IO_L53P_5	AH23		
5	IO_L52N_5	AG22		
5	IO_L52P_5	AG21		
5	IO_L51N_5/VREF_5	AF22		
5	IO_L51P_5	AF23		
5	IO_L50N_5	AE19		
5	IO_L50P_5	AE20		
5	IO_L49N_5	AJ23		
5	IO_L49P_5	AJ22		
5	IO_L24N_5	AF24		
5	IO_L24P_5	AG23		

Table 11: FF896 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
NA	GND	AC1		
NA	GND	AA28		
NA	GND	AA3		
NA	GND	W26		
NA	GND	W19		
NA	GND	W18		
NA	GND	W17		
NA	GND	W16		
NA	GND	W15		
NA	GND	W14		
NA	GND	W13		
NA	GND	W12		
NA	GND	W5		
NA	GND	V19		
NA	GND	V18		
NA	GND	V17		
NA	GND	V16		
NA	GND	V15		
NA	GND	V14		
NA	GND	V13		
NA	GND	V12		
NA	GND	U24		
NA	GND	U19		
NA	GND	U18		
NA	GND	U17		
NA	GND	U16		
NA	GND	U15		
NA	GND	U14		
NA	GND	U13		
NA	GND	U12		
NA	GND	U7		
NA	GND	T19		
NA	GND	T18		
NA	GND	T17		
NA	GND	T16		
NA	GND	T15		
NA	GND	T14		

Table 12: FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
5	IO_L50P_5	AG22	
5	IO_L49N_5	AN29	
5	IO_L49P_5	AN28	
5	IO_L30N_5	AK24	
5	IO_L30P_5	AK25	
5	IO_L29N_5	AH23	
5	IO_L29P_5	AH22	
5	IO_L28N_5	AP31	
5	IO_L28P_5	AP30	
5	IO_L27N_5/VREF_5	AH24	
5	IO_L27P_5	AH25	
5	IO_L26N_5	AF22	
5	IO_L26P_5	AF23	
5	IO_L25N_5	AM27	
5	IO_L25P_5	AM26	
5	IO_L24N_5	AL27	
5	IO_L24P_5	AL26	
5	IO_L23N_5	AH26	
5	IO_L23P_5	AJ25	
5	IO_L22N_5	AN31	
5	IO_L22P_5	AN30	
5	IO_L21N_5/VREF_5	AK26	
5	IO_L21P_5	AK27	
5	IO_L20N_5	AG23	
5	IO_L20P_5	AF24	
5	IO_L19N_5	AM33	
5	IO_L19P_5	AN32	
5	IO_L06N_5	AJ27	
5	IO_L06P_5	AJ26	
5	IO_L05N_5/VRP_5	AE22	
5	IO_L05P_5/VRN_5	AE23	
5	IO_L04N_5	AM28	
5	IO_L04P_5/VREF_5	AM29	
5	IO_L03N_5/D4/ALT_VRP_5	AK28	
5	IO_L03P_5/D5/ALT_VRN_5	AL29	
5	IO_L02N_5/D6	AG24	

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
1	IO_L09N_1/VREF_1	G9	NC	
1	IO_L09P_1	G10	NC	
1	IO_L08N_1	K13	NC	
1	IO_L08P_1	K12	NC	
1	IO_L07N_1	A4	NC	
1	IO_L07P_1	A5	NC	
1	IO_L06N_1	F8		
1	IO_L06P_1	E8		
1	IO_L05N_1	J11		
1	IO_L05P_1	K11		
1	IO_L04N_1	C5		
1	IO_L04P_1/VREF_1	C6		
1	IO_L03N_1/VRP_1	D6		
1	IO_L03P_1/VRN_1	D7		
1	IO_L02N_1	H10		
1	IO_L02P_1	J10		
1	IO_L01N_1	C4		
1	IO_L01P_1	B4		
2	IO_L01N_2	E3		
2	IO_L01P_2	D2		
2	IO_L02N_2/VRP_2	L13		
2	IO_L02P_2/VRN_2	M13		
2	IO_L03N_2	F4		
2	IO_L03P_2/VREF_2	E4		
2	IO_L04N_2	E1		
2	IO_L04P_2	D1		
2	IO_L05N_2	L12		
2	IO_L05P_2	M11		
2	IO_L06N_2	G6		
2	IO_L06P_2	F5		
2	IO_L07N_2	F2	NC	
2	IO_L07P_2	E2	NC	
2	IO_L08N_2	M12	NC	
2	IO_L08P_2	N12	NC	
2	IO_L09N_2	H6	NC	

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
2	IO_L33P_2/VREF_2	J4	NC	
2	IO_L34N_2	K2	NC	
2	IO_L34P_2	J2	NC	
2	IO_L35N_2	P12	NC	
2	IO_L35P_2	R12	NC	
2	IO_L36N_2	M6	NC	
2	IO_L36P_2	L6	NC	
2	IO_L43N_2	L3		
2	IO_L43P_2	K3		
2	IO_L44N_2	N9		
2	IO_L44P_2	P9		
2	IO_L45N_2	M4		
2	IO_L45P_2/VREF_2	L4		
2	IO_L46N_2	L1		
2	IO_L46P_2	K1		
2	IO_L47N_2	P10		
2	IO_L47P_2	R10		
2	IO_L48N_2	N5		
2	IO_L48P_2	M5		
2	IO_L49N_2	N3		
2	IO_L49P_2	M3		
2	IO_L50N_2	N8		
2	IO_L50P_2	P8		
2	IO_L51N_2	T11		
2	IO_L51P_2/VREF_2	R11		
2	IO_L52N_2	N2		
2	IO_L52P_2	M2		
2	IO_L53N_2	T12		
2	IO_L53P_2	U12		
2	IO_L54N_2	P6		
2	IO_L54P_2	N6		
2	IO_L55N_2	N1		
2	IO_L55P_2	M1		
2	IO_L56N_2	R8		
2	IO_L56P_2	T8		
2	IO_L57N_2	R7		

Table 14: BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000

Bank	Pin Description	Pin Number	No Connect in XC2V2000
3	IO_L03P_3	AD7	
3	IO_L02N_3/VRP_3	AE6	
3	IO_L02P_3/VRN_3	AF5	
3	IO_L01N_3	AH2	
3	IO_L01P_3	AH3	
4	IO_L01N_4/BUSY/DOUT ⁽¹⁾	AD9	
4	IO_L01P_4/INIT_B	AD10	
4	IO_L02N_4/D0/DIN ⁽¹⁾	AF7	
4	IO_L02P_4/D1	AG7	
4	IO_L03N_4/D2/ALT_VRP_4	AK3	
4	IO_L03P_4/D3/ALT_VRN_4	AJ5	
4	IO_L04N_4/VREF_4	AE8	
4	IO_L04P_4	AF8	
4	IO_L05N_4/VRP_4	AK4	
4	IO_L05P_4/VRN_4	AK5	
4	IO_L06N_4	AH6	
4	IO_L06P_4	AH7	
4	IO_L19N_4	AC10	
4	IO_L19P_4	AC11	
4	IO_L20N_4	AE9	
4	IO_L20P_4	AE10	
4	IO_L21N_4	AL4	
4	IO_L21P_4/VREF_4	AL5	
4	IO_L22N_4	AB12	
4	IO_L22P_4	AB13	
4	IO_L23N_4	AJ6	
4	IO_L23P_4	AJ8	
4	IO_L24N_4	AK6	
4	IO_L24P_4	AK7	
4	IO_L25N_4	AG8	NC
4	IO_L25P_4	AG9	NC
4	IO_L26N_4	AF9	NC
4	IO_L26P_4	AF11	NC
4	IO_L27N_4	AH8	NC
4	IO_L27P_4/VREF_4	AH9	NC
4	IO_L28N_4	AD11	NC
4	IO_L28P_4	AD12	NC

Table 14: BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000

Bank	Pin Description	Pin Number	No Connect in XC2V2000
7	IO_L53N_7	K30	
7	IO_L52P_7	L28	
7	IO_L52N_7	J28	
7	IO_L51P_7/VREF_7	M24	
7	IO_L51N_7	L24	
7	IO_L50P_7	L29	
7	IO_L50N_7	K29	
7	IO_L49P_7	M25	
7	IO_L49N_7	L25	
7	IO_L48P_7	L26	
7	IO_L48N_7	J26	
7	IO_L47P_7	J31	
7	IO_L47N_7	H31	
7	IO_L46P_7	J29	
7	IO_L46N_7	H29	
7	IO_L45P_7/VREF_7	M22	
7	IO_L45N_7	L22	
7	IO_L44P_7	J30	
7	IO_L44N_7	G30	
7	IO_L43P_7	K27	
7	IO_L43N_7	J27	
7	IO_L27P_7/VREF_7	L23	NC
7	IO_L27N_7	K23	NC
7	IO_L25P_7	G31	NC
7	IO_L25N_7	F31	NC
7	IO_L24P_7	F30	
7	IO_L24N_7	E30	
7	IO_L23P_7	K25	
7	IO_L23N_7	J25	
7	IO_L22P_7	H28	
7	IO_L22N_7	G28	
7	IO_L21P_7/VREF_7	H27	
7	IO_L21N_7	G27	
7	IO_L20P_7	K24	
7	IO_L20N_7	J24	
7	IO_L19P_7	E31	
7	IO_L19N_7	D31	
7	IO_L06P_7	F28	