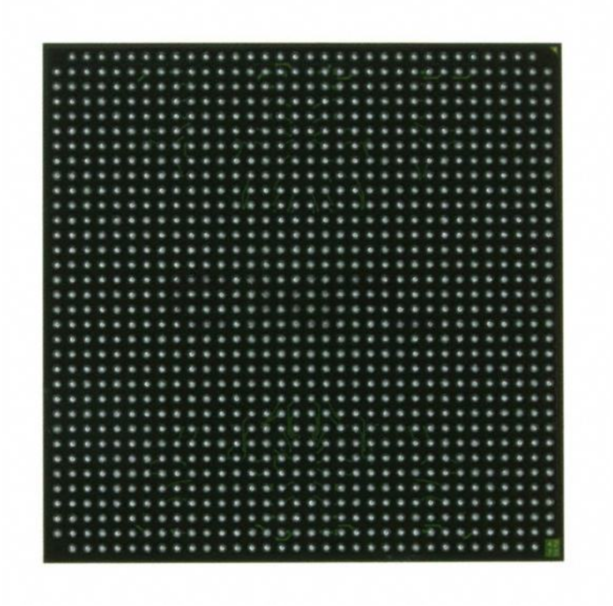
AMD Xilinx - XC2V3000-5FF1152I Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	3584
Number of Logic Elements/Cells	-
Total RAM Bits	1769472
Number of I/O	720
Number of Gates	3000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v3000-5ff1152i

Digitally Controlled Impedance (DCI)

Today's chip output signals with fast edge rates require termination to prevent reflections and maintain signal integrity. High pin count packages (especially ball grid arrays) can not accommodate external termination resistors.

Virtex-II XCITE DCI provides controlled impedance drivers and on-chip termination for single-ended and differential I/Os. This eliminates the need for external resistors, and improves signal integrity. The DCI feature can be used on any IOB by selecting one of the DCI I/O standards.

When applied to inputs, DCI provides input parallel termination. When applied to outputs, DCI provides controlled impedance drivers (series termination) or output parallel termination.

DCI operates independently on each I/O bank. When a DCI I/O standard is used in a particular I/O bank, external reference resistors must be connected to two dual-function pins on the bank. These resistors, voltage reference of N transistor (VRN) and the voltage reference of P transistor (VRP) are shown in Figure 9.

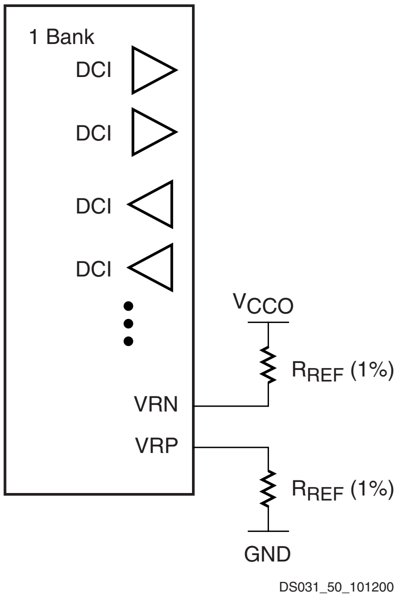

Figure 9: **DCI in a Virtex-II Bank**

When used with a terminated I/O standard, the value of resistors are specified by the standard (typically 50Ω). When used with a controlled impedance driver, the resistors set the output impedance of the driver within the specified range (25Ω to 100Ω). For all series and parallel terminations listed in Table 6 and Table 7, the reference resistors must have the same value for any given bank. One percent resistors are recommended.

The DCI system adjusts the I/O impedance to match the two external reference resistors, or half of the reference resistors, and compensates for impedance changes due to voltage and/or temperature fluctuations. The adjustment is done by turning parallel transistors in the IOB on or off.

Controlled Impedance Drivers (Series Term.)

DCI can be used to provide a buffer with a controlled output impedance. It is desirable for this output impedance to match the transmission line impedance (Z_0). Virtex-II input buffers also support LVDCI and LVDCI_DV2 I/O standards.

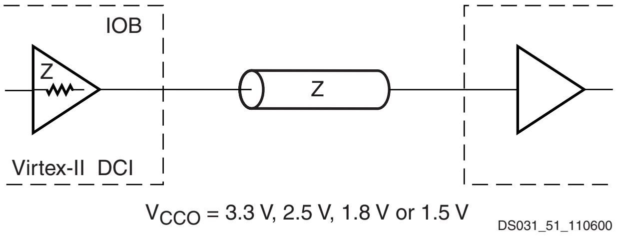

Figure 10: **Internal Series Termination**

Table 6: **SelectI/O-Ultra Controlled Impedance Buffers**

V_{CCO}	DCI	DCI Half Impedance
3.3 V	LVDCI_33	LVDCI_DV2_33
2.5 V	LVDCI_25	LVDCI_DV2_25
1.8 V	LVDCI_18	LVDCI_DV2_18
1.5 V	LVDCI_15	LVDCI_DV2_15

Controlled Impedance Drivers (Parallel)

DCI also provides on-chip termination for SSTL3, SSTL2, HSTL (Class I, II, III, or IV), and GTL/GTLP receivers or transmitters on bidirectional lines.

Table 7 and Table 8 list the on-chip parallel terminations available in Virtex-II devices. V_{CCO} must be set according to Table 3. Note that there is a V_{CCO} requirement for GTL_DCI and GTLP_DCI, due to the on-chip termination resistor.

Table 7: **SelectI/O-Ultra Buffers With On-Chip Parallel Termination**

I/O Standard Description	IOSTANDARD Attribute	
	External Termination	On-Chip Termination
SSTL3 Class I	SSTL3_I	SSTL3_I_DCI(1)
SSTL3 Class II	SSTL3_II	SSTL3_II_DCI(1)
SSTL2 Class I	SSTL2_I	SSTL2_I_DCI(1)
SSTL2 Class II	SSTL2_II	SSTL2_II_DCI(1)
HSTL Class I	HSTL_I	HSTL_I_DCI
HSTL Class II	HSTL_II	HSTL_II_DCI
HSTL Class III	HSTL_III	HSTL_III_DCI
HSTL Class IV	HSTL_IV	HSTL_IV_DCI
GTL	GTL	GTL_DCI
GTLP	GTLP	GTLP_DCI

Notes:

1. SSTL-compatible

Each block SelectRAM cell is a fully synchronous memory, as illustrated in Figure 30. The two ports have independent inputs and outputs and are independently clocked.

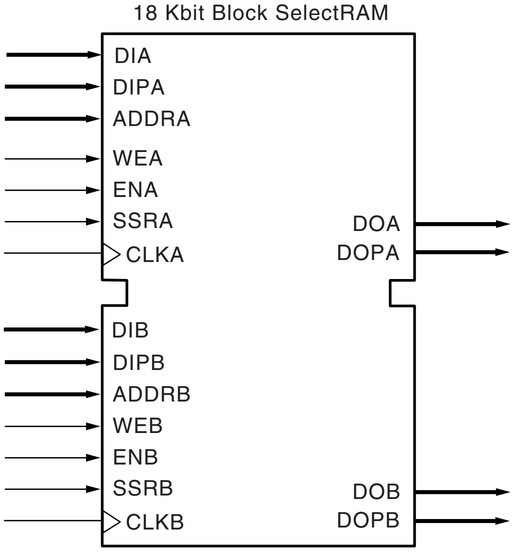

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Figure 30: **18 Kbit Block SelectRAM in Dual-Port Mode**

Port Aspect Ratios

Table 16 shows the depth and the width aspect ratios for the 18 Kbit block SelectRAM. Virtex-II block SelectRAM also includes dedicated routing resources to provide an efficient interface with CLBs, block SelectRAM, and multipliers.

Table 16: **18** Kbit **Block SelectRAM Port Aspect Ratio**

Width	Depth	Address Bus	Data Bus	Parity Bus
1	16,384	ADDR[13:0]	DATA[0]	N/A
2	8,192	ADDR[12:0]	DATA[1:0]	N/A
4	4,096	ADDR[11:0]	DATA[3:0]	N/A
9	2,048	ADDR[10:0]	DATA[7:0]	Parity[0]
18	1,024	ADDR[9:0]	DATA[15:0]	Parity[1:0]
36	512	ADDR[8:0]	DATA[31:0]	Parity[3:0]

Read/Write Operations

The Virtex-II block SelectRAM read operation is fully synchronous. An address is presented, and the read operation is enabled by control signals WEA and WEB in addition to ENA or ENB. Then, depending on clock polarity, a rising or falling clock edge causes the stored data to be loaded into output registers.

The write operation is also fully synchronous. Data and address are presented, and the write operation is enabled by control signals WEA or WEB in addition to ENA or ENB. Then, again depending on the clock input mode, a rising or falling clock edge causes the data to be loaded into the memory cell addressed.

A write operation performs a simultaneous read operation. Three different options are available, selected by configuration:

1. **"WRITE_FIRST"**

   The "WRITE_FIRST" option is a transparent mode. The same clock edge that writes the data input (DI) into the memory also transfers DI into the output registers DO as shown in Figure 31.

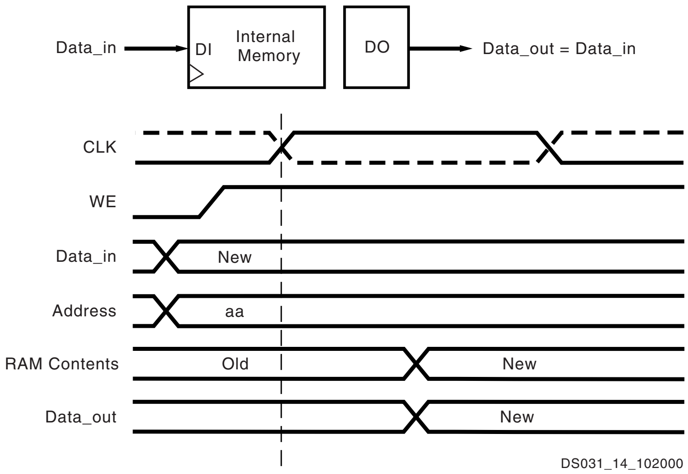

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Figure 31: **WRITE_FIRST Mode**

2. **"READ_FIRST"**

   The "READ_FIRST" option is a read-before-write mode.

   The same clock edge that writes data input (DI) into the memory also transfers the prior content of the memory cell addressed into the data output registers DO, as shown in Figure 32.

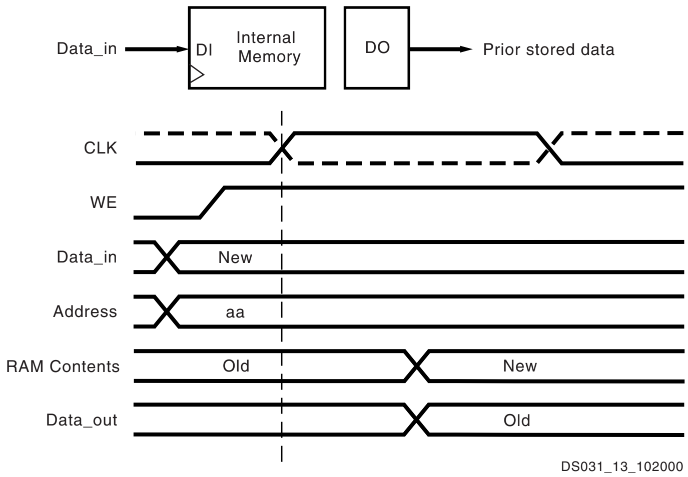

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Figure 32: **READ_FIRST Mode**

Virtex-II Switching Characteristics

Switching characteristics in this document are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Note that Virtex-II Performance Characteristics, page 7 are subject to these guidelines as well. Each designation is defined as follows:

Advance: These speed files are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These speed files are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production: These speed files are released once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 13 correlates the current status of each Virtex-II device with a corresponding speed grade designation.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the Xilinx static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-II devices.

IOB Input Switching Characteristics

Input delays associated with the pad are specified for LVTTL levels. For other standards, adjust the delays with the values shown in IOB Input Switching Characteristics Standard Adjustments, page 11.

Table 13: **Virtex-II Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC2V40			-6, -5, -4
XC2V80			-6, -5, -4
XC2V250			-6, -5, -4
XC2V500			-6, -5, -4
XC2V1000			-6, -5, -4
XC2V1500			-6, -5, -4
XC2V2000			-6, -5, -4
XC2V3000			-6, -5, -4
XC2V4000			-6, -5, -4
XC2V6000			-6, -5, -4
XC2V8000			-5, -4

Table 14: **IOB Input Switching Characteristics**

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
Propagation Delays						
Pad to I output, no delay	T_{IOPI}	All	0.69	0.76	0.88	ns, Max
Pad to I output, with delay	T_{IOPID}	XC2V40	1.92	2.11	2.43	ns, Max
		XC2V80	1.92	2.11	2.43	ns, Max
		XC2V250	1.92	2.11	2.43	ns, Max
		XC2V500	1.92	2.11	2.43	ns, Max
		XC2V1000	1.92	2.11	2.43	ns, Max
		XC2V1500	1.92	2.11	2.43	ns, Max
		XC2V2000	1.92	2.11	2.43	ns, Max
		XC2V3000	1.97	2.16	2.49	ns, Max
		XC2V4000	1.97	2.16	2.49	ns, Max
		XC2V6000	2.10	2.31	2.66	ns, Max
		XC2V8000		2.31	2.66	ns, Max

Miscellaneous Timing Parameters

Table 42: **Miscellaneous Timing Parameters**

Description	Symbol	Constraints F_{CLKIN}	Speed Grade			Units
			-6	**-5**	**-4**	
Time Required to Achieve LOCK						
Using DLL outputs(1)	LOCK_DLL					
	LOCK_DLL_60	> 60MHz	20.0	20.0	20.0	µs
	LOCK_DLL_50_60	50 - 60 MHz	25.0	25.0	25.0	µs
	LOCK_DLL_40_50	40 - 50 MHz	50.0	50.0	50.0	µs
	LOCK_DLL_30_40	30 - 40 MHz	90.0	90.0	90.0	µs
	LOCK_DLL_24_30	24 - 30 MHz	120.0	120.0	120.0	µs
Using CLKFX outputs	LOCK_FX_MIN		10.0	10.0	10.0	ms
	LOCK_FX_MAX		10.0	10.0	10.0	ms
Additional lock time with fine-phase shifting	LOCK_DLL_FINE_SHIFT		50.0	50.0	50.0	µs
Fine-Phase Shifting						
Absolute shifting range	FINE_SHIFT_RANGE		10.0	10.0	10.0	ns
Delay Lines						
Tap delay resolution	DCM_TAP_MIN		30.0	30.0	30.0	ps
	DCM_TAP_MAX		60.0	60.0	60.0	ps

Notes:
1. "DLL outputs" is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. Specification also applies to PSCLK.

Frequency Synthesis

Table 43: **Frequency Synthesis**

Attribute	Min	Max
CLKFX_MULTIPLY	2	32
CLKFX_DIVIDE	1	32

Parameter Cross Reference

Table 44: **Parameter Cross Reference**

Libraries Guide	Data Sheet
DLL_CLKOUT_{MIN|MAX}_LF	CLKOUT_FREQ_{1X|2X|DV}_LF
DFS_CLKOUT_{MIN|MAX}_LF	CLKOUT_FREQ_FX_LF
DLL_CLKIN_{MIN|MAX}_LF	CLKIN_FREQ_DLL_LF
DFS_CLKIN_{MIN|MAX}_LF	CLKIN_FREQ_FX_LF
DLL_CLKOUT_{MIN|MAX}_HF	CLKOUT_FREQ_{1X|DV}_HF
DFS_CLKOUT_{MIN|MAX}_HF	CLKOUT_FREQ_FX_HF
DLL_CLKIN_{MIN|MAX}_HF	CLKIN_FREQ_DLL_HF
DFS_CLKIN_{MIN|MAX}_HF	CLKIN_FREQ_FX_HF

Pin Definitions

Table 4 provides a description of each pin type listed in Virtex-II pinout tables.

Table 4: **Virtex-II Pin Definitions**

Pin Name	Direction	Description
User I/O Pins		
IO_LXXY_#	Input/Output/ Bidirectional	All user I/O pins are capable of differential signalling and can implement LVDS, ULVDS, BLVDS, LVPECL, or LDT pairs. Each user I/O is labeled "**IO_LXXY_#**", where: **IO** indicates a user I/O pin. **LXXY** indicates a differential pair, with **XX** a unique pair in the bank and **Y = P/N** for the positive and negative sides of the differential pair. **#** indicates the bank number (0 through 7)
Dual-Function Pins		
IO_LXXY_#/ZZZ		The dual-function pins are labelled "**IO_LXXY_#/ZZZ**", where **ZZZ** can be one of the following pins: Per Bank - **VRP, VRN,** or **VREF** Globally - **GCLKX(S/P), BUSY/DOUT, INIT_B, D0/DIN – D7, RDWR_B,** or **CS_B**
With /ZZZ:		
D0/DIN, D1, D2, D3, D4, D5, D6, D7	Input/Output	• *In* SelectMAP *mode,* D0 through D7 are configuration data pins. These pins become user I/Os after configuration, unless the SelectMAP port is retained. • *In bit-serial modes,* DIN (D0) is the single-data input. This pin becomes a user I/O after configuration.
CS_B	Input	In SelectMAP mode, this is the active-low Chip Select signal. The pin becomes a user I/O after configuration, unless the SelectMAP port is retained.
RDWR_B	Input	In SelectMAP mode, this is the active-low Write Enable signal. The pin becomes a user I/O after configuration, unless the SelectMAP port is retained.
BUSY/DOUT	Output	• *In* SelectMAP *mode,* BUSY controls the rate at which configuration data is loaded. The pin becomes a user I/O after configuration, unless the SelectMAP port is retained. • *In bit-serial modes,* DOUT provides preamble and configuration data to downstream devices in a daisy-chain. The pin becomes a user I/O after configuration.
INIT_B	Bidirectional (open-drain)	When Low, this pin indicates that the configuration memory is being cleared. When held Low, the start of configuration is delayed. During configuration, a Low on this output indicates that a configuration data error has occurred. The pin becomes a user I/O after configuration.
GCLKx (S/P)	Input/Output	These are clock input pins that connect to Global Clock Buffers. These pins become regular user I/Os when not needed for clocks.
VRP	Input	This pin is for the DCI voltage reference resistor of P transistor (per bank).
VRN	Input	This pin is for the DCI voltage reference resistor of N transistor (per bank).
ALT_VRP	Input	This is the alternative pin for the DCI voltage reference resistor of P transistor.
ALT_VRN	Input	This is the alternative pin for the DCI voltage reference resistor of N transistor.
V_{REF}	Input	These are input threshold voltage pins. They become user I/Os when an external threshold voltage is not needed (per bank).
Dedicated Pins(1)		
CCLK	Input/Output	Configuration clock. Output in Master mode or Input in Slave mode.

Table 4: **Virtex-II Pin Definitions *(Continued)***

Pin Name	Direction	Description
PROG_B	Input	Active Low asynchronous reset to configuration logic. This pin has a permanent weak pull-up resistor.
DONE	Input/Output	DONE is a bidirectional signal with an optional internal pull-up resistor. As an output, this pin indicates completion of the configuration process. As an input, a Low level on DONE can be configured to delay the start-up sequence.
M2, M1, M0	Input	Configuration mode selection.
HSWAP_EN	Input	Enable I/O pull-ups during configuration.
TCK	Input	Boundary Scan Clock.
TDI	Input	Boundary Scan Data Input.
TDO	Output	Boundary Scan Data Output.
TMS	Input	Boundary Scan Mode Select.
PWRDWN_B	Input *(unsupported)*	Active Low power-down pin (unsupported). *Driving this pin Low can adversely affect device operation and configuration.* PWRDWN_B is internally pulled High, which is its default state. It does not require an external pull-up.
Other Pins		
DXN, DXP	N/A	Temperature-sensing diode pins (Anode: DXP, Cathode: DXN).
V_{BATT}	Input	Decryptor key memory backup supply. Connect V_{BATT} to V_{CCAUX} or GND if battery is not used.
RSVD	N/A	Reserved pin - do not connect.
V_{CCO}	Input	Power-supply pins for the output drivers (per bank).
V_{CCAUX}	Input	Power-supply pins for auxiliary circuits.
V_{CCINT}	Input	Power-supply pins for the internal core logic.
GND	Input	Ground.

Notes:

1. All dedicated pins (JTAG and configuration) are powered by V_{CCAUX} (independent of the bank V_{CCO} voltage).

FG456/FGG456 Fine-Pitch BGA Package

As shown in Table 7, XC2V250, XC2V500, and XC2V1000 Virtex-II devices are available in the FG456/FGG456 fine-pitch BGA package. Pins in the XC2V250, XC2V500, and XC2V1000 devices are the same, except for the pin differences in the XC2V250 and XC2V500 devices shown in the No Connect columns. Following this table are the FG456/FGG456 Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
0	IO_L01N_0	B4		
0	IO_L01P_0	A4		
0	IO_L02N_0	C4		
0	IO_L02P_0	C5		
0	IO_L03N_0/VRP_0	B5		
0	IO_L03P_0/VRN_0	A5		
0	IO_L04N_0/VREF_0	D6		
0	IO_L04P_0	C6		
0	IO_L05N_0	B6		
0	IO_L05P_0	A6		
0	IO_L06N_0	E7		
0	IO_L06P_0	E8		
0	IO_L21N_0	D7	NC	NC
0	IO_L21P_0/VREF_0	C7	NC	NC
0	IO_L22N_0	B7	NC	NC
0	IO_L22P_0	A7	NC	NC
0	IO_L24N_0	D8	NC	NC
0	IO_L24P_0	C8	NC	NC
0	IO_L49N_0	B8	NC	
0	IO_L49P_0	A8	NC	
0	IO_L51N_0	E9	NC	
0	IO_L51P_0/VREF_0	F9	NC	
0	IO_L52N_0	D9	NC	
0	IO_L52P_0	C9	NC	
0	IO_L54N_0	B9	NC	
0	IO_L54P_0	A9	NC	
0	IO_L91N_0/VREF_0	E10		
0	IO_L91P_0	F10		
0	IO_L92N_0	D10		
0	IO_L92P_0	C10		

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
6	IO_L52N_6	U1		
6	IO_L54P_6	U7		
6	IO_L54N_6	T7		
6	IO_L67P_6	U4		
6	IO_L67N_6	U3		
6	IO_L69P_6	U6		
6	IO_L69N_6/VREF_6	U5		
6	IO_L70P_6	T5		
6	IO_L70N_6	T6		
6	IO_L72P_6	T8		
6	IO_L72N_6	R8		
6	IO_L73P_6	T2	NC	
6	IO_L73N_6	T1	NC	
6	IO_L75P_6	T4	NC	
6	IO_L75N_6/VREF_6	T3	NC	
6	IO_L76P_6	R6	NC	
6	IO_L76N_6	R5	NC	
6	IO_L78P_6	R4	NC	
6	IO_L78N_6	R3	NC	
6	IO_L91P_6	R2		
6	IO_L91N_6	R1		
6	IO_L93P_6	R7		
6	IO_L93N_6/VREF_6	P7		
6	IO_L94P_6	P6		
6	IO_L94N_6	P5		
6	IO_L96P_6	P4		
6	IO_L96N_6	P3		
7	IO_L96P_7	P1		
7	IO_L96N_7	N1		
7	IO_L94P_7	N4		
7	IO_L94N_7	N5		
7	IO_L93P_7/VREF_7	N6		
7	IO_L93N_7	N7		
7	IO_L91P_7	P8		
7	IO_L91N_7	N8		
7	IO_L78P_7	M1	NC	

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
3	VCCO_3	V19		
3	VCCO_3	U25		
3	VCCO_3	U19		
3	VCCO_3	T18		
3	VCCO_3	R18		
3	VCCO_3	P18		
4	VCCO_4	AE20		
4	VCCO_4	AE17		
4	VCCO_4	W18		
4	VCCO_4	W17		
4	VCCO_4	V16		
4	VCCO_4	V15		
4	VCCO_4	V14		
5	VCCO_5	AE10		
5	VCCO_5	AE7		
5	VCCO_5	W10		
5	VCCO_5	W9		
5	VCCO_5	V13		
5	VCCO_5	V12		
5	VCCO_5	V11		
6	VCCO_6	Y2		
6	VCCO_6	V8		
6	VCCO_6	U8		
6	VCCO_6	U2		
6	VCCO_6	T9		
6	VCCO_6	R9		
6	VCCO_6	P9		
7	VCCO_7	N9		
7	VCCO_7	M9		
7	VCCO_7	L9		
7	VCCO_7	K8		
7	VCCO_7	K2		
7	VCCO_7	J8		
7	VCCO_7	G2		
NA	CCLK	AB21		
NA	PROG_B	C4		

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
NA	VCCINT	H19		
NA	VCCINT	H8		
NA	GND	AF26		
NA	GND	AF1		
NA	GND	AE25		
NA	GND	AE14		
NA	GND	AE13		
NA	GND	AE2		
NA	GND	AD24		
NA	GND	AD3		
NA	GND	AC23		
NA	GND	AC4		
NA	GND	AB22		
NA	GND	AB5		
NA	GND	AA21		
NA	GND	AA6		
NA	GND	U17		
NA	GND	U16		
NA	GND	U15		
NA	GND	U14		
NA	GND	U13		
NA	GND	U12		
NA	GND	U11		
NA	GND	U10		
NA	GND	T17		
NA	GND	T16		
NA	GND	T15		
NA	GND	T14		
NA	GND	T13		
NA	GND	T12		
NA	GND	T11		
NA	GND	T10		
NA	GND	R17		
NA	GND	R16		
NA	GND	R15		
NA	GND	R14		
NA	GND	R13		

BG575/BGG575 Standard BGA Package

As shown in Table 9, XC2V1000, XC2V1500, and XC2V2000 Virtex-II devices are available in the BG575/BGG575 BGA package. Pins in the XC2V1000, XC2V1500, and XC2V2000 devices are the same, except for the pin differences in the XC2V1000 and XC2V1500 devices shown in the No Connect columns. Following this table are the BG575/BGG575 Standard BGA Package Specifications (1.27mm pitch).

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
0	IO_L01N_0	A3		
0	IO_L01P_0	A4		
0	IO_L02N_0	D5		
0	IO_L02P_0	C5		
0	IO_L03N_0/VRP_0	E6		
0	IO_L03P_0/VRN_0	D6		
0	IO_L04N_0/VREF_0	F7		
0	IO_L04P_0	E7		
0	IO_L05N_0	G8		
0	IO_L05P_0	H9		
0	IO_L06N_0	A5		
0	IO_L06P_0	A6		
0	IO_L19N_0	B5		
0	IO_L19P_0	B6		
0	IO_L21N_0	D7		
0	IO_L21P_0/VREF_0	C7		
0	IO_L22N_0	F8		
0	IO_L22P_0	E8		
0	IO_L24N_0	G9		
0	IO_L24P_0	F9		
0	IO_L49N_0	G10		
0	IO_L49P_0	H10		
0	IO_L51N_0	B7		
0	IO_L51P_0/VREF_0	B8		
0	IO_L52N_0	D8		
0	IO_L52P_0	C8		
0	IO_L54N_0	E9		
0	IO_L54P_0	D9		
0	IO_L67N_0	A8	NC	
0	IO_L67P_0	A9	NC	
0	IO_L69N_0	C9	NC	

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
0	IO_L69P_0/VREF_0	B9	NC	
0	IO_L70N_0	F10	NC	
0	IO_L70P_0	E10	NC	
0	IO_L72N_0	A10	NC	
0	IO_L72P_0	A11	NC	
0	IO_L73N_0	C10	NC	NC
0	IO_L73P_0	B10	NC	NC
0	IO_L91N_0/VREF_0	D11		
0	IO_L91P_0	C11		
0	IO_L92N_0	G11		
0	IO_L92P_0	E11		
0	IO_L93N_0	C12		
0	IO_L93P_0	B12		
0	IO_L94N_0/VREF_0	E12		
0	IO_L94P_0	D12		
0	IO_L95N_0/GCLK7P	G12		
0	IO_L95P_0/GCLK6S	F12		
0	IO_L96N_0/GCLK5P	H11		
0	IO_L96P_0/GCLK4S	H12		
1	IO_L96N_1/GCLK3P	A13		
1	IO_L96P_1/GCLK2S	A14		
1	IO_L95N_1/GCLK1P	B13		
1	IO_L95P_1/GCLK0S	C13		
1	IO_L94N_1	D13		
1	IO_L94P_1/VREF_1	E13		
1	IO_L93N_1	F13		
1	IO_L93P_1	G13		
1	IO_L92N_1	H13		
1	IO_L92P_1	H14		
1	IO_L91N_1	C14		
1	IO_L91P_1/VREF_1	D14		
1	IO_L73N_1	E14	NC	NC
1	IO_L73P_1	G14	NC	NC
1	IO_L72N_1	A15	NC	
1	IO_L72P_1	A16	NC	

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
NA	GND	Y5		
NA	GND	W19		
NA	GND	W6		
NA	GND	V24		
NA	GND	V18		
NA	GND	V7		
NA	GND	V1		
NA	GND	R21		
NA	GND	R4		
NA	GND	P14		
NA	GND	P13		
NA	GND	P12		
NA	GND	P11		
NA	GND	N14		
NA	GND	N13		
NA	GND	N12		
NA	GND	N11		
NA	GND	M14		
NA	GND	M13		
NA	GND	M12		
NA	GND	M11		
NA	GND	L14		
NA	GND	L13		
NA	GND	L12		
NA	GND	L11		
NA	GND	K21		
NA	GND	K4		
NA	GND	G24		
NA	GND	G18		
NA	GND	G7		
NA	GND	G1		
NA	GND	F19		
NA	GND	F6		
NA	GND	E20		
NA	GND	E5		
NA	GND	D21		

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
5	IO_L52N_5	AC10
5	IO_L52P_5	AB10
5	IO_L51N_5/VREF_5	Y9
5	IO_L51P_5	Y10
5	IO_L49N_5	AG9
5	IO_L49P_5	AG8
5	IO_L30N_5	AF9
5	IO_L30P_5	AE9
5	IO_L28N_5	AD9
5	IO_L28P_5	AC9
5	IO_L27N_5/VREF_5	AB9
5	IO_L27P_5	AA9
5	IO_L25N_5	AE8
5	IO_L25P_5	AE7
5	IO_L24N_5	AD8
5	IO_L24P_5	AC8
5	IO_L22N_5	AB8
5	IO_L22P_5	AA8
5	IO_L21N_5/VREF_5	AG7
5	IO_L21P_5	AF7
5	IO_L19N_5	AC7
5	IO_L19P_5	AB7
5	IO_L06N_5	AG6
5	IO_L06P_5	AF6
5	IO_L05N_5/VRP_5	AE6
5	IO_L05P_5/VRN_5	AD6
5	IO_L04N_5	AG5
5	IO_L04P_5/VREF_5	AF5
5	IO_L03N_5/D4/ALT_VRP_5	AE5
5	IO_L03P_5/D5/ALT_VRN_5	AD5
5	IO_L02N_5/D6	AG4
5	IO_L02P_5/D7	AF4
5	IO_L01N_5/RDWR_B	AG3
5	IO_L01P_5/CS_B	AF3
6	IO_L01P_6	AE1

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
2	VCCO_2	L10		
2	VCCO_2	L9		
2	VCCO_2	K9		
2	VCCO_2	E2		
3	VCCO_3	AF2		
3	VCCO_3	AA9		
3	VCCO_3	Y10		
3	VCCO_3	Y9		
3	VCCO_3	W10		
3	VCCO_3	W9		
3	VCCO_3	V10		
3	VCCO_3	V9		
3	VCCO_3	V3		
3	VCCO_3	U10		
3	VCCO_3	T10		
4	VCCO_4	AJ5		
4	VCCO_4	AH13		
4	VCCO_4	AB13		
4	VCCO_4	AB12		
4	VCCO_4	AB11		
4	VCCO_4	AB10		
4	VCCO_4	AA15		
4	VCCO_4	AA14		
4	VCCO_4	AA13		
4	VCCO_4	AA12		
4	VCCO_4	AA11		
5	VCCO_5	AJ26		
5	VCCO_5	AH18		
5	VCCO_5	AB21		
5	VCCO_5	AB20		
5	VCCO_5	AB19		
5	VCCO_5	AB18		
5	VCCO_5	AA20		
5	VCCO_5	AA19		
5	VCCO_5	AA18		
5	VCCO_5	AA17		
5	VCCO_5	AA16		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
1	IO_L93N_1	E19		
1	IO_L93P_1	E20		
1	IO_L92N_1	J19		
1	IO_L92P_1	J18		
1	IO_L91N_1	A18		
1	IO_L91P_1/VREF_1	A19		
1	IO_L84N_1	D18		
1	IO_L84P_1	D19		
1	IO_L83N_1	K19		
1	IO_L83P_1	K18		
1	IO_L82N_1	B18		
1	IO_L82P_1	B19		
1	IO_L81N_1/VREF_1	G18		
1	IO_L81P_1	G19		
1	IO_L80N_1	E18		
1	IO_L80P_1	E17		
1	IO_L79N_1	A16		
1	IO_L79P_1	A17		
1	IO_L78N_1	F17		
1	IO_L78P_1	F18		
1	IO_L77N_1	L19		
1	IO_L77P_1	L18		
1	IO_L76N_1	B16		
1	IO_L76P_1	B17		
1	IO_L75N_1/VREF_1	G16		
1	IO_L75P_1	G17		
1	IO_L74N_1	M19		
1	IO_L74P_1	M18		
1	IO_L73N_1	C16		
1	IO_L73P_1	C17		
1	IO_L72N_1	D15		
1	IO_L72P_1	D16		
1	IO_L71N_1	J17		
1	IO_L71P_1	J16		
1	IO_L70N_1	A14		
1	IO_L70P_1	A15		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
1	IO_L09N_1/VREF_1	G9	NC	
1	IO_L09P_1	G10	NC	
1	IO_L08N_1	K13	NC	
1	IO_L08P_1	K12	NC	
1	IO_L07N_1	A4	NC	
1	IO_L07P_1	A5	NC	
1	IO_L06N_1	F8		
1	IO_L06P_1	E8		
1	IO_L05N_1	J11		
1	IO_L05P_1	K11		
1	IO_L04N_1	C5		
1	IO_L04P_1/VREF_1	C6		
1	IO_L03N_1/VRP_1	D6		
1	IO_L03P_1/VRN_1	D7		
1	IO_L02N_1	H10		
1	IO_L02P_1	J10		
1	IO_L01N_1	C4		
1	IO_L01P_1	B4		
2	IO_L01N_2	E3		
2	IO_L01P_2	D2		
2	IO_L02N_2/VRP_2	L13		
2	IO_L02P_2/VRN_2	M13		
2	IO_L03N_2	F4		
2	IO_L03P_2/VREF_2	E4		
2	IO_L04N_2	E1		
2	IO_L04P_2	D1		
2	IO_L05N_2	L12		
2	IO_L05P_2	M11		
2	IO_L06N_2	G6		
2	IO_L06P_2	F5		
2	IO_L07N_2	F2	NC	
2	IO_L07P_2	E2	NC	
2	IO_L08N_2	M12	NC	
2	IO_L08P_2	N12	NC	
2	IO_L09N_2	H6	NC	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	GND	U4		
NA	GND	T23		
NA	GND	T22		
NA	GND	T21		
NA	GND	T20		
NA	GND	T19		
NA	GND	T18		
NA	GND	T17		
NA	GND	P35		
NA	GND	P5		
NA	GND	L38		
NA	GND	L29		
NA	GND	L11		
NA	GND	L2		
NA	GND	K30		
NA	GND	K20		
NA	GND	K10		
NA	GND	J31		
NA	GND	J9		
NA	GND	H32		
NA	GND	H23		
NA	GND	H17		
NA	GND	H8		
NA	GND	G33		
NA	GND	G20		
NA	GND	G7		
NA	GND	F34		
NA	GND	F6		
NA	GND	E35		
NA	GND	E26		
NA	GND	E14		
NA	GND	E5		
NA	GND	D36		
NA	GND	D23		
NA	GND	D20		
NA	GND	D17		

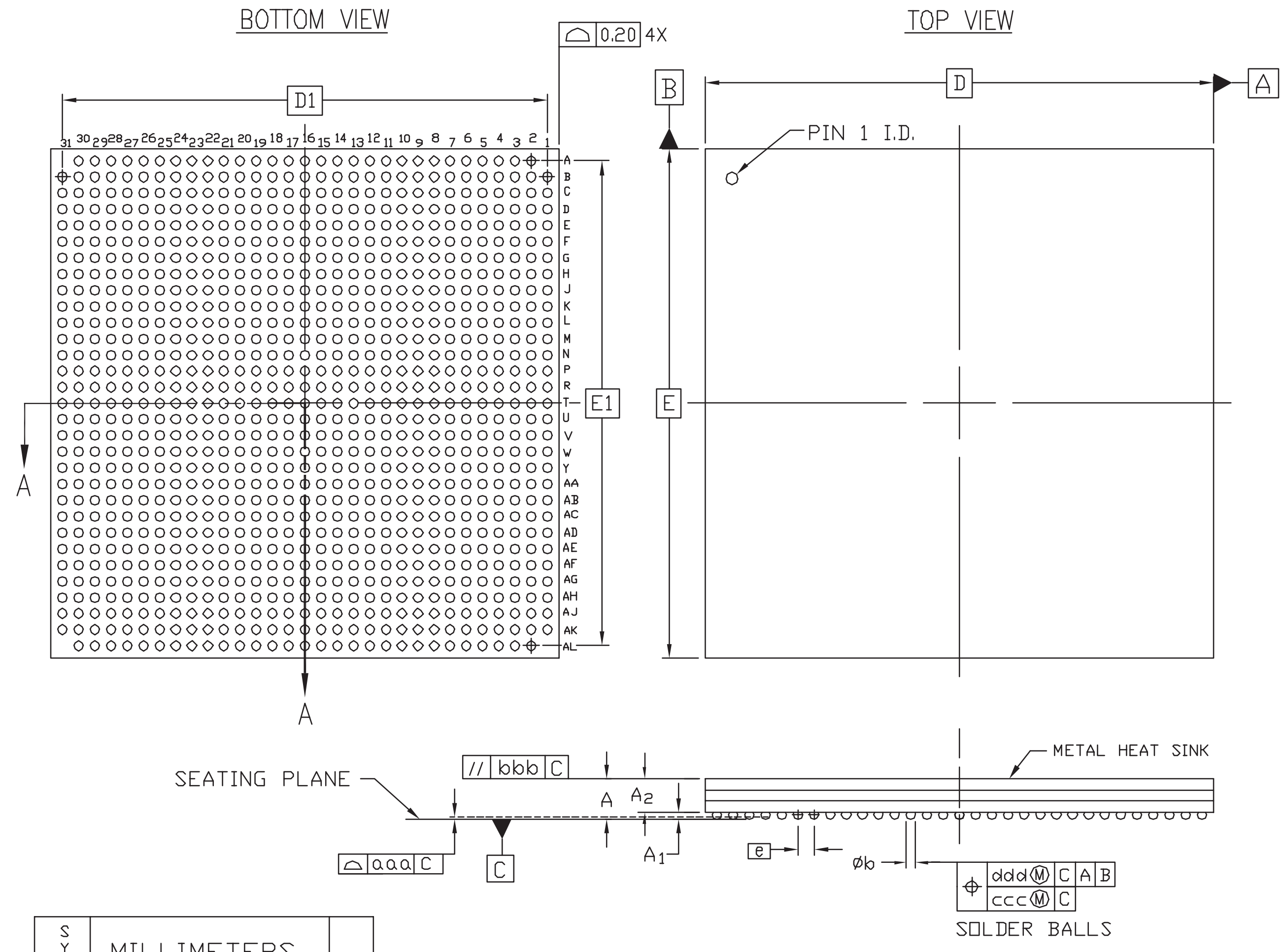
BF957 Flip-Chip BGA Package

As shown in Table 14, XC2V2000, XC2V3000, XC2V4000, and XC2V6000 Virtex-II devices are available in the BF957 package. Pins in each of these devices are the same, except for the pin differences in the XC2V2000 device shown in the No Connect column. Following this table are the BF957 Flip-Chip BGA Package Specifications (1.27mm pitch).

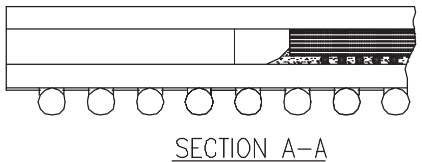
Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
0	IO_L01N_0	H23	
0	IO_L01P_0	H22	
0	IO_L02N_0	G24	
0	IO_L02P_0	E25	
0	IO_L03N_0/VRP_0	B29	
0	IO_L03P_0/VRN_0	C27	
0	IO_L04N_0/VREF_0	F24	
0	IO_L04P_0	F23	
0	IO_L05N_0	D26	
0	IO_L05P_0	D25	
0	IO_L06N_0	A28	
0	IO_L06P_0	A27	
0	IO_L19N_0	J22	
0	IO_L19P_0	J21	
0	IO_L20N_0	G23	
0	IO_L20P_0	G22	
0	IO_L21N_0	B27	
0	IO_L21P_0/VREF_0	B26	
0	IO_L22N_0	K20	
0	IO_L22P_0	K19	
0	IO_L23N_0	C26	
0	IO_L23P_0	C24	
0	IO_L24N_0	D24	
0	IO_L24P_0	D23	
0	IO_L25N_0	E24	NC
0	IO_L25P_0	E23	NC
0	IO_L26N_0	G21	NC
0	IO_L26P_0	G20	NC
0	IO_L27N_0	A26	NC
0	IO_L27P_0/VREF_0	A25	NC
0	IO_L29N_0	H21	NC
0	IO_L29P_0	H20	NC
0	IO_L30N_0	B25	NC
0	IO_L30P_0	B23	NC

BF957 Flip-Chip BGA Package Specifications (1.27mm pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	—	3.25	3.50	
A_1	0.50	0.60	0.70	
A_2	—	—	2.80	
A_3	0.20	—	—	
D/E	40.00 BSC			
D_1/E_1	38.10 REF.			
e	1.27 BSC			
Øb	0.60	0.75	0.90	
aaa	—	—	0.20	
bbb	—	—	0.25	
ccc	—	—	0.15	
ddd	—	—	0.30	
M	31			



SECTION A–A
(NOT TO SCALE)

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–BAU–1 (DEPOPULATED)

Figure 10: **BF957 Flip-Chip BGA Package Specifications**