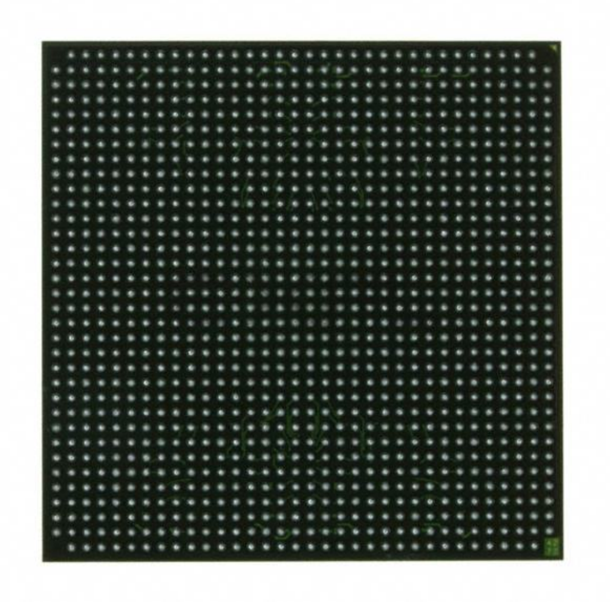

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3584
Number of Logic Elements/Cells	-
Total RAM Bits	1769472
Number of I/O	720
Number of Gates	3000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v3000-5ffg1152c

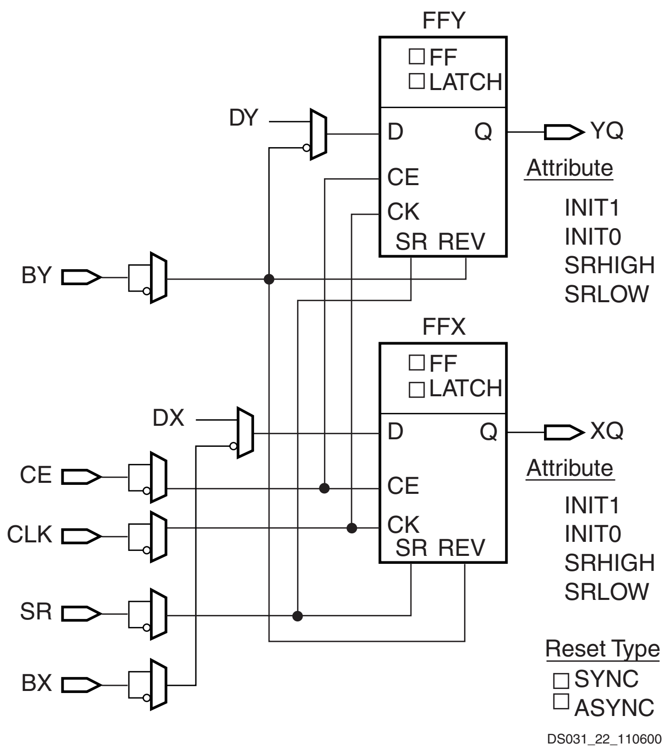


Figure 17: **Register / Latch Configuration in a Slice**

The set and reset functionality of a register or a latch can be configured as follows:

- No set or reset
- Synchronous set
- Synchronous reset
- Synchronous set and reset
- Asynchronous set (preset)
- Asynchronous reset (clear)
- Asynchronous set and reset (preset and clear)

The synchronous reset has precedence over a set, and an asynchronous clear has precedence over a preset.

Distributed SelectRAM Memory

Each function generator (LUT) can implement a 16 x 1-bit synchronous RAM resource called a distributed SelectRAM element. The SelectRAM elements are configurable within a CLB to implement the following:

- Single-Port 16 x 8 bit RAM
- Single-Port 32 x 4 bit RAM
- Single-Port 64 x 2 bit RAM
- Single-Port 128 x 1 bit RAM
- Dual-Port 16 x 4 bit RAM
- Dual-Port 32 x 2 bit RAM
- Dual-Port 64 x 1 bit RAM

Distributed SelectRAM memory modules are synchronous (write) resources. The combinatorial read access time is extremely fast, while the synchronous write simplifies high-speed designs. A synchronous read can be implemented with a storage element in the same slice. The distributed SelectRAM memory and the storage element share the same clock input. A Write Enable (WE) input is active High, and is driven by the SR input.

Table 9 shows the number of LUTs (2 per slice) occupied by each distributed SelectRAM configuration.

Table 9: **Distributed SelectRAM Configurations**

RAM	Number of LUTs
16 x 1S	1
16 x 1D	2
32 x 1S	2
32 x 1D	4
64 x 1S	4
64 x 1D	8
128 x 1S	8

Notes:

1. S = single-port configuration; D = dual-port configuration

For single-port configurations, distributed SelectRAM memory has one address port for synchronous writes and asynchronous reads.

For dual-port configurations, distributed SelectRAM memory has one port for synchronous writes and asynchronous reads and another port for asynchronous reads. The function generator (LUT) has separated read address inputs (A1, A2, A3, A4) and write address inputs (WG1/WF1, WG2/WF2, WG3/WF3, WG4/WF4).

In single-port mode, read and write addresses share the same address bus. In dual-port mode, one function generator (R/W port) is connected with shared read and write addresses. The second function generator has the A inputs (read) connected to the second read-only port address and the W inputs (write) shared with the first read/write port address.

Shift Registers

Each function generator can also be configured as a 16-bit shift register. The write operation is synchronous with a clock input (CLK) and an optional clock enable, as shown in Figure 21. A dynamic read access is performed through the 4-bit address bus, A[3:0]. The configurable 16-bit shift register cannot be set or reset. The read is asynchronous, however the storage element or flip-flop is available to implement a synchronous read. The storage element should always be used with a constant address. For example, when building an 8-bit shift register and configuring the addresses to point to the 7th bit, the 8th bit can be the flip-flop. The overall system performance is improved by using the superior clock-to-out of the flip-flops.

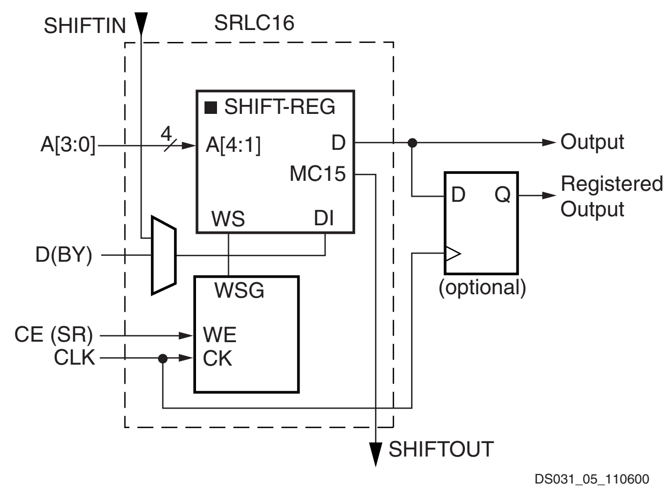


Figure 21: **Shift Register Configurations**

An additional dedicated connection between shift registers allows connecting the last bit of one shift register to the first bit of the next, without using the ordinary LUT output. (See Figure 22.) Longer shift registers can be built with dynamic access to any bit in the chain. The shift register chaining and the MUXF5, MUXF6, and MUXF7 multiplexers allow up to a 128-bit shift register with addressable access to be implemented in one CLB.

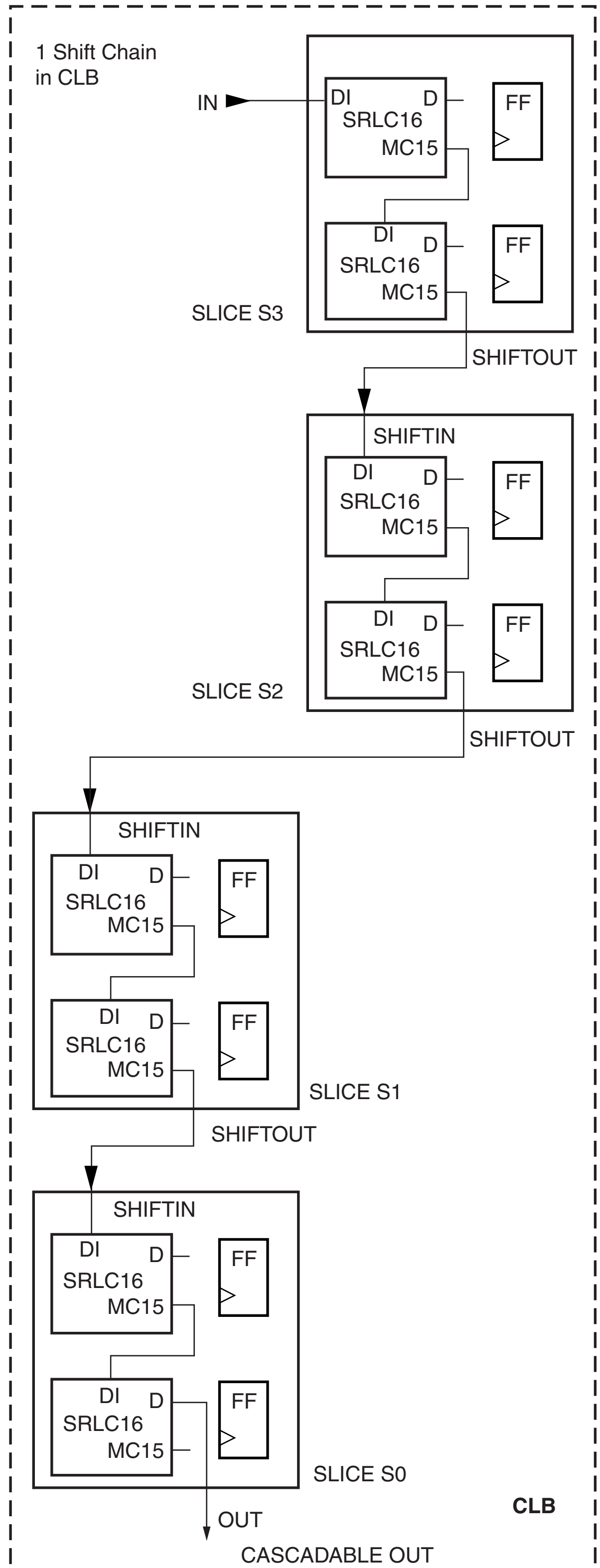


Figure 22: **Cascadable Shift Register**

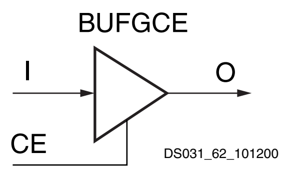


Figure 42: **Virtex-II BUFGCE Function**

If the CE input is inactive (Low) prior to the incoming rising clock edge, the following clock pulse does not pass through the clock buffer, and the output stays Low. Any level change of CE during the incoming clock High time has no effect. CE must not change during a short setup window just prior to the rising clock edge on the BUFGCE input I. Violating this setup time requirement can result in an undefined runt pulse output.

BUFGMUX

BUFGMUX can switch between two unrelated, even asynchronous clocks. Basically, a Low on S selects the I0 input, a High on S selects the I1 input. Switching from one clock to the other is done in such a way that the output High and Low time is never shorter than the shortest High or Low time of either input clock. As long as the presently selected clock is High, any level change of S has no effect .

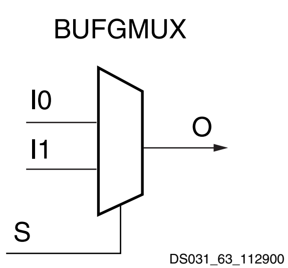


Figure 43: **Virtex-II BUFGMUX Function**

If the presently selected clock is Low while S changes, or if it goes Low after S has changed, the output is kept Low until the other ("to-be-selected") clock has made a transition from High to Low. At that instant, the new clock starts driving the output.

The two clock inputs can be asynchronous with regard to each other, and the S input can change at any time, except for a short setup time prior to the rising edge of the presently selected clock (I0 or I1). Violating this setup time requirement can result in an undefined runt pulse output.

All Virtex-II devices have 16 global clock multiplexer buffers.

Figure 44 shows a switchover from I0 to I1.

- The current clock is CLK0.
- S is activated High.
- If CLK0 is currently High, the multiplexer waits for CLK0 to go Low.
- Once CLK0 is Low, the multiplexer output stays Low until CLK1 transitions High to Low.
- When CLK1 transitions from High to Low, the output switches to CLK1.
- No glitches or short pulses can appear on the output.

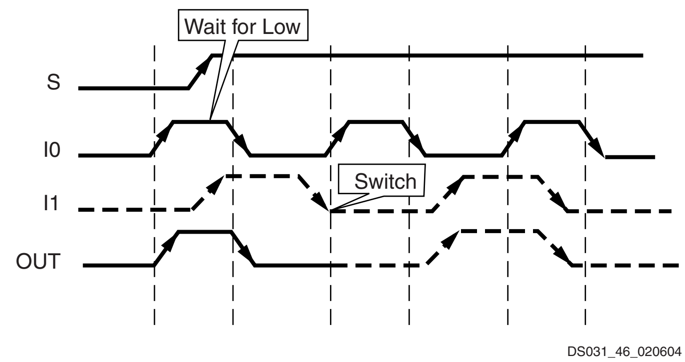


Figure 44: **Clock Multiplexer Waveform Diagram**

Local Clocking

In addition to global clocks, there are local clock resources in the Virtex-II devices. There are more than 72 local clocks in the Virtex-II family. These resources can be used for many different applications, including but not limited to memory interfaces. For example, even using only the left and right I/O banks, Virtex-II FPGAs can support up to 50 local clocks for DDR SDRAM. These interfaces can operate beyond 200 MHz on Virtex-II devices.

Digital Clock Manager (DCM)

The Virtex-II DCM offers a wide range of powerful clock management features.

- **Clock De-skew**: The DCM generates new system clocks (either internally or externally to the FPGA), which are phase-aligned to the input clock, thus eliminating clock distribution delays.
- **Frequency Synthesis**: The DCM generates a wide range of output clock frequencies, performing very flexible clock multiplication and division.
- **Phase Shifting**: The DCM provides both coarse phase shifting and fine-grained phase shifting with dynamic phase shift control.

The DCM utilizes fully digital delay lines allowing robust high-precision control of clock phase and frequency. It also utilizes fully digital feedback systems, operating dynamically to compensate for temperature and voltage variations during operation.

Up to four of the nine DCM clock outputs can drive inputs to global clock buffers or global clock multiplexer buffers simultaneously (see Figure 45). All DCM clock outputs can simultaneously drive general routing resources, including routes to output buffers.

The Virtex-II implementation process is comprised of Synthesis, translation, mapping, place and route, and configuration file generation. While the tools can be run individually, many designers choose to run the entire implementation process with the click of a button. To assist those who prefer to script their design flows, Xilinx provides Xflow, an automated single command line process.

Design Verification

In addition to conventional design verification using static timing analysis or simulation techniques, Xilinx offers powerful in-circuit debugging techniques using ChipScope ILA (Integrated Logic Analysis). The reconfigurable nature of Xilinx FPGAs means that designs can be verified in real time without the need for extensive sets of software simulation vectors.

For simulation, the system extracts post-layout timing information from the design database, and back-annotates this information into the netlist for use by the simulator. The back annotation features a variety of patented Xilinx techniques, resulting in the industry's most powerful simulation flows. Alternatively, timing-critical portions of a design can be verified using the Xilinx static timing analyzer or a third party static timing analysis tool like Synopsys Prime Time™, by exporting timing data in the STAMP data format.

For in-circuit debugging, ChipScope ILA enables designers to analyze the real-time behavior of a device while operating at full system speeds. Logic analysis commands and captured data are transferred between the ChipScope software and ILA cores within the Virtex-II FPGA, using industry standard JTAG protocols. These JTAG transactions are driven over an optional download cable (MultiLINX or JTAG), connecting the Virtex device in the target system to a PC or workstation.

ChipScope ILA was designed to look and feel like a logic analyzer, making it easy to begin debugging a design immediately. Modifications to the desired logic analysis can be downloaded directly into the system in a matter of minutes.

Other Unique Features of Virtex-II Design Flow

Xilinx design flows feature a number of unique capabilities. Among these are efficient incremental HDL design flows; a robust capability that is enabled by Xilinx exclusive hierarchical floorplanning capabilities. Another powerful design capability only available in the Xilinx design flow is "Modular Design", part of the Xilinx suite of team design tools, which enables autonomous design, implementation, and verification of design modules.

Incremental Synthesis

Xilinx unique hierarchical floorplanning capabilities enable designers to create a programmable logic design by isolating design changes within one hierarchical "logic block", and perform synthesis, verification and implementation processes on that specific logic block. By preserving the logic in unchanged portions of a design, Xilinx incremental design makes the high-density design process more efficient.

Xilinx hierarchical floorplanning capabilities can be specified using the high-level floorplanner or a preferred RTL floorplanner (see the Xilinx web site for a list of supported EDA partners). When used in conjunction with one of the EDA partners' floorplanners, higher performance results can be achieved, as many synthesis tools use this more predictable detailed physical implementation information to establish more aggressive and accurate timing estimates when performing their logic optimizations.

Modular Design

Xilinx innovative modular design capabilities take the incremental design process one step further by enabling the designer to delegate responsibility for completing the design, synthesis, verification, and implementation of a hierarchical "logic block" to an arbitrary number of designers - assigning a specific region within the target FPGA for exclusive use by each of the team members.

This team design capability enables an autonomous approach to design modules, changing the hand-off point to the lead designer or integrator from "my module works in simulation" to "my module works in the FPGA". This unique design methodology also leverages the Xilinx hierarchical floorplanning capabilities and enables the Xilinx (or EDA partner) floorplanner to manage the efficient implementation of very high-density FPGAs.

Extended LVDS DC Specifications (LVDSEXT_33 & LVDSEXT_25)

Table 9: **Extended LVDS DC Specifications**

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}			3.3 or 2.5		V
Output High voltage for Q and $\overline{Q}$	V_{OH}	R_T = 100 Ω across Q and $\overline{Q}$ signals			1.785	V
Output Low voltage for Q and $\overline{Q}$	V_{OL}	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.705			V
Differential output voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{ODIFF}	R_T = 100 Ω across Q and $\overline{Q}$ signals	440		820	mV
Output common-mode voltage	V_{OCM}	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.200	1.375	V
Differential input voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{IDIFF}	Common-mode input voltage = 1.25 V	100	350	N/A	mV
Input common-mode voltage	V_{ICM}	Differential input voltage = ±350 mV	0.2	1.25	V_{CCO} – 0.5	V

LVPECL DC Specifications

These values are valid when driving a 100 Ω differential load only, i.e., a 100 Ω resistor between the two receiver pins. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. Table 10 summarizes the DC output specifications of LVPECL. For more information on using LVPECL, see the *Virtex-II User Guide*.

Table 10: **LVPECL DC Specifications**

DC Parameter	Min	Max	Min	Max	Min	Max	Units
V_{CCO}	3.0		3.3		3.6		V
V_{OH}	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{OL}	0.96	1.27	1.06	1.43	1.30	1.57	V
V_{IH}	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	0.86	2.125	0.86	2.125	0.86	2.125	V
Differential Input Voltage	0.3	–	0.3	–	0.3	–	V

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 18 shows the test setup parameters used for measuring Input standard adjustments (see Table 15, page 11).

Table 18: **Input Delay Measurement Methodology**

Description	IOSTANDARD Attribute	V_L (1,2)	V_H (1,2)	V_{MEAS} (1,4,5)	V_{REF} (1,3,5)
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL	0	3.0	1.4	–
LVCMOS (Low-Voltage CMOS), 3.3V	LVCMOS33	0	3.3	1.65	–
LVCMOS, 2.5V	LVCMOS25	0	2.5	1.25	–
LVCMOS, 1.8V	LVCMOS18	0	1.8	0.9	–
LVCMOS, 1.5V	LVCMOS15	0	1.5	0.75	–
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3	Per PCI Specification			–
PCI, 66 MHz, 3.3V	PCI66_3	Per PCI Specification			–
PCI-X, 133 MHz, 3.3V	PCIX	Per PCI-X Specification			–
GTL (Gunning Transceiver Logic)	GTL	$V_{REF} - 0.2$	$V_{REF} + 0.2$	V_{REF}	0.80
GTL Plus	GTLP	$V_{REF} - 0.2$	$V_{REF} + 0.2$	V_{REF}	1.0
HSTL (High-Speed Transceiver Logic), Class I & II	HSTL_I, HSTL_II	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.75
HSTL, Class III & IV	HSTL_III, HSTL_IV	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
HSTL, Class III & IV, 1.8V	HSTL_III_18, HSTL_IV_18	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	1.08
SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V	SSTL3_I, SSTL3_II	$V_{REF} - 1.00$	$V_{REF} + 1.00$	V_{REF}	1.5
SSTL, Class I & II, 2.5V	SSTL2_I, SSTL2_II	$V_{REF} - 0.75$	$V_{REF} + 0.75$	V_{REF}	1.25
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
AGP-2X/AGP (Accelerated Graphics Port)	AGP	$V_{REF} - (0.2 \times V_{CCO})$	$V_{REF} + (0.2 \times V_{CCO})$	V_{REF}	AGP Spec
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	1.2 – 0.125	1.2 + 0.125	1.2	
LVDS, 3.3V	LVDS_33	1.2 – 0.125	1.2 + 0.125	1.2	
LVDSEXT (LVDS Extended Mode), 2.5V	LVDSEXT_25	1.2 – 0.125	1.2 + 0.125	1.2	
LVDSEXT, 3.3V	LVDSEXT_33	1.2 – 0.125	1.2 + 0.125	1.2	
ULVDS (Ultra LVDS), 2.5V	ULVDS_25	0.6 – 0.125	0.6 + 0.125	0.6	
LDT (HyperTransport), 2.5V	LDT_25	0.6 – 0.125	0.6 + 0.125	0.6	
LVPECL (Low-Voltage Positive Electron-Coupled Logic), 3.3V	LVPECL_33	1.6 – 0.3	1.6 + 0.3	1.6	

Notes:
1. Input delay measurement methodology parameters for LVDCI and HSLVDCI are the same as for LVCMOS standards of the same voltage. Parameters for all other DCI standards are the same as for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H.
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical. See **Virtex-II Platform FPGA User Guide** for min/max specifications.
4. Input voltage level from which measurement starts.
5. Note that this is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 1.

Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. (See ***Virtex-II Platform FPGA User Guide*** for details.) The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setup shown in Figure 1.

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. (IBIS models can be found on the web at **http://support.xilinx.com/support/sw_ibis.htm**.) Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 19.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. The increase or decrease in delay should be added to or subtracted from the I/O Output Standard Adjustment value (Table 17) to yield the actual worst-case propagation delay (clock-to-input) of the PCB trace.

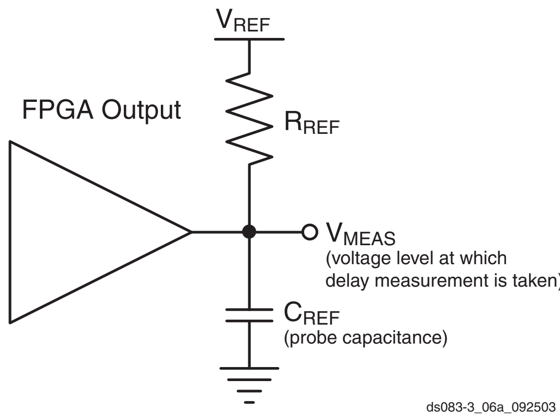


Figure 1: **Generalized Test Setup**

Table 19: **Output Delay Measurement Methodology**

Description	IOSTANDARD Attribute	R_{REF} (Ω)	C_{REF}(1) (pF)	V_{MEAS} (V)	V_{REF} (V)
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL (all)	1M	0	1.4	0
LVCMOS (Low-Voltage CMOS), 3.3V	LVCMOS33	1M	0	1.65	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3 (rising edge)	25	10(2)	0.94	0
	PCI33_3 (falling edge)	25	10(2)	2.03	3.3
PCI, 66 MHz, 3.3V	PCI66_3 (rising edge)	25	10(2)	0.94	0
	PCI66_3 (falling edge)	25	10(2)	2.03	3.3
PCI-X, 133 MHz, 3.3V	PCIX (rising edge)	25	10(3)	0.94	
	PCIX (falling edge	25	10(3)	2.03	3.3
GTL (Gunning Transceiver Logic)	GTL	25	0	0.8	1.2
GTL Plus	GTLP	25	0	1.0	1.5
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class III	HSTL_III	50	0	0.9	1.5
HSTL, Class IV	HSTL_IV	25	0	0.9	1.5
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSTL, Class III, 1.8V	HSTL_III_18	50	0	1.1	1.8
HSTL, Class IV, 1.8V	HSTL_IV_18	25	0	1.1	1.8

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *Without* DCM

Table 35: **Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *Without* DCM**

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
LVTTL Global Clock Input to Output Delay using Output flip-flop, 12 mA, Fast Slew Rate, *without* DCM. For data *output* with different standards, adjust the delays with the values shown in IOB Output Switching Characteristics Standard Adjustments, page 14.						
Global Clock and OFF without DCM	T_{ICKOF}	XC2V40	3.46	3.58	3.69	ns
		XC2V80	3.62	3.58	3.69	ns
		XC2V250	3.79	3.88	4.47	ns
		XC2V500	3.85	3.88	4.47	ns
		XC2V1000	4.02	4.28	4.62	ns
		XC2V1500	4.16	4.28	4.62	ns
		XC2V2000	4.30	4.43	5.10	ns
		XC2V3000	4.49	4.64	5.34	ns
		XC2V4000	4.82	4.99	5.74	ns
		XC2V6000	5.19	5.38	5.93	ns
		XC2V8000		6.09	7.00	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with test setup shown in Figure 1. For other I/O standards, see Table 19.

Table 6: **FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
4	IO_L91N_4/VREF_4	R11	NC	NC
4	IO_L91P_4	T11	NC	NC
4	IO_L92N_4	M11	NC	NC
4	IO_L92P_4	M10	NC	NC
4	IO_L93N_4	N10	NC	NC
4	IO_L93P_4	P10	NC	NC
4	IO_L94N_4/VREF_4	R10		
4	IO_L94P_4	T10		
4	IO_L95N_4/GCLK3S	N9		
4	IO_L95P_4/GCLK2P	P9		
4	IO_L96N_4/GCLK1S	R9		
4	IO_L96P_4/GCLK0P	T9		
5	IO_L96N_5/GCLK7S	T8		
5	IO_L96P_5/GCLK6P	R8		
5	IO_L95N_5/GCLK5S	P8		
5	IO_L95P_5/GCLK4P	N8		
5	IO_L94N_5	T7		
5	IO_L94P_5/VREF_5	R7		
5	IO_L93N_5	P7	NC	NC
5	IO_L93P_5	N7	NC	NC
5	IO_L92N_5	M7	NC	NC
5	IO_L92P_5	M6	NC	NC
5	IO_L91N_5	T6	NC	NC
5	IO_L91P_5/VREF_5	R6	NC	NC
5	IO_L05N_5/VRP_5	P6	NC	NC
5	IO_L05P_5/VRN_5	N6	NC	NC
5	IO_L04N_5	T5	NC	NC
5	IO_L04P_5/VREF_5	R5	NC	NC
5	IO_L03N_5/D4/ALT_VRP_5	P5		
5	IO_L03P_5/D5/ALT_VRN_5	N5		
5	IO_L02N_5/D6	R4		
5	IO_L02P_5/D7	P4		
5	IO_L01N_5/RDWR_B	T4		

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
4	IO_L95N_4/GCLK3S	W12		
4	IO_L95P_4/GCLK2P	Y12		
4	IO_L96N_4/GCLK1S	AA12		
4	IO_L96P_4/GCLK0P	AB12		
5	IO_L96N_5/GCLK7S	AA11		
5	IO_L96P_5/GCLK6P	Y11		
5	IO_L95N_5/GCLK5S	W11		
5	IO_L95P_5/GCLK4P	V11		
5	IO_L94N_5	U11		
5	IO_L94P_5/VREF_5	U10		
5	IO_L93N_5	AB10		
5	IO_L93P_5	AA10		
5	IO_L92N_5	Y10		
5	IO_L92P_5	W10		
5	IO_L91N_5	V10		
5	IO_L91P_5/VREF_5	V9		
5	IO_L54N_5	AB9	NC	
5	IO_L54P_5	AA9	NC	
5	IO_L52N_5	Y9	NC	
5	IO_L52P_5	W9	NC	
5	IO_L51N_5/VREF_5	AB8	NC	
5	IO_L51P_5	AA8	NC	
5	IO_L49N_5	Y8	NC	
5	IO_L49P_5	W8	NC	
5	IO_L24N_5	U9	NC	NC
5	IO_L24P_5	V8	NC	NC
5	IO_L22N_5	AB7	NC	NC
5	IO_L22P_5	AA7	NC	NC
5	IO_L21N_5/VREF_5	Y7	NC	NC
5	IO_L21P_5	W7	NC	NC
5	IO_L19N_5	AB6	NC	NC
5	IO_L19P_5	AA6	NC	NC
5	IO_L06N_5	Y6		

BG575/BGG575 Standard BGA Package

As shown in Table 9, XC2V1000, XC2V1500, and XC2V2000 Virtex-II devices are available in the BG575/BGG575 BGA package. Pins in the XC2V1000, XC2V1500, and XC2V2000 devices are the same, except for the pin differences in the XC2V1000 and XC2V1500 devices shown in the No Connect columns. Following this table are the BG575/BGG575 Standard BGA Package Specifications (1.27mm pitch).

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
0	IO_L01N_0	A3		
0	IO_L01P_0	A4		
0	IO_L02N_0	D5		
0	IO_L02P_0	C5		
0	IO_L03N_0/VRP_0	E6		
0	IO_L03P_0/VRN_0	D6		
0	IO_L04N_0/VREF_0	F7		
0	IO_L04P_0	E7		
0	IO_L05N_0	G8		
0	IO_L05P_0	H9		
0	IO_L06N_0	A5		
0	IO_L06P_0	A6		
0	IO_L19N_0	B5		
0	IO_L19P_0	B6		
0	IO_L21N_0	D7		
0	IO_L21P_0/VREF_0	C7		
0	IO_L22N_0	F8		
0	IO_L22P_0	E8		
0	IO_L24N_0	G9		
0	IO_L24P_0	F9		
0	IO_L49N_0	G10		
0	IO_L49P_0	H10		
0	IO_L51N_0	B7		
0	IO_L51P_0/VREF_0	B8		
0	IO_L52N_0	D8		
0	IO_L52P_0	C8		
0	IO_L54N_0	E9		
0	IO_L54P_0	D9		
0	IO_L67N_0	A8	NC	
0	IO_L67P_0	A9	NC	
0	IO_L69N_0	C9	NC	

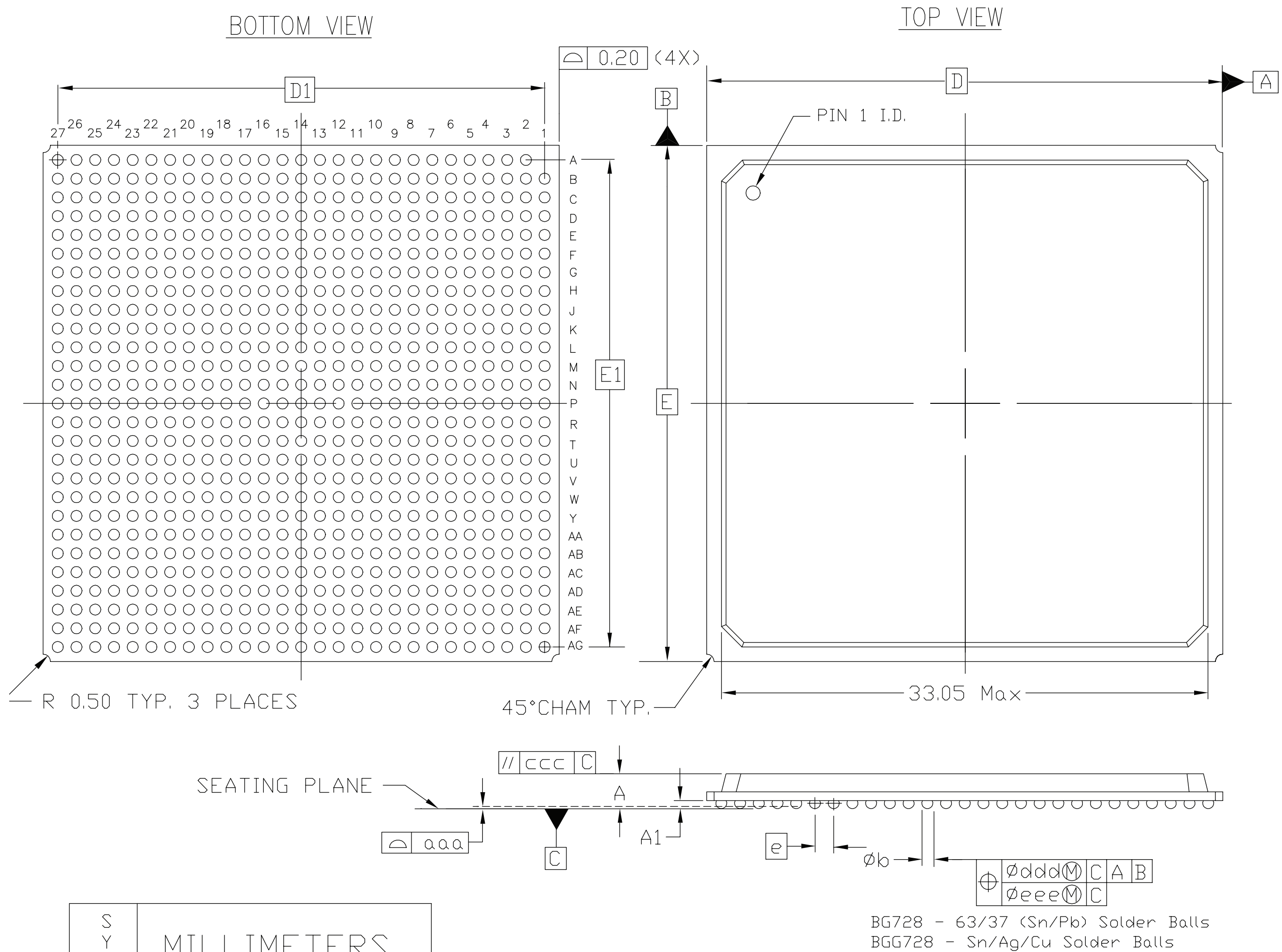
Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
1	IO_L27N_1/VREF_1	F19
1	IO_L27P_1	G19
1	IO_L25N_1	J19
1	IO_L25P_1	J20
1	IO_L24N_1	C20
1	IO_L24P_1	C21
1	IO_L22N_1	D20
1	IO_L22P_1	E21
1	IO_L21N_1/VREF_1	E20
1	IO_L21P_1	F20
1	IO_L19N_1	A21
1	IO_L19P_1	B21
1	IO_L06N_1	A22
1	IO_L06P_1	B22
1	IO_L05N_1	C22
1	IO_L05P_1	C23
1	IO_L04N_1	D22
1	IO_L04P_1/VREF_1	E22
1	IO_L03N_1/VRP_1	A23
1	IO_L03P_1/VRN_1	B23
1	IO_L02N_1	A24
1	IO_L02P_1	B24
1	IO_L01N_1	A25
1	IO_L01P_1	B25
2	IO_L01N_2	C27
2	IO_L01P_2	D27
2	IO_L02N_2/VRP_2	D25
2	IO_L02P_2/VRN_2	D26
2	IO_L03N_2	E24
2	IO_L03P_2/VREF_2	E25
2	IO_L04N_2	E26
2	IO_L04P_2	E27
2	IO_L06N_2	F23
2	IO_L06P_2	F24
2	IO_L19N_2	F25

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
5	IO_L52N_5	AC10
5	IO_L52P_5	AB10
5	IO_L51N_5/VREF_5	Y9
5	IO_L51P_5	Y10
5	IO_L49N_5	AG9
5	IO_L49P_5	AG8
5	IO_L30N_5	AF9
5	IO_L30P_5	AE9
5	IO_L28N_5	AD9
5	IO_L28P_5	AC9
5	IO_L27N_5/VREF_5	AB9
5	IO_L27P_5	AA9
5	IO_L25N_5	AE8
5	IO_L25P_5	AE7
5	IO_L24N_5	AD8
5	IO_L24P_5	AC8
5	IO_L22N_5	AB8
5	IO_L22P_5	AA8
5	IO_L21N_5/VREF_5	AG7
5	IO_L21P_5	AF7
5	IO_L19N_5	AC7
5	IO_L19P_5	AB7
5	IO_L06N_5	AG6
5	IO_L06P_5	AF6
5	IO_L05N_5/VRP_5	AE6
5	IO_L05P_5/VRN_5	AD6
5	IO_L04N_5	AG5
5	IO_L04P_5/VREF_5	AF5
5	IO_L03N_5/D4/ALT_VRP_5	AE5
5	IO_L03P_5/D5/ALT_VRN_5	AD5
5	IO_L02N_5/D6	AG4
5	IO_L02P_5/D7	AF4
5	IO_L01N_5/RDWR_B	AG3
5	IO_L01P_5/CS_B	AF3
6	IO_L01P_6	AE1

BG728/BGG728 Standard BGA Package Specifications (1.27mm pitch)



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A	~	2.33	2.60
A_1	0.50	0.60	0.70
D/E	35.00 BSC		
D_1/E_1	33.02 REF		
e	1.27BSC		
øb	0.60	0.75	0.90
aaa	~	~	0.20
ccc	~	~	0.35
ddd	~	~	0.30
eee	~	~	0.15
M	27		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-BAR-1
4. NO SOLDER BALL AND LAND ON A1.

728-BALL MOLDED BGA (BG728/BGG728)

Figure 6: **BG728/BGG728 Standard BGA Package Specifications**

FF896 Flip-Chip Fine-Pitch BGA Package

As shown in Table 11, XC2V1000, XC2V1500, and XC2V2000 Virtex-II devices are available in the FF896 flip-chip fine-pitch BGA package. Pins in the XC2V1000, XC2V1500, and XC2V2000 devices are the same, except for the pin differences in the XC2V1000 and XC2V1500 devices shown in the No Connect columns. Following this table are the FF896 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
0	IO_L01N_0	B27		
0	IO_L01P_0	A27		
0	IO_L02N_0	F24		
0	IO_L02P_0	E24		
0	IO_L03N_0/VRP_0	C26		
0	IO_L03P_0/VRN_0	C25		
0	IO_L04N_0/VREF_0	A26		
0	IO_L04P_0	A25		
0	IO_L05N_0	F23		
0	IO_L05P_0	F22		
0	IO_L06N_0	C24		
0	IO_L06P_0	D25		
0	IO_L19N_0	A24		
0	IO_L19P_0	B25		
0	IO_L20N_0	G22		
0	IO_L20P_0	G21		
0	IO_L21N_0	D24		
0	IO_L21P_0/VREF_0	D23		
0	IO_L22N_0	B23		
0	IO_L22P_0	B24		
0	IO_L23N_0	H21		
0	IO_L23P_0	H20		
0	IO_L24N_0	E22		
0	IO_L24P_0	E23		
0	IO_L49N_0	A22		
0	IO_L49P_0	B22		
0	IO_L50N_0	F21		
0	IO_L50P_0	F20		
0	IO_L51N_0	C23		
0	IO_L51P_0/VREF_0	C22		
0	IO_L52N_0	B20		
0	IO_L52P_0	B21		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
0	IO_L95P_0/GCLK6S	G16		
0	IO_L96N_0/GCLK5P	C17		
0	IO_L96P_0/GCLK4S	C16		
1	IO_L96N_1/GCLK3P	C15		
1	IO_L96P_1/GCLK2S	C14		
1	IO_L95N_1/GCLK1P	F15		
1	IO_L95P_1/GCLK0S	F14		
1	IO_L94N_1	B15		
1	IO_L94P_1/VREF_1	B14		
1	IO_L93N_1	D14		
1	IO_L93P_1	D15		
1	IO_L92N_1	G15		
1	IO_L92P_1	H15		
1	IO_L91N_1	A14		
1	IO_L91P_1/VREF_1	A13		
1	IO_L78N_1	E14	NC	NC
1	IO_L78P_1	E15	NC	NC
1	IO_L77N_1	J15	NC	NC
1	IO_L77P_1	J14	NC	NC
1	IO_L76N_1	B12	NC	NC
1	IO_L76P_1	B13	NC	NC
1	IO_L75N_1/VREF_1	D13	NC	NC
1	IO_L75P_1	E13	NC	NC
1	IO_L74N_1	H14	NC	NC
1	IO_L74P_1	H13	NC	NC
1	IO_L73N_1	A11	NC	NC
1	IO_L73P_1	A12	NC	NC
1	IO_L72N_1	C11	NC	
1	IO_L72P_1	C12	NC	
1	IO_L71N_1	F13	NC	
1	IO_L71P_1	F12	NC	
1	IO_L70N_1	B10	NC	
1	IO_L70P_1	B11	NC	
1	IO_L69N_1/VREF_1	D12	NC	
1	IO_L69P_1	D11	NC	
1	IO_L68N_1	G13	NC	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
6	IO_L71P_6	AD34	
6	IO_L71N_6	AC34	
6	IO_L72P_6	AC31	
6	IO_L72N_6	AD31	
6	IO_L73P_6	Y27	
6	IO_L73N_6	W27	
6	IO_L74P_6	AB29	
6	IO_L74N_6	AA29	
6	IO_L75P_6	AB31	
6	IO_L75N_6/VREF_6	AA31	
6	IO_L76P_6	Y28	
6	IO_L76N_6	Y29	
6	IO_L77P_6	AB33	
6	IO_L77N_6	AA33	
6	IO_L78P_6	AA30	
6	IO_L78N_6	AB30	
6	IO_L79P_6	W24	NC
6	IO_L79N_6	V24	NC
6	IO_L80P_6	AB34	NC
6	IO_L80N_6	AA34	NC
6	IO_L81P_6	W33	NC
6	IO_L81N_6/VREF_6	Y34	NC
6	IO_L82P_6	W25	NC
6	IO_L82N_6	V25	NC
6	IO_L83P_6	Y32	NC
6	IO_L83N_6	AA32	NC
6	IO_L84P_6	W29	NC
6	IO_L84N_6	V29	NC
6	IO_L91P_6	W28	
6	IO_L91N_6	V28	
6	IO_L92P_6	V33	
6	IO_L92N_6	V34	
6	IO_L93P_6	Y31	
6	IO_L93N_6/VREF_6	W31	
6	IO_L94P_6	V26	
6	IO_L94N_6	V27	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
2	VCCO_2	R11	
2	VCCO_2	R5	
2	VCCO_2	P12	
2	VCCO_2	P11	
2	VCCO_2	N12	
2	VCCO_2	N11	
2	VCCO_2	M11	
2	VCCO_2	K1	
2	VCCO_2	G4	
3	VCCO_3	AH4	
3	VCCO_3	AE1	
3	VCCO_3	AC11	
3	VCCO_3	AB12	
3	VCCO_3	AB11	
3	VCCO_3	AA12	
3	VCCO_3	AA11	
3	VCCO_3	Y12	
3	VCCO_3	Y11	
3	VCCO_3	Y5	
3	VCCO_3	W12	
3	VCCO_3	W1	
3	VCCO_3	V12	
4	VCCO_4	AP16	
4	VCCO_4	AP10	
4	VCCO_4	AL7	
4	VCCO_4	AK15	
4	VCCO_4	AD15	
4	VCCO_4	AD14	
4	VCCO_4	AD13	
4	VCCO_4	AD12	
4	VCCO_4	AC17	
4	VCCO_4	AC16	
4	VCCO_4	AC15	
4	VCCO_4	AC14	
4	VCCO_4	AC13	
5	VCCO_5	AP25	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
4	IO_L08P_4	AL12	NC	
4	IO_L09N_4	AP9	NC	
4	IO_L09P_4/VREF_4	AP8	NC	
4	IO_L10N_4	AV6	NC	
4	IO_L10P_4	AV5	NC	
4	IO_L11N_4	AM11	NC	
4	IO_L11P_4	AM12	NC	
4	IO_L12N_4	AN10	NC	
4	IO_L12P_4	AN9	NC	
4	IO_L19N_4	AU8		
4	IO_L19P_4	AU7		
4	IO_L20N_4	AH14		
4	IO_L20P_4	AH15		
4	IO_L21N_4	AT8		
4	IO_L21P_4/VREF_4	AT7		
4	IO_L22N_4	AW7		
4	IO_L22P_4	AW6		
4	IO_L23N_4	AK13		
4	IO_L23P_4	AK14		
4	IO_L24N_4	AR10		
4	IO_L24P_4	AR9		
4	IO_L25N_4	AV8		
4	IO_L25P_4	AV7		
4	IO_L26N_4	AJ14		
4	IO_L26P_4	AJ15		
4	IO_L27N_4	AP11		
4	IO_L27P_4/VREF_4	AP10		
4	IO_L28N_4	AU10		
4	IO_L28P_4	AU9		
4	IO_L29N_4	AL13		
4	IO_L29P_4	AL14		
4	IO_L30N_4	AN12		
4	IO_L30P_4	AN11		
4	IO_L31N_4	AW9	NC	
4	IO_L31P_4	AW8	NC	
4	IO_L32N_4	AM13	NC	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
5	IO_L73P_5	AJ20	
5	IO_L72N_5	AG18	
5	IO_L72P_5	AG19	
5	IO_L71N_5	AF18	
5	IO_L71P_5	AF19	
5	IO_L70N_5	AK20	
5	IO_L70P_5	AK21	
5	IO_L69N_5/VREF_5	AH20	
5	IO_L69P_5	AH21	
5	IO_L68N_5	AD19	
5	IO_L68P_5	AD20	
5	IO_L67N_5	AL21	
5	IO_L67P_5	AL22	
5	IO_L54N_5	AG20	
5	IO_L54P_5	AG21	
5	IO_L53N_5	AB19	
5	IO_L53P_5	AB20	
5	IO_L52N_5	AJ21	
5	IO_L52P_5	AJ22	
5	IO_L51N_5/VREF_5	AF20	
5	IO_L51P_5	AF21	
5	IO_L50N_5	AE20	
5	IO_L50P_5	AE21	
5	IO_L49N_5	AK22	
5	IO_L49P_5	AK23	
5	IO_L30N_5	AJ23	NC
5	IO_L30P_5	AJ24	NC
5	IO_L29N_5	AC20	NC
5	IO_L29P_5	AC21	NC
5	IO_L28N_5	AL23	NC
5	IO_L28P_5	AL24	NC
5	IO_L27N_5/VREF_5	AL25	NC
5	IO_L27P_5	AL26	NC
5	IO_L26N_5	AD21	NC
5	IO_L26P_5	AD22	NC
5	IO_L25N_5	AH23	NC
5	IO_L25P_5	AH24	NC
5	IO_L24N_5	AG22	