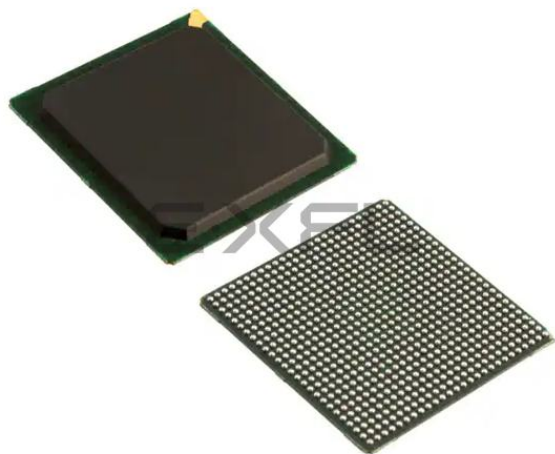




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	3584
Number of Logic Elements/Cells	-
Total RAM Bits	1769472
Number of I/O	484
Number of Gates	3000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v3000-5fgg676i

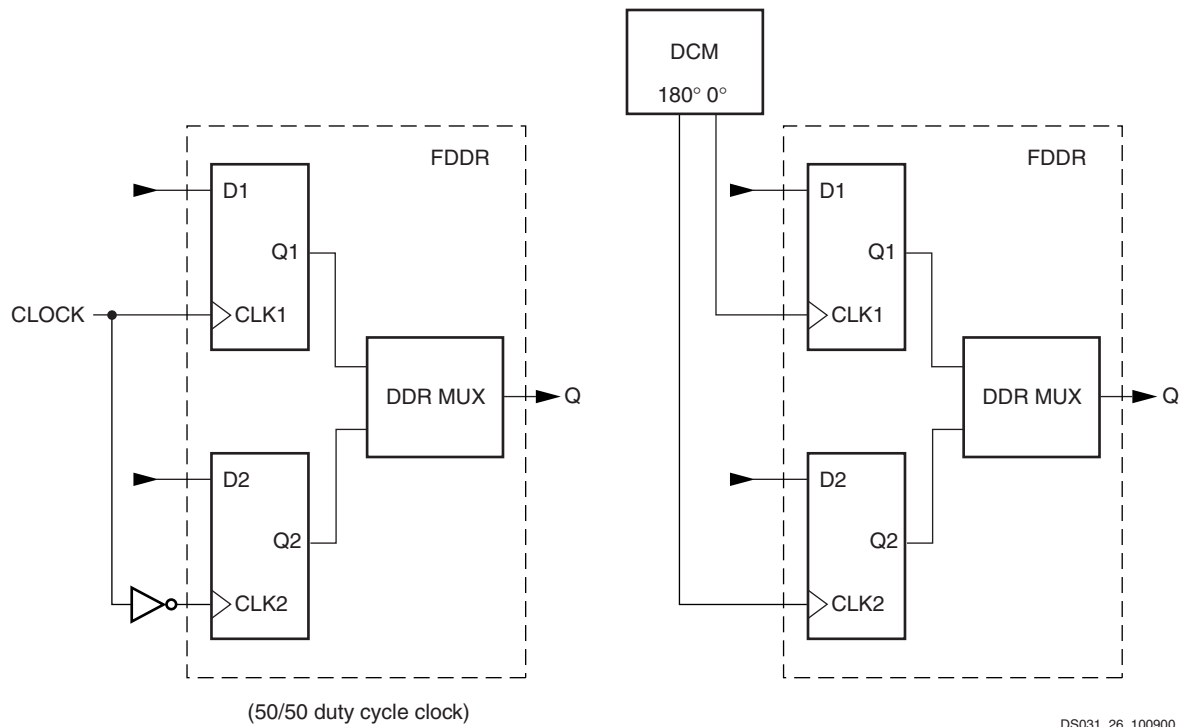


Figure 3: Double Data Rate Registers

The DDR mechanism shown in Figure 3 can be used to mirror a copy of the clock on the output. This is useful for propagating a clock along the data that has an identical delay. It is also useful for multiple clock generation, where there is a unique clock driver for every clock load. Virtex-II devices can produce many copies of a clock with very little skew.

Each group of two registers has a clock enable signal (ICE for the input registers, OCE for the output registers, and TCE for the 3-state registers). The clock enable signals are active High by default. If left unconnected, the clock enable for that storage element defaults to the active state.

Each IOB block has common synchronous or asynchronous set and reset (SR and REV signals).

SR forces the storage element into the state specified by the SRHIGH or SRLOW attribute. SRHIGH forces a logic “1”. SRLOW forces a logic “0”. When SR is used, a second input (REV) forces the storage element into the opposite state. The reset condition predominates over the set condition. The initial state after configuration or global initialization state is defined by a separate INIT0 and INIT1 attribute. By default, the SRLOW attribute forces INIT0, and the SRHIGH attribute forces INIT1.

For each storage element, the SRHIGH, SRLOW, INIT0, and INIT1 attributes are independent. Synchronous or asynchronous set / reset is consistent in an IOB block.

All the control signals have independent polarity. Any inverter placed on a control input is automatically absorbed.

Each register or latch (independent of all other registers or latches) (see Figure 4) can be configured as follows:

- No set or reset
- Synchronous set
- Synchronous reset
- Synchronous set and reset
- Asynchronous set (preset)
- Asynchronous reset (clear)
- Asynchronous set and reset (preset and clear)

The synchronous reset overrides a set, and an asynchronous clear overrides a preset.

Multiplexers

Virtex-II function generators and associated multiplexers can implement the following:

- 4:1 multiplexer in one slice
- 8:1 multiplexer in two slices
- 16:1 multiplexer in one CLB element (4 slices)
- 32:1 multiplexer in two CLB elements (8 slices)

Each Virtex-II slice has one MUXF5 multiplexer and one MUXFX multiplexer. The MUXFX multiplexer implements the MUXF6, MUXF7, or MUXF8, as shown in **Figure 23**. Each CLB element has two MUXF6 multiplexers, one MUXF7 multiplexer and one MUXF8 multiplexer. Examples of multiplexers are shown in the *Virtex-II Platform FPGA User Guide*. Any LUT can implement a 2:1 multiplexer.

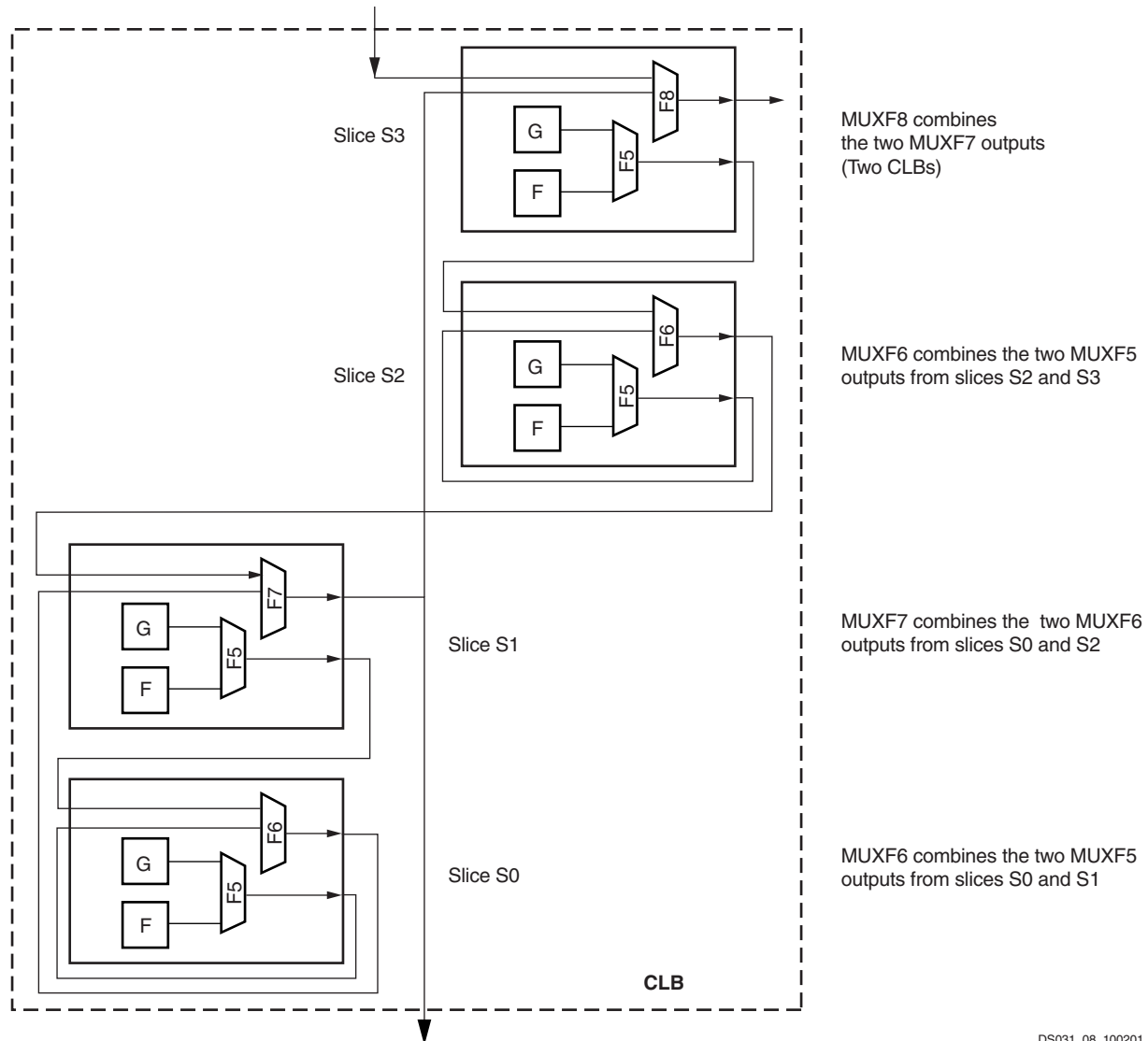


Figure 23: MUXF5 and MUXFX multiplexers

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Fast Lookahead Carry Logic

Dedicated carry logic provides fast arithmetic addition and subtraction. The Virtex-II CLB has two separate carry chains, as shown in the **Figure 24**.

The height of the carry chains is two bits per slice. The carry chain in the Virtex-II device is running upward. The dedicated carry path and carry multiplexer (MUXCY) can also

be used to cascade function generators for implementing wide logic functions.

Arithmetic Logic

The arithmetic logic includes an XOR gate that allows a 2-bit full adder to be implemented within a slice. In addition, a dedicated AND (MULT_AND) gate (shown in **Figure 16**) improves the efficiency of multiplier implementation.

Table 13: Virtex-II Logic Resources Available in All CLBs

Device	CLB Array: Row x Column	Number of Slices	Number of LUTs	Max Distributed SelectRAM or Shift Register (bits)	Number of Flip-Flops	Number of Carry-Chains ⁽¹⁾	Number of SOP Chains ⁽¹⁾
XC2V40	8 x 8	256	512	8,192	512	16	16
XC2V80	16 x 8	512	1,024	16,384	1,024	16	32
XC2V250	24 x 16	1,536	3,072	49,152	3,072	32	48
XC2V500	32 x 24	3,072	6,144	98,304	6,144	48	64
XC2V1000	40 x 32	5,120	10,240	163,840	10,240	64	80
XC2V1500	48 x 40	7,680	15,360	245,760	15,360	80	96
XC2V2000	56 x 48	10,752	21,504	344,064	21,504	96	112
XC2V3000	64 x 56	14,336	28,672	458,752	28,672	112	128
XC2V4000	80 x 72	23,040	46,080	737,280	46,080	144	160
XC2V6000	96 x 88	33,792	67,584	1,081,344	67,584	176	192
XC2V8000	112 x 104	46,592	93,184	1,490,944	93,184	208	224

Notes:

1. The carry-chains and SOP chains can be split or cascaded.

18 Kbit Block SelectRAM Resources

Introduction

Virtex-II devices incorporate large amounts of 18 Kbit block SelectRAM. These complement the distributed SelectRAM resources that provide shallow RAM structures implemented in CLBs. Each Virtex-II block SelectRAM is an 18 Kbit true dual-port RAM with two independently clocked and independently controlled synchronous ports that access a common storage area. Both ports are functionally identical. CLK, EN, WE, and SSR polarities are defined through configuration.

Each port has the following types of inputs: Clock and Clock Enable, Write Enable, Set/Reset, and Address, as well as separate Data/parity data inputs (for write) and Data/parity data outputs (for read).

Operation is synchronous; the block SelectRAM behaves like a register. Control, address and data inputs must (and need only) be valid during the set-up time window prior to a rising (or falling, a configuration option) clock edge. Data outputs change as a result of the same clock edge.

Configuration

The Virtex-II block SelectRAM supports various configurations, including single- and dual-port RAM and various

data/address aspect ratios. Supported memory configurations for single- and dual-port modes are shown in Table 14.

Table 14: Dual- and Single-Port Configurations

16K x 1 bit	2K x 9 bits
8K x 2 bits	1K x 18 bits
4K x 4 bits	512 x 36 bits

Single-Port Configuration

As a single-port RAM, the block SelectRAM has access to the 18 Kbit memory locations in any of the 2K x 9-bit, 1K x 18-bit, or 512 x 36-bit configurations and to 16 Kbit memory locations in any of the 16K x 1-bit, 8K x 2-bit, or 4K x 4-bit configurations. The advantage of the 9-bit, 18-bit and 36-bit widths is the ability to store a parity bit for each eight bits. Parity bits must be generated or checked externally in user logic. In such cases, the width is viewed as 8 + 1, 16 + 2, or 32 + 4. These extra parity bits are stored and behave exactly as the other bits, including the timing parameters. Video applications can use the 9-bit ratio of Virtex-II block SelectRAM memory to advantage.

Each block SelectRAM cell is a fully synchronous memory as illustrated in Figure 29. Input data bus and output data bus widths are identical.

Virtex-II FPGA device. Timing is similar to the Slave Serial-MAP mode except that CCLK is supplied by the Virtex-II FPGA.

Boundary-Scan (JTAG, IEEE 1532) Mode

In Boundary-Scan mode, dedicated pins are used for configuring the Virtex-II device. The configuration is done entirely through the IEEE 1149.1 Test Access Port (TAP). Virtex-II device configuration using Boundary-Scan is compatible with the IEEE 1149.1-1993 standard and the new

IEEE 1532 standard for In-System Configurable (ISC) devices. The IEEE 1532 standard is backward compliant with the IEEE 1149.1-1993 TAP and state machine. The IEEE Standard 1532 for In-System Configurable (ISC) devices is intended to be programmed, reprogrammed, or tested on the board via a physical and logical protocol.

Configuration through the Boundary-Scan port is always available, independent of the mode selection. Selecting the Boundary-Scan mode simply turns off the other modes.

Table 25: Virtex-II Configuration Mode Pin Settings

Configuration Mode ⁽¹⁾	M2	M1	M0	CCLK Direction	Data Width	Serial D _{OUT} ⁽²⁾
Master Serial	0	0	0	Out	1	Yes
Slave Serial	1	1	1	In	1	Yes
Master SelectMAP	0	1	1	Out	8	No
Slave SelectMAP	1	1	0	In	8	No
Boundary-Scan	1	0	1	N/A	1	No

Notes:

1. The HSWAP_EN pin controls the pull-ups. Setting M2, M1, and M0 selects the configuration mode, while the HSWAP_EN pin controls whether or not the pull-ups are used.
2. Daisy chaining is possible only in modes where Serial D_{OUT} is used. For example, in SelectMAP modes, the first device does NOT support daisy chaining of downstream devices.

Table 26 lists the total number of bits required to configure each device.

Table 26: Virtex-II Bitstream Lengths

Device	# of Configuration Bits
XC2V40	338,976
XC2V80	598,816
XC2V250	1,593,632
XC2V500	2,560,544
XC2V1000	4,082,592
XC2V1500	5,170,208
XC2V2000	6,812,960
XC2V3000	10,494,368
XC2V4000	15,659,936
XC2V6000	21,849,504
XC2V8000	26,194,208

Configuration Sequence

The configuration of Virtex-II devices is a three-phase process after Power On Reset or POR. POR occurs when V_{CCINT} is greater than 1.2V, V_{CCAUX} is greater than 2.5V,

and V_{CCO} (bank 4) is greater than 1.5V. Once the POR voltages have been reached, the three-phase process begins.

First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process.

Configuration is automatically initiated on power-up unless it is delayed by the user. The INIT_B pin can be held Low using an open-drain driver. An open-drain is required since INIT_B is a bidirectional open-drain pin that is held Low by a Virtex-II FPGA device while the configuration memory is being cleared. Extending the time that the pin is Low causes the configuration sequencer to wait. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

The configuration process can also be initiated by asserting the PROG_B pin. The end of the memory-clearing phase is signaled by the INIT_B pin going High, and the completion of the entire process is signaled by the DONE pin going High. The Global Set/Reset (GSR) signal is pulsed after the last frame of configuration data is written but before the start-up sequence. The GSR signal resets all flip-flops on the device.

The default start-up sequence is that one CCLK cycle after DONE goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary. One CCLK cycle later, the Global Write Enable (GWE) signal is released. This permits the internal storage ele-

Table 8: FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
2	IO_L45N_2	H23		
2	IO_L45P_2/VREF_2	H24		
2	IO_L46N_2	J21		
2	IO_L46P_2	J20		
2	IO_L48N_2	H25		
2	IO_L48P_2	H26		
2	IO_L49N_2	J22		
2	IO_L49P_2	J23		
2	IO_L51N_2	K21		
2	IO_L51P_2/VREF_2	K22		
2	IO_L52N_2	K20		
2	IO_L52P_2	L20		
2	IO_L54N_2	J24		
2	IO_L54P_2	J25		
2	IO_L67N_2	K23		
2	IO_L67P_2	K24		
2	IO_L69N_2	J26		
2	IO_L69P_2/VREF_2	K26		
2	IO_L70N_2	L22		
2	IO_L70P_2	L21		
2	IO_L72N_2	L25		
2	IO_L72P_2	L26		
2	IO_L73N_2	L19	NC	
2	IO_L73P_2	M19	NC	
2	IO_L75N_2	L23	NC	
2	IO_L75P_2/VREF_2	L24	NC	
2	IO_L76N_2	M22	NC	
2	IO_L76P_2	M21	NC	
2	IO_L78N_2	M23	NC	
2	IO_L78P_2	M24	NC	
2	IO_L91N_2	M25		
2	IO_L91P_2	M26		
2	IO_L93N_2	M20		
2	IO_L93P_2/VREF_2	N20		
2	IO_L94N_2	N22		
2	IO_L94P_2	N21		
2	IO_L96N_2	N24		

Table 8: FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
7	IO_L78N_7	M2	NC	
7	IO_L76P_7	M5	NC	
7	IO_L76N_7	M6	NC	
7	IO_L75P_7/VREF_7	M3	NC	
7	IO_L75N_7	M4	NC	
7	IO_L73P_7	M7	NC	
7	IO_L73N_7	M8	NC	
7	IO_L72P_7	L1		
7	IO_L72N_7	L2		
7	IO_L70P_7	L5		
7	IO_L70N_7	L6		
7	IO_L69P_7/VREF_7	L3		
7	IO_L69N_7	L4		
7	IO_L67P_7	K1		
7	IO_L67N_7	J1		
7	IO_L54P_7	K3		
7	IO_L54N_7	K4		
7	IO_L52P_7	K5		
7	IO_L52N_7	K6		
7	IO_L51P_7/VREF_7	L8		
7	IO_L51N_7	L7		
7	IO_L49P_7	J2		
7	IO_L49N_7	H1		
7	IO_L48P_7	J3		
7	IO_L48N_7	J4		
7	IO_L46P_7	J5		
7	IO_L46N_7	J6		
7	IO_L45P_7/VREF_7	H5		
7	IO_L45N_7	H4		
7	IO_L43P_7	K7		
7	IO_L43N_7	J7		
7	IO_L25P_7	H2	NC	NC
7	IO_L25N_7	H3	NC	NC
7	IO_L24P_7	G1		
7	IO_L24N_7	F1		
7	IO_L22P_7	G3		
7	IO_L22N_7	G4		

Table 9: BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
2	IO_L69P_2/VREF_2	L18	NC	
2	IO_L70N_2	K23	NC	
2	IO_L70P_2	L24	NC	
2	IO_L72N_2	K22	NC	
2	IO_L72P_2	L22	NC	
2	IO_L73N_2	L21	NC	NC
2	IO_L73P_2	L20	NC	NC
2	IO_L91N_2	M23		
2	IO_L91P_2	N24		
2	IO_L93N_2	M21		
2	IO_L93P_2/VREF_2	M22		
2	IO_L94N_2	M19		
2	IO_L94P_2	M20		
2	IO_L96N_2	M17		
2	IO_L96P_2	M18		
3	IO_L96N_3	N23		
3	IO_L96P_3	N22		
3	IO_L94N_3	N20		
3	IO_L94P_3	N21		
3	IO_L93N_3/VREF_3	N19		
3	IO_L93P_3	N18		
3	IO_L91N_3	N17		
3	IO_L91P_3	P17		
3	IO_L73N_3	P24	NC	NC
3	IO_L73P_3	R24	NC	NC
3	IO_L72N_3	R23	NC	
3	IO_L72P_3	R22	NC	
3	IO_L70N_3	P22	NC	
3	IO_L70P_3	P21	NC	
3	IO_L69N_3/VREF_3	P20	NC	
3	IO_L69P_3	P18	NC	
3	IO_L67N_3	T24	NC	
3	IO_L67P_3	U24	NC	
3	IO_L54N_3	T23		
3	IO_L54P_3	T22		

Table 10: BG728 BGA — XC2V3000

Bank	Pin Description	Pin Number
4	IO_L27P_4/VREF_4	AG19
4	IO_L28N_4	AB19
4	IO_L28P_4	AA19
4	IO_L30N_4	AC19
4	IO_L30P_4	AD19
4	IO_L49N_4	AE19
4	IO_L49P_4	AF19
4	IO_L51N_4	AA18
4	IO_L51P_4/VREF_4	Y18
4	IO_L52N_4	AB18
4	IO_L52P_4	AC18
4	IO_L54N_4	AD18
4	IO_L54P_4	AE18
4	IO_L67N_4	AF18
4	IO_L67P_4	AG18
4	IO_L69N_4	AA17
4	IO_L69P_4/VREF_4	Y17
4	IO_L70N_4	AB17
4	IO_L70P_4	AB16
4	IO_L72N_4	AD17
4	IO_L72P_4	AE17
4	IO_L73N_4	AF17
4	IO_L73P_4	AG17
4	IO_L75N_4	Y16
4	IO_L75P_4/VREF_4	W16
4	IO_L76N_4	AC16
4	IO_L76P_4	AD16
4	IO_L78N_4	AF16
4	IO_L78P_4	AG16
4	IO_L91N_4/VREF_4	W15
4	IO_L91P_4	Y15
4	IO_L92N_4	AB15
4	IO_L92P_4	AA15
4	IO_L93N_4	AC15
4	IO_L93P_4	AD15
4	IO_L94N_4/VREF_4	AE15

Table 10: BG728 BGA — XC2V3000

Bank	Pin Description	Pin Number
4	IO_L94P_4	AE14
4	IO_L95N_4/GCLK3S	AF15
4	IO_L95P_4/GCLK2P	AG15
4	IO_L96N_4/GCLK1S	Y14
4	IO_L96P_4/GCLK0P	AA14
5	IO_L96N_5/GCLK7S	AC14
5	IO_L96P_5/GCLK6P	AB14
5	IO_L95N_5/GCLK5S	AG13
5	IO_L95P_5/GCLK4P	AF13
5	IO_L94N_5	AE13
5	IO_L94P_5/VREF_5	AD13
5	IO_L93N_5	AC13
5	IO_L93P_5	AB13
5	IO_L92N_5	AA13
5	IO_L92P_5	Y13
5	IO_L91N_5	W13
5	IO_L91P_5/VREF_5	W12
5	IO_L78N_5	AG12
5	IO_L78P_5	AF12
5	IO_L76N_5	AD12
5	IO_L76P_5	AC12
5	IO_L75N_5/VREF_5	AB12
5	IO_L75P_5	AB11
5	IO_L73N_5	Y12
5	IO_L73P_5	Y11
5	IO_L72N_5	AG11
5	IO_L72P_5	AF11
5	IO_L70N_5	AE11
5	IO_L70P_5	AD11
5	IO_L69N_5/VREF_5	AA10
5	IO_L69P_5	AA11
5	IO_L67N_5	AG10
5	IO_L67P_5	AF10
5	IO_L54N_5	AE10
5	IO_L54P_5	AD10

FF896 Flip-Chip Fine-Pitch BGA Package

As shown in Table 11, XC2V1000, XC2V1500, and XC2V2000 Virtex-II devices are available in the FF896 flip-chip fine-pitch BGA package. Pins in the XC2V1000, XC2V1500, and XC2V2000 devices are the same, except for the pin differences in the XC2V1000 and XC2V1500 devices shown in the No Connect columns. Following this table are the **FF896 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)**.

Table 11: FF896 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
0	IO_L01N_0	B27		
0	IO_L01P_0	A27		
0	IO_L02N_0	F24		
0	IO_L02P_0	E24		
0	IO_L03N_0/VRP_0	C26		
0	IO_L03P_0/VRN_0	C25		
0	IO_L04N_0/VREF_0	A26		
0	IO_L04P_0	A25		
0	IO_L05N_0	F23		
0	IO_L05P_0	F22		
0	IO_L06N_0	C24		
0	IO_L06P_0	D25		
0	IO_L19N_0	A24		
0	IO_L19P_0	B25		
0	IO_L20N_0	G22		
0	IO_L20P_0	G21		
0	IO_L21N_0	D24		
0	IO_L21P_0/VREF_0	D23		
0	IO_L22N_0	B23		
0	IO_L22P_0	B24		
0	IO_L23N_0	H21		
0	IO_L23P_0	H20		
0	IO_L24N_0	E22		
0	IO_L24P_0	E23		
0	IO_L49N_0	A22		
0	IO_L49P_0	B22		
0	IO_L50N_0	F21		
0	IO_L50P_0	F20		
0	IO_L51N_0	C23		
0	IO_L51P_0/VREF_0	C22		
0	IO_L52N_0	B20		
0	IO_L52P_0	B21		

Table 12: FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
0	IO_L77N_0	J20	
0	IO_L77P_0	K19	
0	IO_L78N_0	D20	
0	IO_L78P_0	D21	
0	IO_L79N_0	A21	NC
0	IO_L79P_0	A22	NC
0	IO_L80N_0	L19	NC
0	IO_L80P_0	L18	NC
0	IO_L81N_0	B19	NC
0	IO_L81P_0/VREF_0	A20	NC
0	IO_L82N_0	A18	NC
0	IO_L82P_0	B18	NC
0	IO_L83N_0	H19	NC
0	IO_L83P_0	H18	NC
0	IO_L84N_0	C20	NC
0	IO_L84P_0	C21	NC
0	IO_L91N_0/VREF_0	D19	
0	IO_L91P_0	D18	
0	IO_L92N_0	G18	
0	IO_L92P_0	G19	
0	IO_L93N_0	F18	
0	IO_L93P_0	F19	
0	IO_L94N_0/VREF_0	C19	
0	IO_L94P_0	C18	
0	IO_L95N_0/GCLK7P	K18	
0	IO_L95P_0/GCLK6S	J18	
0	IO_L96N_0/GCLK5P	E19	
0	IO_L96P_0/GCLK4S	E18	
1	IO_L96N_1/GCLK3P	E17	
1	IO_L96P_1/GCLK2S	E16	
1	IO_L95N_1/GCLK1P	H17	
1	IO_L95P_1/GCLK0S	H16	
1	IO_L94N_1	D17	
1	IO_L94P_1/VREF_1	D16	
1	IO_L93N_1	F16	

Table 12: FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
3	IO_L53P_3	AD2	
3	IO_L52N_3	AC8	
3	IO_L52P_3	AB8	
3	IO_L51N_3/VREF_3	AB10	
3	IO_L51P_3	AC10	
3	IO_L50N_3	AD5	
3	IO_L50P_3	AE5	
3	IO_L49N_3	AE4	
3	IO_L49P_3	AF4	
3	IO_L48N_3	AB9	
3	IO_L48P_3	AC9	
3	IO_L47N_3	AE2	
3	IO_L47P_3	AF1	
3	IO_L46N_3	AD6	
3	IO_L46P_3	AE6	
3	IO_L45N_3/VREF_3	AD9	
3	IO_L45P_3	AE9	
3	IO_L44N_3	AF2	
3	IO_L44P_3	AG2	
3	IO_L43N_3	AF3	
3	IO_L43P_3	AG3	
3	IO_L30N_3	AD7	
3	IO_L30P_3	AE7	
3	IO_L29N_3	AF5	
3	IO_L29P_3	AG5	
3	IO_L28N_3	AE8	
3	IO_L28P_3	AD8	
3	IO_L27N_3/VREF_3	AF8	
3	IO_L27P_3	AF9	
3	IO_L26N_3	AH1	
3	IO_L26P_3	AJ1	
3	IO_L25N_3	AG4	
3	IO_L25P_3	AH5	
3	IO_L24N_3	AF6	
3	IO_L24P_3	AG6	
3	IO_L23N_3	AH3	

Table 12: FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
6	IO_L95P_6	W30	
6	IO_L95N_6	V30	
6	IO_L96P_6	V32	
6	IO_L96N_6	W32	
7	IO_L96P_7	U31	
7	IO_L96N_7	V31	
7	IO_L95P_7	T28	
7	IO_L95N_7	U28	
7	IO_L94P_7	U33	
7	IO_L94N_7	U34	
7	IO_L93P_7/VREF_7	U29	
7	IO_L93N_7	T29	
7	IO_L92P_7	U27	
7	IO_L92N_7	U26	
7	IO_L91P_7	T30	
7	IO_L91N_7	U30	
7	IO_L84P_7	R32	NC
7	IO_L84N_7	T32	NC
7	IO_L83P_7	U25	NC
7	IO_L83N_7	T25	NC
7	IO_L82P_7	R34	NC
7	IO_L82N_7	T33	NC
7	IO_L81P_7/VREF_7	N34	NC
7	IO_L81N_7	P34	NC
7	IO_L80P_7	U24	NC
7	IO_L80N_7	T24	NC
7	IO_L79P_7	R31	NC
7	IO_L79N_7	T31	NC
7	IO_L78P_7	N32	
7	IO_L78N_7	P32	
7	IO_L77P_7	T27	
7	IO_L77N_7	R27	
7	IO_L76P_7	N33	
7	IO_L76N_7	P33	
7	IO_L75P_7/VREF_7	R29	

Table 12: FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
NA	GND	P20	
NA	GND	P19	
NA	GND	P18	
NA	GND	P17	
NA	GND	P16	
NA	GND	P15	
NA	GND	P14	
NA	GND	P7	
NA	GND	M30	
NA	GND	M5	
NA	GND	K32	
NA	GND	K3	
NA	GND	J19	
NA	GND	J16	
NA	GND	H34	
NA	GND	H27	
NA	GND	H8	
NA	GND	H1	
NA	GND	G28	
NA	GND	G21	
NA	GND	G14	
NA	GND	G7	
NA	GND	F29	
NA	GND	F6	
NA	GND	E30	
NA	GND	E23	
NA	GND	E12	
NA	GND	E5	
NA	GND	D31	
NA	GND	D4	
NA	GND	C34	
NA	GND	C32	
NA	GND	C25	
NA	GND	C10	
NA	GND	C3	
NA	GND	C1	

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
2	IO_L33P_2/VREF_2	J4	NC	
2	IO_L34N_2	K2	NC	
2	IO_L34P_2	J2	NC	
2	IO_L35N_2	P12	NC	
2	IO_L35P_2	R12	NC	
2	IO_L36N_2	M6	NC	
2	IO_L36P_2	L6	NC	
2	IO_L43N_2	L3		
2	IO_L43P_2	K3		
2	IO_L44N_2	N9		
2	IO_L44P_2	P9		
2	IO_L45N_2	M4		
2	IO_L45P_2/VREF_2	L4		
2	IO_L46N_2	L1		
2	IO_L46P_2	K1		
2	IO_L47N_2	P10		
2	IO_L47P_2	R10		
2	IO_L48N_2	N5		
2	IO_L48P_2	M5		
2	IO_L49N_2	N3		
2	IO_L49P_2	M3		
2	IO_L50N_2	N8		
2	IO_L50P_2	P8		
2	IO_L51N_2	T11		
2	IO_L51P_2/VREF_2	R11		
2	IO_L52N_2	N2		
2	IO_L52P_2	M2		
2	IO_L53N_2	T12		
2	IO_L53P_2	U12		
2	IO_L54N_2	P6		
2	IO_L54P_2	N6		
2	IO_L55N_2	N1		
2	IO_L55P_2	M1		
2	IO_L56N_2	R8		
2	IO_L56P_2	T8		
2	IO_L57N_2	R7		

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
3	IO_L58N_3	AD5		
3	IO_L58P_3	AE5		
3	IO_L57N_3/VREF_3	AE11		
3	IO_L57P_3	AD11		
3	IO_L56N_3	AG1		
3	IO_L56P_3	AH1		
3	IO_L55N_3	AD6		
3	IO_L55P_3	AE6		
3	IO_L54N_3	AF10		
3	IO_L54P_3	AE10		
3	IO_L53N_3	AG2		
3	IO_L53P_3	AH2		
3	IO_L52N_3	AF4		
3	IO_L52P_3	AG4		
3	IO_L51N_3/VREF_3	AG8		
3	IO_L51P_3	AF8		
3	IO_L50N_3	AH3		
3	IO_L50P_3	AJ3		
3	IO_L49N_3	AE7		
3	IO_L49P_3	AF7		
3	IO_L48N_3	AG9		
3	IO_L48P_3	AF9		
3	IO_L47N_3	AF6		
3	IO_L47P_3	AG6		
3	IO_L46N_3	AG5		
3	IO_L46P_3	AH5		
3	IO_L45N_3/VREF_3	AF12		
3	IO_L45P_3	AE12		
3	IO_L44N_3	AJ1		
3	IO_L44P_3	AK1		
3	IO_L43N_3	AH4		
3	IO_L43P_3	AJ4		
3	IO_L36N_3	AG11	NC	
3	IO_L36P_3	AF11	NC	
3	IO_L35N_3	AK2	NC	
3	IO_L35P_3	AL2	NC	

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
3	IO_L34N_3	AH6	NC	
3	IO_L34P_3	AJ6	NC	
3	IO_L33N_3/VREF_3	AJ8	NC	
3	IO_L33P_3	AH8	NC	
3	IO_L32N_3	AL1	NC	
3	IO_L32P_3	AM1	NC	
3	IO_L31N_3	AH7	NC	
3	IO_L31P_3	AJ7	NC	
3	IO_L30N_3	AH10		
3	IO_L30P_3	AG10		
3	IO_L29N_3	AK3		
3	IO_L29P_3	AL3		
3	IO_L28N_3	AK4		
3	IO_L28P_3	AL4		
3	IO_L27N_3/VREF_3	AJ9		
3	IO_L27P_3	AH9		
3	IO_L26N_3	AM2		
3	IO_L26P_3	AN2		
3	IO_L25N_3	AK5		
3	IO_L25P_3	AL5		
3	IO_L24N_3	AK9		
3	IO_L24P_3	AK8		
3	IO_L23N_3	AN1		
3	IO_L23P_3	AP1		
3	IO_L22N_3	AK6		
3	IO_L22P_3	AL6		
3	IO_L21N_3/VREF_3	AH12		
3	IO_L21P_3	AG12		
3	IO_L20N_3	AM3		
3	IO_L20P_3	AN3		
3	IO_L19N_3	AM4		
3	IO_L19P_3	AN4		
3	IO_L12N_3	AJ12	NC	
3	IO_L12P_3	AH11	NC	
3	IO_L11N_3	AP2	NC	
3	IO_L11P_3	AR2	NC	

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
6	IO_L23N_6	AM38		
6	IO_L24P_6	AM36		
6	IO_L24N_6	AN36		
6	IO_L25P_6	AH30		
6	IO_L25N_6	AG30		
6	IO_L26P_6	AM37		
6	IO_L26N_6	AL37		
6	IO_L27P_6	AK34		
6	IO_L27N_6/VREF_6	AL34		
6	IO_L28P_6	AG29		
6	IO_L28N_6	AF29		
6	IO_L29P_6	AL35		
6	IO_L29N_6	AK35		
6	IO_L30P_6	AH33		
6	IO_L30N_6	AJ33		
6	IO_L31P_6	AJ32	NC	
6	IO_L31N_6	AH32	NC	
6	IO_L32P_6	AM39	NC	
6	IO_L32N_6	AL39	NC	
6	IO_L33P_6	AK36	NC	
6	IO_L33N_6/VREF_6	AL36	NC	
6	IO_L34P_6	AF28	NC	
6	IO_L34N_6	AE28	NC	
6	IO_L35P_6	AL38	NC	
6	IO_L35N_6	AK38	NC	
6	IO_L36P_6	AH34	NC	
6	IO_L36N_6	AJ34	NC	
6	IO_L43P_6	AG31		
6	IO_L43N_6	AF31		
6	IO_L44P_6	AK37		
6	IO_L44N_6	AJ37		
6	IO_L45P_6	AH36		
6	IO_L45N_6/VREF_6	AJ36		
6	IO_L46P_6	AF30		
6	IO_L46N_6	AE30		
6	IO_L47P_6	AK39		

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
6	IO_L47N_6	AJ39		
6	IO_L48P_6	AG35		
6	IO_L48N_6	AH35		
6	IO_L49P_6	AG32		
6	IO_L49N_6	AF32		
6	IO_L50P_6	AH37		
6	IO_L50N_6	AG37		
6	IO_L51P_6	AD29		
6	IO_L51N_6/VREF_6	AE29		
6	IO_L52P_6	AD28		
6	IO_L52N_6	AC28		
6	IO_L53P_6	AH38		
6	IO_L53N_6	AG38		
6	IO_L54P_6	AF34		
6	IO_L54N_6	AG34		
6	IO_L55P_6	AE32		
6	IO_L55N_6	AD32		
6	IO_L56P_6	AH39		
6	IO_L56N_6	AG39		
6	IO_L57P_6	AE33		
6	IO_L57N_6/VREF_6	AF33		
6	IO_L58P_6	AD30		
6	IO_L58N_6	AC30		
6	IO_L59P_6	AF37		
6	IO_L59N_6	AE37		
6	IO_L60P_6	AF36		
6	IO_L60N_6	AG36		
6	IO_L67P_6	AD31		
6	IO_L67N_6	AC31		
6	IO_L68P_6	AE34		
6	IO_L68N_6	AD34		
6	IO_L69P_6	AD35		
6	IO_L69N_6/VREF_6	AE35		
6	IO_L70P_6	AB28		
6	IO_L70N_6	AA28		
6	IO_L71P_6	AF39		

Table 14: BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000

Bank	Pin Description	Pin Number	No Connect in XC2V2000
3	IO_L93P_3	V1	
3	IO_L92N_3	U8	
3	IO_L92P_3	W8	
3	IO_L91N_3	U2	
3	IO_L91P_3	V2	
3	IO_L78N_3	U7	
3	IO_L78P_3	V7	
3	IO_L77N_3	U4	
3	IO_L77P_3	V4	
3	IO_L76N_3	W1	
3	IO_L76P_3	Y1	
3	IO_L75N_3/VREF_3	V5	
3	IO_L75P_3	W5	
3	IO_L74N_3	W2	
3	IO_L74P_3	Y2	
3	IO_L73N_3	W6	
3	IO_L73P_3	Y6	
3	IO_L72N_3	Y5	
3	IO_L72P_3	AA5	
3	IO_L71N_3	W3	
3	IO_L71P_3	Y3	
3	IO_L70N_3	W4	
3	IO_L70P_3	Y4	
3	IO_L69N_3/VREF_3	U9	
3	IO_L69P_3	V9	
3	IO_L68N_3	AA1	
3	IO_L68P_3	AB1	
3	IO_L67N_3	Y7	
3	IO_L67P_3	AA7	
3	IO_L54N_3	AA6	
3	IO_L54P_3	AC6	
3	IO_L53N_3	AA2	
3	IO_L53P_3	AB2	
3	IO_L52N_3	AA4	
3	IO_L52P_3	AC4	
3	IO_L51N_3/VREF_3	V10	
3	IO_L51P_3	W10	
3	IO_L50N_3	AA3	