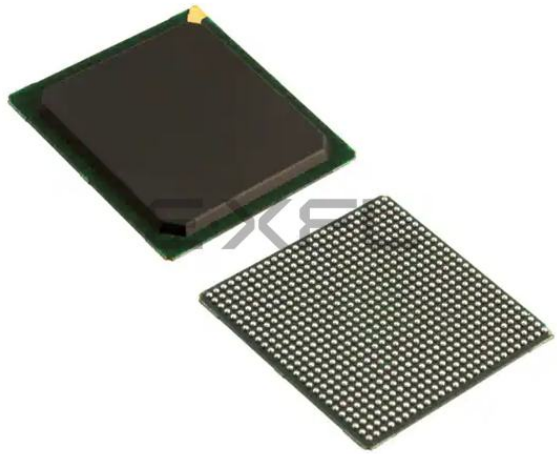

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3584
Number of Logic Elements/Cells	-
Total RAM Bits	1769472
Number of I/O	484
Number of Gates	3000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v3000-6fgg676c

Table 2: **Supported Differential Signal I/O Standards**

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Output V_{OD}
LVPECL_33	3.3	N/R(1)	N/R	0.490 - 1.220
LDT_25	2.5	N/R	N/R	0.500 - 0.700
LVDS_33	3.3	N/R	N/R	0.250 - 0.400
LVDS_25	2.5	N/R	N/R	0.250 - 0.400
LVDSEXT_33	3.3	N/R	N/R	0.440 - 0.820
LVDSEXT_25	2.5	N/R	N/R	0.440 - 0.820
BLVDS_25	2.5	N/R	N/R	0.250 - 0.450
ULVDS_25	2.5	N/R	N/R	0.500 - 0.700

Notes:
1. N/R = no requirement.

Table 3: **Supported DCI I/O Standards**

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Termination Type
LVDCI_33(1)	3.3	3.3	N/R(4)	Series
LVDCI_DV2_33(1)	3.3	3.3	N/R	Series
LVDCI_25(1)	2.5	2.5	N/R	Series
LVDCI_DV2_25(1)	2.5	2.5	N/R	Series
LVDCI_18(1)	1.8	1.8	N/R	Series
LVDCI_DV2_18(1)	1.8	1.8	N/R	Series
LVDCI_15(1)	1.5	1.5	N/R	Series
LVDCI_DV2_15(1)	1.5	1.5	N/R	Series
GTL_DCI	1.2	1.2	0.8	Single
GTLP_DCI	1.5	1.5	1.0	Single
HSTL_I_DCI	1.5	1.5	0.75	Split
HSTL_II_DCI	1.5	1.5	0.75	Split
HSTL_III_DCI	1.5	1.5	0.9	Single
HSTL_IV_DCI	1.5	1.5	0.9	Single
HSTL_I_DCI_18	1.8	1.8	0.9	Split
HSTL_II_DCI_18	1.8	1.8	0.9	Split
HSTL_III_DCI_18	1.8	1.8	1.1	Single
HSTL_IV_DCI_18	1.8	1.8	1.1	Single
SSTL18_I_DCI(3)	1.8	1.8	0.9	Split
SSTL18_II_DCI	1.8	1.8	0.9	Split
SSTL2_I_DCI(2)	2.5	2.5	1.25	Split
SSTL2_II_DCI(2)	2.5	2.5	1.25	Split
SSTL3_I_DCI(2)	3.3	3.3	1.5	Split
SSTL3_II_DCI(2)	3.3	3.3	1.5	Split
LVDS_25_DCI	2.5	2.5	N/R	Split
LVDSEXT_25_DCI	2.5	2.5	N/R	Split

Notes:
1. LVDCI_XX and LVDCI_DV2_XX are LVCMOS controlled impedance buffers, matching the reference resistors or half of the reference resistors.
2. These are SSTL compatible.
3. SSTL18_I is not a JEDEC-supported standard.
4. N/R = no requirement.

Logic Resources

IOB blocks include six storage elements, as shown in Figure 2.

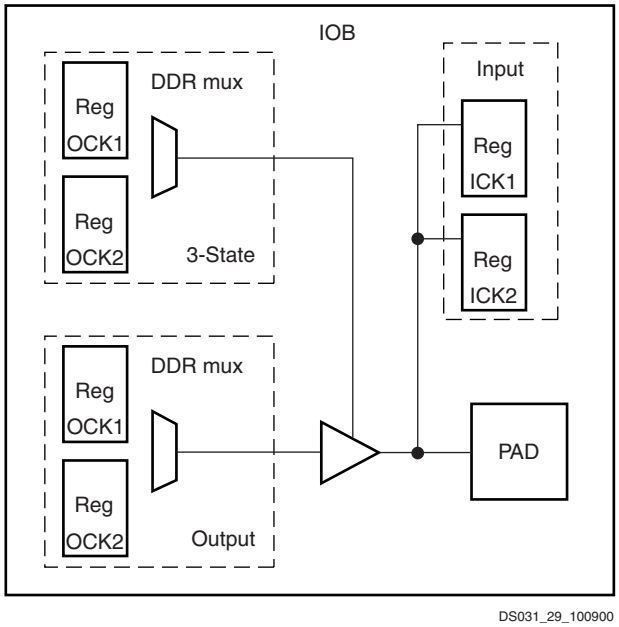

Figure 2: **Virtex-II IOB Block**

Each storage element can be configured either as an edge-triggered D-type flip-flop or as a level-sensitive latch. On the input, output, and 3-state path, one or two DDR registers can be used.

Double data rate is directly accomplished by the two registers on each path, clocked by the rising edges (or falling edges) from two different clock nets. The two clock signals are generated by the DCM and must be 180 degrees out of phase, as shown in Figure 3. There are two input, output, and 3-state data signals, each being alternately clocked out.

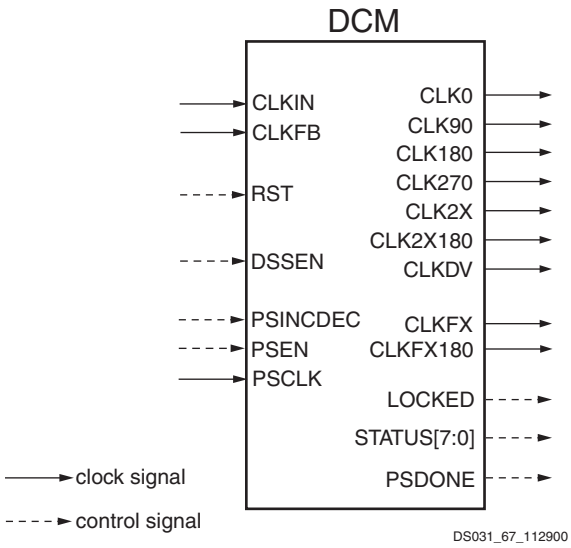

Figure 45: **Digital Clock Manager**

The DCM can be configured to delay the completion of the Virtex-II configuration process until after the DCM has achieved lock. This guarantees that the chip does not begin operating until after the system clocks generated by the DCM have stabilized.

The DCM has the following general control signals:

- RST input pin: resets the entire DCM
- LOCKED output pin: asserted High when all enabled DCM circuits have locked.
- STATUS output pins (active High): shown in Table 21.

Table 21: **DCM Status Pins**

Status Pin	Function
0	Phase Shift Overflow
1	CLKIN Stopped
2	CLKFX Stopped
3	N/A
4	N/A
5	N/A
6	N/A
7	N/A

Clock De-Skew

The DCM de-skews the output clocks relative to the input clock by automatically adjusting a digital delay line. Additional delay is introduced so that clock edges arrive at internal registers and block RAMs simultaneously with the clock edges arriving at the input clock pad. Alternatively, external clocks, which are also de-skewed relative to the input clock, can be generated for board-level routing. All DCM output clocks are phase-aligned to CLK0 and, therefore, are also phase-aligned to the input clock.

To achieve clock de-skew, the CLKFB input must be connected, and its source must be either CLK0 or CLK2X. Note that CLKFB must always be connected, unless only the CLKFX or CLKFX180 outputs are used and de-skew is not required.

Frequency Synthesis

The DCM provides flexible methods for generating new clock frequencies. Each method has a different operating frequency range and different AC characteristics. The CLK2X and CLK2X180 outputs double the clock frequency. The CLKDV output creates divided output clocks with division options of 1.5, 2, 2.5, 3, 3.5, 4, 4.5, 5, 5.5, 6, 6.5, 7, 7.5, 8, 9, 10, 11, 12, 13, 14, 15, and 16.

The CLKFX and CLKFX180 outputs can be used to produce clocks at the following frequency:

$$FREQ_{CLKFX} = (M/D) * FREQ_{CLKIN}$$

where M and D are two integers. Specifications for M and D are provided under DCM Timing Parameters in Module 3. By default, M=4 and D=1, which results in a clock output frequency four times faster than the clock input frequency (CLKIN).

CLK2X180 is phase shifted 180 degrees relative to CLK2X. CLKFX180 is phase shifted 180 degrees relative to CLKFX. All frequency synthesis outputs automatically have 50/50 duty cycles (with the exception of the CLKDV output when performing a non-integer divide in high-frequency mode).

Note that CLK2X and CLK2X180 are not available in high-frequency mode.

Phase Shifting

The DCM provides additional control over clock skew through either coarse or fine-grained phase shifting. The CLK0, CLK90, CLK180, and CLK270 outputs are each phase shifted by ¼ of the input clock period relative to each other, providing coarse phase control. Note that CLK90 and CLK270 are not available in high-frequency mode.

Fine-phase adjustment affects all nine DCM output clocks. When activated, the phase shift between the rising edges of CLKIN and CLKFB is a specified fraction of the input clock period.

In variable mode, the PHASE_SHIFT value can also be dynamically incremented or decremented as determined by PSINCDEC synchronously to PSCLK, when the PSEN input is active. Figure 46 illustrates the effects of fine-phase shifting. For more information on DCM features, see the Virtex-II *User Guide*.

Routing

DCM Locations/Organization

Virtex-II DCMs are placed on the top and bottom of each block RAM and multiplier column. The number of DCMs depends on the device size, as shown in Table 24.

Table 24: **DCM Organization**

Device	Columns	DCMs
XC2V40	2	4
XC2V80	2	4
XC2V250	4	8
XC2V500	4	8
XC2V1000	4	8
XC2V1500	4	8
XC2V2000	4	8
XC2V3000	6	12
XC2V4000	6	12
XC2V6000	6	12
XC2V8000	6	12

Active Interconnect Technology

Local and global Virtex-II routing resources are optimized for speed and timing predictability, as well as to facilitate IP cores implementation. Virtex-II Active Interconnect Technology is a fully buffered programmable routing matrix. All routing resources are segmented to offer the advantages of a hierarchical solution. Virtex-II logic features like CLBs, IOBs, block RAM, multipliers, and DCMs are all connected to an identical switch matrix for access to global routing resources, as shown in Figure 47.

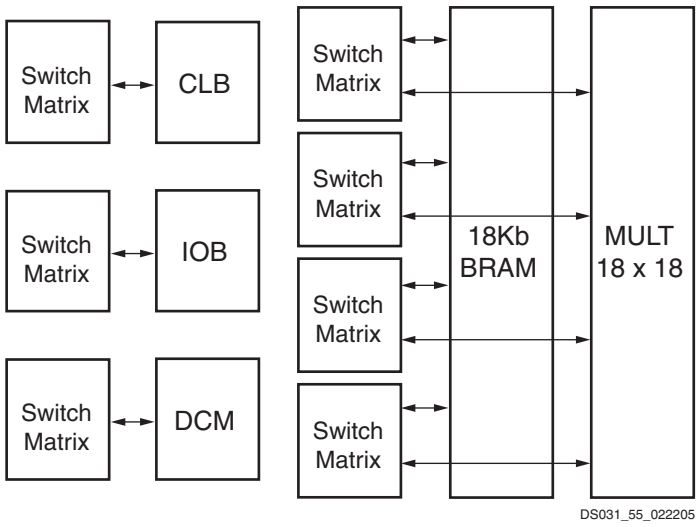

Figure 47: **Active Interconnect Technology**

Each Virtex-II device can be represented as an array of switch matrixes with logic blocks attached, as illustrated in Figure 48.

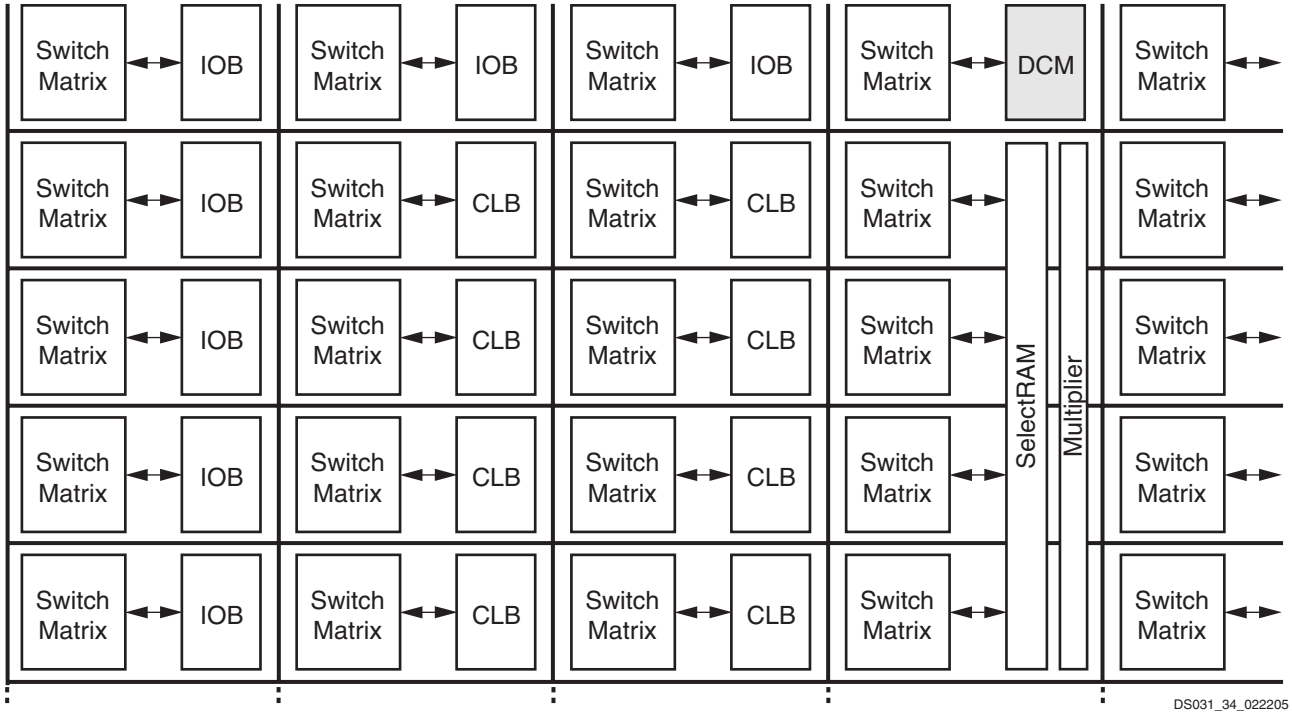

Figure 48: **Routing Resources**

Virtex-II Electrical Characteristics

Virtex-II™ devices are provided in -6, -5, and -4 speed grades, with -6 having the highest performance.

Virtex-II DC and AC characteristics are specified for both commercial and industrial grades. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -4 speed grade industrial device are the same as for a -4 speed grade commercial device). However, only selected speed grades and/or devices might be available in the industrial range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications. Contact Xilinx for design considerations requiring more detailed information.

All specifications are subject to change without notice.

Virtex-II DC Characteristics

Table 1: **Absolute Maximum Ratings**

Symbol	Description(1)			Units
V_{CCINT}	Internal supply voltage relative to GND		–0.5 to 1.65	V
V_{CCAUX}	Auxiliary supply voltage relative to GND		–0.5 to 4.0	V
V_{CCO}	Output drivers supply voltage relative to GND		–0.5 to 4.0	V
V_{BATT}	Key memory battery backup supply		–0.5 to 4.0	V
V_{REF}	Input reference voltage		–0.5 to V_{CCO} + 0.5	V
V_{IN}(3)	Input voltage relative to GND (user and dedicated I/Os)		–0.5 to V_{CCO} + 0.5	V
V_{TS}	Voltage applied to 3-state output (user and dedicated I/Os)		–0.5 to 4.0	V
T_{STG}	Storage temperature (ambient)		–65 to +150	°C
T_{SOL}	Maximum soldering temperature(2)	All regular FF/BF flip-chip and FG/BG/CS wire-bond packages	+220	°C
		Pb-free FGG456, FGG676, BGG575, and BGG728 wire-bond packages	+250	°C
		Pb-free FGG256 and CSG144 wire-bond packages	+260	°C
T_J	Maximum junction temperature(2)		+125	°C

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. For soldering guidelines and thermal considerations, see the **Device Packaging and Thermal Characteristics Guide** information on the Xilinx website.
3. Inputs configured as PCI are fully PCI compliant. This statement takes precedence over any specification that would imply that the device is not PCI compliant.

Virtex-II Switching Characteristics

Switching characteristics in this document are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Note that Virtex-II Performance Characteristics, page 7 are subject to these guidelines as well. Each designation is defined as follows:

Advance: These speed files are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These speed files are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production: These speed files are released once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 13 correlates the current status of each Virtex-II device with a corresponding speed grade designation.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the Xilinx static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-II devices.

IOB Input Switching Characteristics

Input delays associated with the pad are specified for LVTTL levels. For other standards, adjust the delays with the values shown in IOB Input Switching Characteristics Standard Adjustments, page 11.

Table 13: **Virtex-II Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC2V40			-6, -5, -4
XC2V80			-6, -5, -4
XC2V250			-6, -5, -4
XC2V500			-6, -5, -4
XC2V1000			-6, -5, -4
XC2V1500			-6, -5, -4
XC2V2000			-6, -5, -4
XC2V3000			-6, -5, -4
XC2V4000			-6, -5, -4
XC2V6000			-6, -5, -4
XC2V8000			-5, -4

Table 14: **IOB Input Switching Characteristics**

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
Propagation Delays						
Pad to I output, no delay	T_{IOPI}	All	0.69	0.76	0.88	ns, Max
Pad to I output, with delay	T_{IOPID}	XC2V40	1.92	2.11	2.43	ns, Max
		XC2V80	1.92	2.11	2.43	ns, Max
		XC2V250	1.92	2.11	2.43	ns, Max
		XC2V500	1.92	2.11	2.43	ns, Max
		XC2V1000	1.92	2.11	2.43	ns, Max
		XC2V1500	1.92	2.11	2.43	ns, Max
		XC2V2000	1.92	2.11	2.43	ns, Max
		XC2V3000	1.97	2.16	2.49	ns, Max
		XC2V4000	1.97	2.16	2.49	ns, Max
		XC2V6000	2.10	2.31	2.66	ns, Max
		XC2V8000		2.31	2.66	ns, Max

IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in IOB Output Switching Characteristics Standard Adjustments, page 14.

Table 16: **IOB Output Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-6**	**-5**	**-4**	**Units**
Propagation Delays					
O input to Pad	T_{IOOP}	1.43	1.51	1.74	ns, Max
O input to Pad via transparent latch	T_{IOOLP}	1.72	1.83	2.11	ns, Max
3-State Delays					
T input to Pad high-impedance(1)	T_{IOTHZ}	0.51	0.56	0.64	ns, Max
T input to valid data on Pad	T_{IOTP}	1.38	1.45	1.67	ns, Max
T input to Pad high-impedance via transparent latch(1)	$T_{IOTLPHZ}$	0.80	0.88	1.01	ns, Max
T input to valid data on Pad via transparent latch	$T_{IOTLPON}$	1.67	1.77	2.04	ns, Max
GTS to Pad high impedance(1)	T_{GTS}	4.73	5.20	5.98	ns, Max
Sequential Delays					
Clock CLK to Pad	T_{IOCKP}	1.76	1.87	2.15	ns, Max
Clock CLK to Pad high-impedance (synchronous)(1)	T_{IOCKHZ}	0.95	1.04	1.20	ns, Max
Clock CLK to valid data on Pad (synchronous)	T_{IOCKON}	1.82	1.94	2.22	ns, Max
Setup and Hold Times Before/After Clock CLK					
O input	T_{IOOCK}/T_{IOCKO}	0.31/–0.08	0.34/–0.09	0.39/–0.11	ns, Min
OCE input	$T_{IOOCECK}/T_{IOCKOCE}$	0.19/–0.06	0.21/–0.07	0.24/–0.08	ns, Min
SR input (OFF)	$T_{IOSRCKO}/T_{IOCKOSR}$	0.27/–0.05	0.30/–0.06	0.34/–0.07	ns, Min
3–State Setup Times, T input	T_{IOTCK}/T_{IOCKT}	0.28/–0.06	0.31/–0.07	0.35/–0.08	ns, Min
3–State Setup Times, TCE input	$T_{IOTCECK}/T_{IOCKTCE}$	0.19/–0.06	0.21/–0.07	0.24/–0.08	ns, Min
3–State Setup Times, SR input (TFF)	$T_{IOSRCKT}/T_{IOCKTSR}$	0.27/–0.05	0.30/–0.06	0.34/–0.07	ns, Min
Set/Reset Delays					
Minimum Pulse Width, SR input (asynchronous)	T_{RPW}	0.61	0.67	0.77	ns, Min
SR input to Pad (asynchronous)	T_{IOSRP}	2.41	2.59	2.98	ns, Max
SR input to Pad high-impedance (asynchronous)(1)	T_{IOSRHZ}	1.52	1.67	1.92	ns, Max
SR input to valid data on Pad (asynchronous)	T_{IOSRON}	2.39	2.56	2.95	ns, Max
GSR to Pad	T_{IOGSRQ}	5.44	5.98	6.88	ns, Max

Notes:
1. The 3-state turn-off delays should not be adjusted.

Global Clock Setup and Hold for LVTTL Standard, *Without* DCM

Table 37: **Global Clock Setup and Hold for LVTTL Standard, *Without* DCM**

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard.(2) For data input with different standards, adjust the setup time delay by the values shown in IOB Input Switching Characteristics Standard Adjustments, page 11.						
Full Delay Global Clock and IFF(1) without DCM	T_{PSFD}/T_{PHFD}	XC2V40	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V80	2.10/ 0.00	2.10/ 0.00	2.21/ 0.00	ns
		XC2V250	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V500	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V1000	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V1500	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V2000	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V3000	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V4000	2.00/ 0.00	2.00/ 0.00	2.30/ 0.00	ns
		XC2V6000	1.92/ 0.50	1.92/ 0.50	2.21/ 0.50	ns
		XC2V8000		2.38/ 0.00	2.60/ 0.00	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. These values are parametrically measured.

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
4	IO_L95N_4/GCLK3S	W12		
4	IO_L95P_4/GCLK2P	Y12		
4	IO_L96N_4/GCLK1S	AA12		
4	IO_L96P_4/GCLK0P	AB12		
5	IO_L96N_5/GCLK7S	AA11		
5	IO_L96P_5/GCLK6P	Y11		
5	IO_L95N_5/GCLK5S	W11		
5	IO_L95P_5/GCLK4P	V11		
5	IO_L94N_5	U11		
5	IO_L94P_5/VREF_5	U10		
5	IO_L93N_5	AB10		
5	IO_L93P_5	AA10		
5	IO_L92N_5	Y10		
5	IO_L92P_5	W10		
5	IO_L91N_5	V10		
5	IO_L91P_5/VREF_5	V9		
5	IO_L54N_5	AB9	NC	
5	IO_L54P_5	AA9	NC	
5	IO_L52N_5	Y9	NC	
5	IO_L52P_5	W9	NC	
5	IO_L51N_5/VREF_5	AB8	NC	
5	IO_L51P_5	AA8	NC	
5	IO_L49N_5	Y8	NC	
5	IO_L49P_5	W8	NC	
5	IO_L24N_5	U9	NC	NC
5	IO_L24P_5	V8	NC	NC
5	IO_L22N_5	AB7	NC	NC
5	IO_L22P_5	AA7	NC	NC
5	IO_L21N_5/VREF_5	Y7	NC	NC
5	IO_L21P_5	W7	NC	NC
5	IO_L19N_5	AB6	NC	NC
5	IO_L19P_5	AA6	NC	NC
5	IO_L06N_5	Y6		

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
2	IO_L45N_2	H23		
2	IO_L45P_2/VREF_2	H24		
2	IO_L46N_2	J21		
2	IO_L46P_2	J20		
2	IO_L48N_2	H25		
2	IO_L48P_2	H26		
2	IO_L49N_2	J22		
2	IO_L49P_2	J23		
2	IO_L51N_2	K21		
2	IO_L51P_2/VREF_2	K22		
2	IO_L52N_2	K20		
2	IO_L52P_2	L20		
2	IO_L54N_2	J24		
2	IO_L54P_2	J25		
2	IO_L67N_2	K23		
2	IO_L67P_2	K24		
2	IO_L69N_2	J26		
2	IO_L69P_2/VREF_2	K26		
2	IO_L70N_2	L22		
2	IO_L70P_2	L21		
2	IO_L72N_2	L25		
2	IO_L72P_2	L26		
2	IO_L73N_2	L19	NC	
2	IO_L73P_2	M19	NC	
2	IO_L75N_2	L23	NC	
2	IO_L75P_2/VREF_2	L24	NC	
2	IO_L76N_2	M22	NC	
2	IO_L76P_2	M21	NC	
2	IO_L78N_2	M23	NC	
2	IO_L78P_2	M24	NC	
2	IO_L91N_2	M25		
2	IO_L91P_2	M26		
2	IO_L93N_2	M20		
2	IO_L93P_2/VREF_2	N20		
2	IO_L94N_2	N22		
2	IO_L94P_2	N21		
2	IO_L96N_2	N24		

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
5	IO_L52N_5	AA9		
5	IO_L52P_5	Y9		
5	IO_L51N_5/VREF_5	W9		
5	IO_L51P_5	V9		
5	IO_L49N_5	AD8		
5	IO_L49P_5	AD6		
5	IO_L24N_5	AC8		
5	IO_L24P_5	AC7		
5	IO_L22N_5	AB8		
5	IO_L22P_5	AA8		
5	IO_L21N_5/VREF_5	W8		
5	IO_L21P_5	Y8		
5	IO_L19N_5	AD5		
5	IO_L19P_5	AD4		
5	IO_L06N_5	AC6		
5	IO_L06P_5	AC5		
5	IO_L05N_5/VRP_5	AB7		
5	IO_L05P_5/VRN_5	AA7		
5	IO_L04N_5	AB5		
5	IO_L04P_5/VREF_5	AA5		
5	IO_L03N_5/D4/ALT_VRP_5	AA6		
5	IO_L03P_5/D5/ALT_VRN_5	Y6		
5	IO_L02N_5/D6	Y7		
5	IO_L02P_5/D7	W7		
5	IO_L01N_5/RDWR_B	V8		
5	IO_L01P_5/CS_B	U9		
6	IO_L01P_6	AB2		
6	IO_L01N_6	AB1		
6	IO_L02P_6/VRN_6	AA3		
6	IO_L02N_6/VRP_6	AA2		
6	IO_L03P_6	Y4		
6	IO_L03N_6/VREF_6	Y3		
6	IO_L04P_6	W4		
6	IO_L04N_6	W5		
6	IO_L06P_6	V5		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
2	IO_L78P_2	P5	NC	NC
2	IO_L91N_2	R2		
2	IO_L91P_2	P2		
2	IO_L92N_2	P8		
2	IO_L92P_2	R8		
2	IO_L93N_2	P4		
2	IO_L93P_2/VREF_2	R4		
2	IO_L94N_2	R1		
2	IO_L94P_2	T2		
2	IO_L95N_2	R7		
2	IO_L95P_2	R6		
2	IO_L96N_2	R3		
2	IO_L96P_2	P3		
3	IO_L96N_3	T7		
3	IO_L96P_3	T6		
3	IO_L95N_3	U1		
3	IO_L95P_3	V1		
3	IO_L94N_3	T3		
3	IO_L94P_3	U3		
3	IO_L93N_3/VREF_3	T8		
3	IO_L93P_3	U8		
3	IO_L92N_3	U2		
3	IO_L92P_3	V2		
3	IO_L91N_3	T4		
3	IO_L91P_3	U4		
3	IO_L78N_3	U9	NC	NC
3	IO_L78P_3	T9	NC	NC
3	IO_L77N_3	W1	NC	NC
3	IO_L77P_3	Y1	NC	NC
3	IO_L76N_3	T5	NC	NC
3	IO_L76P_3	U5	NC	NC
3	IO_L75N_3/VREF_3	U6	NC	NC
3	IO_L75P_3	V6	NC	NC
3	IO_L74N_3	W2	NC	NC
3	IO_L74P_3	Y2	NC	NC
3	IO_L73N_3	V4	NC	NC

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
6	IO_L20P_6	AE26		
6	IO_L20N_6	AD26		
6	IO_L21P_6	AG30		
6	IO_L21N_6/VREF_6	AF30		
6	IO_L22P_6	AD25		
6	IO_L22N_6	AC25		
6	IO_L23P_6	AE28		
6	IO_L23N_6	AD28		
6	IO_L24P_6	AD29		
6	IO_L24N_6	AE29		
6	IO_L43P_6	AC24		
6	IO_L43N_6	AB24		
6	IO_L44P_6	AD27		
6	IO_L44N_6	AC27		
6	IO_L45P_6	AC26		
6	IO_L45N_6/VREF_6	AB26		
6	IO_L46P_6	AA23		
6	IO_L46N_6	Y23		
6	IO_L47P_6	AC28		
6	IO_L47N_6	AB28		
6	IO_L48P_6	AD30		
6	IO_L48N_6	AE30		
6	IO_L49P_6	AB25		
6	IO_L49N_6	AA25		
6	IO_L50P_6	AA24		
6	IO_L50N_6	Y24		
6	IO_L51P_6	AC29		
6	IO_L51N_6/VREF_6	AB30		
6	IO_L52P_6	Y25		
6	IO_L52N_6	W25		
6	IO_L53P_6	AB27		
6	IO_L53N_6	AA27		
6	IO_L54P_6	AA29		
6	IO_L54N_6	AB29		
6	IO_L67P_6	W23	NC	
6	IO_L67N_6	V23	NC	
6	IO_L68P_6	AA26	NC	

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
7	IO_L95N_7	R24		
7	IO_L94P_7	R29		
7	IO_L94N_7	T29		
7	IO_L93P_7/VREF_7	R27		
7	IO_L93N_7	P27		
7	IO_L92P_7	R23		
7	IO_L92N_7	P23		
7	IO_L91P_7	N30		
7	IO_L91N_7	P30		
7	IO_L78P_7	P26	NC	NC
7	IO_L78N_7	R26	NC	NC
7	IO_L77P_7	R22	NC	NC
7	IO_L77N_7	P22	NC	NC
7	IO_L76P_7	N29	NC	NC
7	IO_L76N_7	P29	NC	NC
7	IO_L75P_7/VREF_7	N27	NC	NC
7	IO_L75N_7	N26	NC	NC
7	IO_L74P_7	P25	NC	NC
7	IO_L74N_7	N25	NC	NC
7	IO_L73P_7	L30	NC	NC
7	IO_L73N_7	M30	NC	NC
7	IO_L72P_7	L28	NC	
7	IO_L72N_7	M28	NC	
7	IO_L71P_7	N24	NC	
7	IO_L71N_7	M24	NC	
7	IO_L70P_7	L29	NC	
7	IO_L70N_7	M29	NC	
7	IO_L69P_7/VREF_7	M27	NC	
7	IO_L69N_7	L27	NC	
7	IO_L68P_7	N23	NC	
7	IO_L68N_7	M23	NC	
7	IO_L67P_7	J30	NC	
7	IO_L67N_7	K30	NC	
7	IO_L54P_7	K26		
7	IO_L54N_7	L26		
7	IO_L53P_7	M25		
7	IO_L53N_7	L25		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
2	VCCO_2	L10		
2	VCCO_2	L9		
2	VCCO_2	K9		
2	VCCO_2	E2		
3	VCCO_3	AF2		
3	VCCO_3	AA9		
3	VCCO_3	Y10		
3	VCCO_3	Y9		
3	VCCO_3	W10		
3	VCCO_3	W9		
3	VCCO_3	V10		
3	VCCO_3	V9		
3	VCCO_3	V3		
3	VCCO_3	U10		
3	VCCO_3	T10		
4	VCCO_4	AJ5		
4	VCCO_4	AH13		
4	VCCO_4	AB13		
4	VCCO_4	AB12		
4	VCCO_4	AB11		
4	VCCO_4	AB10		
4	VCCO_4	AA15		
4	VCCO_4	AA14		
4	VCCO_4	AA13		
4	VCCO_4	AA12		
4	VCCO_4	AA11		
5	VCCO_5	AJ26		
5	VCCO_5	AH18		
5	VCCO_5	AB21		
5	VCCO_5	AB20		
5	VCCO_5	AB19		
5	VCCO_5	AB18		
5	VCCO_5	AA20		
5	VCCO_5	AA19		
5	VCCO_5	AA18		
5	VCCO_5	AA17		
5	VCCO_5	AA16		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
1	IO_L09N_1/VREF_1	G9	NC	
1	IO_L09P_1	G10	NC	
1	IO_L08N_1	K13	NC	
1	IO_L08P_1	K12	NC	
1	IO_L07N_1	A4	NC	
1	IO_L07P_1	A5	NC	
1	IO_L06N_1	F8		
1	IO_L06P_1	E8		
1	IO_L05N_1	J11		
1	IO_L05P_1	K11		
1	IO_L04N_1	C5		
1	IO_L04P_1/VREF_1	C6		
1	IO_L03N_1/VRP_1	D6		
1	IO_L03P_1/VRN_1	D7		
1	IO_L02N_1	H10		
1	IO_L02P_1	J10		
1	IO_L01N_1	C4		
1	IO_L01P_1	B4		
2	IO_L01N_2	E3		
2	IO_L01P_2	D2		
2	IO_L02N_2/VRP_2	L13		
2	IO_L02P_2/VRN_2	M13		
2	IO_L03N_2	F4		
2	IO_L03P_2/VREF_2	E4		
2	IO_L04N_2	E1		
2	IO_L04P_2	D1		
2	IO_L05N_2	L12		
2	IO_L05P_2	M11		
2	IO_L06N_2	G6		
2	IO_L06P_2	F5		
2	IO_L07N_2	F2	NC	
2	IO_L07P_2	E2	NC	
2	IO_L08N_2	M12	NC	
2	IO_L08P_2	N12	NC	
2	IO_L09N_2	H6	NC	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
4	IO_L08P_4	AL12	NC	
4	IO_L09N_4	AP9	NC	
4	IO_L09P_4/VREF_4	AP8	NC	
4	IO_L10N_4	AV6	NC	
4	IO_L10P_4	AV5	NC	
4	IO_L11N_4	AM11	NC	
4	IO_L11P_4	AM12	NC	
4	IO_L12N_4	AN10	NC	
4	IO_L12P_4	AN9	NC	
4	IO_L19N_4	AU8		
4	IO_L19P_4	AU7		
4	IO_L20N_4	AH14		
4	IO_L20P_4	AH15		
4	IO_L21N_4	AT8		
4	IO_L21P_4/VREF_4	AT7		
4	IO_L22N_4	AW7		
4	IO_L22P_4	AW6		
4	IO_L23N_4	AK13		
4	IO_L23P_4	AK14		
4	IO_L24N_4	AR10		
4	IO_L24P_4	AR9		
4	IO_L25N_4	AV8		
4	IO_L25P_4	AV7		
4	IO_L26N_4	AJ14		
4	IO_L26P_4	AJ15		
4	IO_L27N_4	AP11		
4	IO_L27P_4/VREF_4	AP10		
4	IO_L28N_4	AU10		
4	IO_L28P_4	AU9		
4	IO_L29N_4	AL13		
4	IO_L29P_4	AL14		
4	IO_L30N_4	AN12		
4	IO_L30P_4	AN11		
4	IO_L31N_4	AW9	NC	
4	IO_L31P_4	AW8	NC	
4	IO_L32N_4	AM13	NC	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
4	IO_L91P_4	AV18		
4	IO_L92N_4	AH20		
4	IO_L92P_4	AJ20		
4	IO_L93N_4	AR19		
4	IO_L93P_4	AT18		
4	IO_L94N_4/VREF_4	AW19		
4	IO_L94P_4	AW18		
4	IO_L95N_4/GCLK3S	AL20		
4	IO_L95P_4/GCLK2P	AM20		
4	IO_L96N_4/GCLK1S	AU19		
4	IO_L96P_4/GCLK0P	AT19		
5	IO_L96N_5/GCLK7S	AP21		
5	IO_L96P_5/GCLK6P	AP20		
5	IO_L95N_5/GCLK5S	AN21		
5	IO_L95P_5/GCLK4P	AN22		
5	IO_L94N_5	AU21		
5	IO_L94P_5/VREF_5	AU20		
5	IO_L93N_5	AR21		
5	IO_L93P_5	AR20		
5	IO_L92N_5	AM21		
5	IO_L92P_5	AM22		
5	IO_L91N_5	AW22		
5	IO_L91P_5/VREF_5	AW21		
5	IO_L85N_5	AV22	NC	NC
5	IO_L85P_5	AV21	NC	NC
5	IO_L84N_5	AT22		
5	IO_L84P_5	AT21		
5	IO_L83N_5	AL21		
5	IO_L83P_5	AL22		
5	IO_L82N_5	AW24		
5	IO_L82P_5	AW23		
5	IO_L81N_5/VREF_5	AR23		
5	IO_L81P_5	AR22		
5	IO_L80N_5	AK21		
5	IO_L80P_5	AK22		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
6	IO_L23N_6	AM38		
6	IO_L24P_6	AM36		
6	IO_L24N_6	AN36		
6	IO_L25P_6	AH30		
6	IO_L25N_6	AG30		
6	IO_L26P_6	AM37		
6	IO_L26N_6	AL37		
6	IO_L27P_6	AK34		
6	IO_L27N_6/VREF_6	AL34		
6	IO_L28P_6	AG29		
6	IO_L28N_6	AF29		
6	IO_L29P_6	AL35		
6	IO_L29N_6	AK35		
6	IO_L30P_6	AH33		
6	IO_L30N_6	AJ33		
6	IO_L31P_6	AJ32	NC	
6	IO_L31N_6	AH32	NC	
6	IO_L32P_6	AM39	NC	
6	IO_L32N_6	AL39	NC	
6	IO_L33P_6	AK36	NC	
6	IO_L33N_6/VREF_6	AL36	NC	
6	IO_L34P_6	AF28	NC	
6	IO_L34N_6	AE28	NC	
6	IO_L35P_6	AL38	NC	
6	IO_L35N_6	AK38	NC	
6	IO_L36P_6	AH34	NC	
6	IO_L36N_6	AJ34	NC	
6	IO_L43P_6	AG31		
6	IO_L43N_6	AF31		
6	IO_L44P_6	AK37		
6	IO_L44N_6	AJ37		
6	IO_L45P_6	AH36		
6	IO_L45N_6/VREF_6	AJ36		
6	IO_L46P_6	AF30		
6	IO_L46N_6	AE30		
6	IO_L47P_6	AK39		

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
4	IO_L29N_4	AL6	NC
4	IO_L29P_4	AL7	NC
4	IO_L30N_4	AJ9	NC
4	IO_L30P_4	AJ10	NC
4	IO_L49N_4	AE11	
4	IO_L49P_4	AE12	
4	IO_L50N_4	AG10	
4	IO_L50P_4	AG11	
4	IO_L51N_4	AL8	
4	IO_L51P_4/VREF_4	AL9	
4	IO_L52N_4	AF12	
4	IO_L52P_4	AF13	
4	IO_L53N_4	AK9	
4	IO_L53P_4	AK10	
4	IO_L54N_4	AH11	
4	IO_L54P_4	AH12	
4	IO_L67N_4	AC12	
4	IO_L67P_4	AC13	
4	IO_L68N_4	AG12	
4	IO_L68P_4	AG13	
4	IO_L69N_4	AL10	
4	IO_L69P_4/VREF_4	AL11	
4	IO_L70N_4	AD13	
4	IO_L70P_4	AD15	
4	IO_L71N_4	AJ11	
4	IO_L71P_4	AJ12	
4	IO_L72N_4	AK11	
4	IO_L72P_4	AK12	
4	IO_L73N_4	AE14	
4	IO_L73P_4	AE15	
4	IO_L74N_4	AF14	
4	IO_L74P_4	AF15	
4	IO_L75N_4	AL12	
4	IO_L75P_4/VREF_4	AL13	
4	IO_L76N_4	AB14	
4	IO_L76P_4	AC14	
4	IO_L77N_4	AH13	
4	IO_L77P_4	AH14	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
4	IO_L78N_4	AJ13	
4	IO_L78P_4	AK13	
4	IO_L91N_4/VREF_4	AC15	
4	IO_L91P_4	AC16	
4	IO_L92N_4	AG14	
4	IO_L92P_4	AG15	
4	IO_L93N_4	AK14	
4	IO_L93P_4	AK15	
4	IO_L94N_4/VREF_4	AF16	
4	IO_L94P_4	AG16	
4	IO_L95N_4/GCLK3S	AL14	
4	IO_L95P_4/GCLK2P	AL15	
4	IO_L96N_4/GCLK1S	AH15	
4	IO_L96P_4/GCLK0P	AJ15	
5	IO_L96N_5/GCLK7S	AJ16	
5	IO_L96P_5/GCLK6P	AH17	
5	IO_L95N_5/GCLK5S	AD16	
5	IO_L95P_5/GCLK4P	AD17	
5	IO_L94N_5	AL17	
5	IO_L94P_5/VREF_5	AL18	
5	IO_L93N_5	AG17	
5	IO_L93P_5	AF17	
5	IO_L92N_5	AE17	
5	IO_L92P_5	AE18	
5	IO_L91N_5	AK17	
5	IO_L91P_5/VREF_5	AJ17	
5	IO_L78N_5	AK18	
5	IO_L78P_5	AK19	
5	IO_L77N_5	AC17	
5	IO_L77P_5	AB18	
5	IO_L76N_5	AH18	
5	IO_L76P_5	AH19	
5	IO_L75N_5/VREF_5	AL19	
5	IO_L75P_5	AL20	
5	IO_L74N_5	AC18	
5	IO_L74P_5	AC19	
5	IO_L73N_5	AJ19	