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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	64
Number of Logic Elements/Cells	-
Total RAM Bits	73728
Number of I/O	88
Number of Gates	40000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-TFBGA, CSPBGA
Supplier Device Package	144-LCSBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v40-4csg144c

Summary of Virtex-II™ Features

- Industry First Platform FPGA Solution
- IP-Immersion Architecture
 - Densities from 40K to 8M system gates
 - 420 MHz internal clock speed (Advance Data)
 - 840+ Mb/s I/O (Advance Data)
- SelectRAM™ Memory Hierarchy
 - 3 Mb of dual-port RAM in 18 Kbit block SelectRAM resources
 - Up to 1.5 Mb of distributed SelectRAM resources
- High-Performance Interfaces to External Memory
 - DRAM interfaces
 - SDR / DDR SDRAM
 - Network FCRAM
 - Reduced Latency DRAM
 - SRAM interfaces
 - SDR / DDR SRAM
 - QDR™ SRAM
 - CAM interfaces
- Arithmetic Functions
 - Dedicated 18-bit x 18-bit multiplier blocks
 - Fast look-ahead carry logic chains
- Flexible Logic Resources
 - Up to 93,184 internal registers / latches with Clock Enable
 - Up to 93,184 look-up tables (LUTs) or cascadable 16-bit shift registers
 - Wide multiplexers and wide-input function support
 - Horizontal cascade chain and sum-of-products support
 - Internal 3-state bussing
- High-Performance Clock Management Circuitry
 - Up to 12 DCM (Digital Clock Manager) modules
 - Precise clock de-skew
 - Flexible frequency synthesis
 - High-resolution phase shifting
 - 16 global clock multiplexer buffers
- Active Interconnect Technology
 - Fourth generation segmented routing structure
 - Predictable, fast routing delay, independent of fanout
- SelectIO™-Ultra Technology
 - Up to 1,108 user I/Os
 - 19 single-ended and six differential standards
 - Programmable sink current (2 mA to 24 mA) per I/O
 - Digitally Controlled Impedance (DCI) I/O: on-chip termination resistors for single-ended I/O standards
 - PCI-X compatible (133 MHz and 66 MHz) at 3.3V
 - PCI compliant (66 MHz and 33 MHz) at 3.3V
 - CardBus compliant (33 MHz) at 3.3V
 - Differential Signaling
 - 840 Mb/s Low-Voltage Differential Signaling I/O (LVDS) with current mode drivers
 - Bus LVDS I/O
 - Lightning Data Transport (LDT) I/O with current driver buffers
 - Low-Voltage Positive Emitter-Coupled Logic (LVPECL) I/O
 - Built-in DDR input and output registers
 - Proprietary high-performance SelectLink Technology
 - High-bandwidth data path
 - Double Data Rate (DDR) link
 - Web-based HDL generation methodology
- Supported by Xilinx Foundation™ and Alliance Series™ Development Systems
 - Integrated VHDL and Verilog design flows
 - Compilation of 10M system gates designs
 - Internet Team Design (ITD) tool
- SRAM-Based In-System Configuration
 - Fast SelectMAP configuration
 - Triple Data Encryption Standard (DES) security option (Bitstream Encryption)
 - IEEE 1532 support
 - Partial reconfiguration
 - Unlimited reprogrammability
 - Readback capability
- 0.15 µm 8-Layer Metal Process with 0.12 µm High-Speed Transistors
- 1.5V (V_{CCINT}) Core Power Supply, Dedicated 3.3V V_{CCAUX} Auxiliary and V_{CCO} I/O Power Supplies
- IEEE 1149.1 Compatible Boundary-Scan Logic Support
- Flip-Chip and Wire-Bond Ball Grid Array (BGA) Packages in Three Standard Fine Pitches (0.80 mm, 1.00 mm, and 1.27 mm)
- Wire-Bond BGA Devices Available in Pb-Free Packaging (www.xilinx.com/pbfree)
- 100% Factory Tested

Table 5: Minimum Power On Current Required for Virtex-II Devices

	Device (mA)							
	XC2V40, XC2V80, XC2V250, XC2V500	XC2V1000	XC2V1500	XC2V2000	XC2V3000	XC2V4000	XC2V6000	XC2V8000
$I_{CCINTMIN}$	200	250	350	400	500	650	800	1100
$I_{CCAUXMIN}$	100	100	100	100	100	100	100	100
I_{CCOMIN}	50	50	100	100	100	100	100	100

Notes:

- Values specified for power on current parameters are Commercial Grade. For Industrial Grade values, multiply Commercial Grade values by 1.25.
- I_{CCOMIN} values listed here apply to the entire device (all banks).

General Power Supply Requirements

Proper decoupling of all FPGA power supplies is essential. Consult Xilinx Application Note [XAPP623](#) for detailed information on power distribution system design.

V_{CCAUX} powers critical resources in the FPGA. Thus, V_{CCAUX} is especially susceptible to power supply noise.

Changes in V_{CCAUX} voltage outside of 200 mV peak to peak should take place at a rate no faster than 10 mV per millisecond. Techniques to help reduce jitter and period distortion are provided in Xilinx Answer Record 13756, available at [www.support.xilinx.com](#).

V_{CCAUX} can share a power plane with 3.3V V_{CCO} , but only if V_{CCO} does not have excessive noise. Using simultaneously switching output (SSO) limits are essential for keeping power supply noise to a minimum. Refer to [XAPP689](#), "Managing Ground Bounce in Large FPGAs," to determine the number of simultaneously switching outputs allowed per bank at the package level.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 6: DC Input and Output Levels

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTL ⁽¹⁾	-0.5	0.8	2.0	3.6	0.4	2.4	24	-24
LVC MOS33	-0.5	0.8	2.0	3.6	0.4	$V_{CCO} - 0.4$	24	-24
LVC MOS25	-0.5	0.7	1.7	2.7	0.4	$V_{CCO} - 0.4$	24	-24
LVC MOS18	-0.5	35% V_{CCO}	65% V_{CCO}	1.95	0.4	$V_{CCO} - 0.4$	16	-16
LVC MOS15	-0.5	35% V_{CCO}	65% V_{CCO}	1.7	0.4	$V_{CCO} - 0.4$	16	-16
PCI33_3	-0.5	30% V_{CCO}	50% V_{CCO}	$V_{CCO} + 0.5$	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
PCI66_3	-0.5	30% V_{CCO}	50% V_{CCO}	$V_{CCO} + 0.5$	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
PCI-X	-0.5	Note 2	Note 2	Note 2	Note 2	Note 2	Note 2	Note 2
GTLP	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCO} + 0.5$	0.6	n/a	36	n/a
GTL	-0.5	$V_{REF} - 0.05$	$V_{REF} + 0.05$	$V_{CCO} + 0.5$	0.4	n/a	40	n/a
HSTL I	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCO} + 0.5$	0.4	$V_{CCO} - 0.4$	8	-8
HSTL II	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCO} + 0.5$	0.4	$V_{CCO} - 0.4$	16	-16
HSTL III	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCO} + 0.5$	0.4	$V_{CCO} - 0.4$	24	-8
HSTL IV	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCO} + 0.5$	0.4	$V_{CCO} - 0.4$	48	-8

IOB Input Switching Characteristics Standard Adjustments

Table 15 gives all standard-specific data input delay adjustments.

Table 15: IOB Input Switching Characteristics Standard Adjustments

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-6	-5	-4	
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL	T_{ILVTTL}	0.00	0.00	0.00	ns
LVC MOS (Low-Voltage CMOS), 3.3V	LVC MOS33	$T_{ILVCMOS33}$	0.00	0.00	0.00	ns
LVC MOS, 2.5V	LVC MOS25	$T_{ILVCMOS25}$	0.11	0.11	0.12	ns
LVC MOS, 1.8V	LVC MOS18	$T_{ILVCMOS18}$	0.42	0.43	0.49	ns
LVC MOS, 1.5V	LVC MOS15	$T_{ILVCMOS15}$	0.98	1.00	1.15	ns
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	T_{ILVDS_25}	0.60	0.60	0.69	ns
LVDS, 3.3V	LVDS_33	T_{ILVDS_33}	0.60	0.60	0.69	ns
LVDSEXT (Extended Mode), 2.5V	LVDSEXT_25	$T_{ILVDSEXT_25}$	0.68	0.69	0.79	ns
LVDSEXT, 3.3V	LVDSEXT_33	$T_{ILVDSEXT_33}$	0.56	0.56	0.65	ns
ULVDS (Ultra LVDS), 2.5V	ULVDS_25	T_{IULVDS_25}	0.48	0.49	0.56	ns
BLVDS (Bus LVDS), 2.5V	BLVDS_25	T_{IBLVDS_25}	0.68	0.69	0.79	ns
LDT (HyperTransport), 2.5V	LDT_25	$T_{ILD T_25}$	0.48	0.49	0.56	ns
LVPECL (Low-Voltage Positive Electron-Coupled Logic), 3.3V	LVPECL_33	$T_{ILVPECL_33}$	0.60	0.60	0.69	ns
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3	T_{IPCI33_3}	0.00	0.00	0.00	ns
PCI, 66 MHz, 3.3V	PCI66_3	T_{IPCI66_3}	0.00	0.00	0.00	ns
PCI-X, 133 MHz, 3.3V	PCIX	T_{IPCIX}	0.00	0.00	0.00	ns
GTL (Gunning Transceiver Logic)	GTL	T_{IGTL}	0.42	0.42	0.48	ns
GTL Plus	GTLP	T_{IGTLP}	0.42	0.42	0.48	ns
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	T_{IHSTL_I}	0.42	0.42	0.48	ns
HSTL, Class II	HSTL_II	T_{IHSTL_II}	0.42	0.42	0.48	ns
HSTL, Class III	HSTL_III	T_{IHSTL_III}	0.42	0.42	0.48	ns
HSTL, Class IV	HSTL_IV	T_{IHSTL_IV}	0.42	0.42	0.48	ns
HSTL, Class I, 1.8V	HSTL_I_18	$T_{IHSTL_I_18}$	0.42	0.42	0.48	ns
HSTL, Class II, 1.8V	HSTL_II_18	$T_{IHSTL_II_18}$	0.42	0.42	0.48	ns
HSTL, Class III, 1.8V	HSTL_III_18	$T_{IHSTL_III_18}$	0.42	0.42	0.48	ns
HSTL, Class IV, 1.8V	HSTL_IV_18	$T_{IHSTL_IV_18}$	0.42	0.42	0.48	ns
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	$T_{ISSTL18_I}$	0.42	0.42	0.48	ns
SSTL, Class II, 1.8V	SSTL18_II	$T_{ISSTL18_II}$	0.42	0.42	0.48	ns
SSTL, Class I, 2.5V	SSTL2_I	T_{ISSTL2_I}	0.42	0.42	0.48	ns
SSTL, Class II, 2.5V	SSTL2_II	T_{ISSTL2_II}	0.42	0.42	0.48	ns
SSTL, Class I, 3.3V	SSTL3_I	T_{ISSTL3_I}	0.35	0.35	0.40	ns
SSTL, Class II, 3.3V	SSTL3_II	T_{ISSTL3_II}	0.35	0.35	0.40	ns
AGP-2X/AGP (Accelerated Graphics Port)	AGP	T_{IAGP}	0.35	0.35	0.40	ns
LVDCI (Low-Voltage Digitally Controlled Impedance), 3.3V	LVDCI_33	T_{ILVDCI_33}	0.00	0.00	0.00	ns
LVDCI, 2.5V	LVDCI_25	T_{ILVDCI_25}	0.11	0.11	0.12	ns
LVDCI, 1.8V	LVDCI_18	T_{ILVDCI_18}	0.42	0.43	0.49	ns
LVDCI, 1.5V	LVDCI_15	T_{ILVDCI_15}	0.98	1.00	1.14	ns

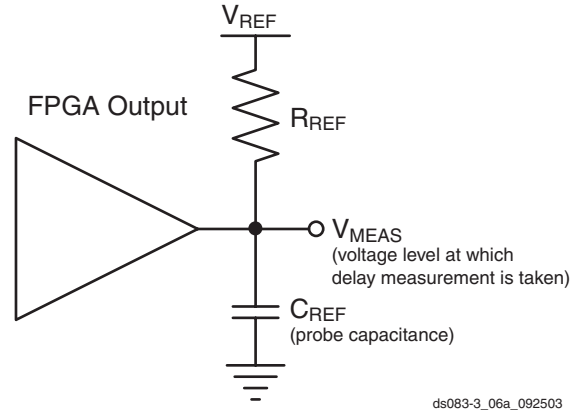
Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. (See [Virtex-II Platform FPGA User Guide](#) for details.) The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setup shown in **Figure 1**.

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. (IBIS models can be found on the web at http://support.xilinx.com/support/sw_ibis.htm.) Parameters V_{REF} , R_{REF} , C_{REF} , and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from **Table 19**.
2. Record the time to V_{MEAS} .
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.

4. Record the time to V_{MEAS} .
5. Compare the results of steps 2 and 4. The increase or decrease in delay should be added to or subtracted from the I/O Output Standard Adjustment value (**Table 17**) to yield the actual worst-case propagation delay (clock-to-input) of the PCB trace.



ds083-3_06a_092503

Figure 1: Generalized Test Setup

Table 19: Output Delay Measurement Methodology

Description	IOSTANDARD Attribute	R_{REF} (Ω)	$C_{REF}^{(1)}$ (pF)	V_{MEAS} (V)	V_{REF} (V)
LVTTTL (Low-Voltage Transistor-Transistor Logic)	LVTTTL (all)	1M	0	1.4	0
LVC MOS (Low-Voltage CMOS), 3.3V	LVC MOS33	1M	0	1.65	0
LVC MOS, 2.5V	LVC MOS25	1M	0	1.25	0
LVC MOS, 1.8V	LVC MOS18	1M	0	0.9	0
LVC MOS, 1.5V	LVC MOS15	1M	0	0.75	0
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3 (rising edge)	25	$10^{(2)}$	0.94	0
	PCI33_3 (falling edge)	25	$10^{(2)}$	2.03	3.3
PCI, 66 MHz, 3.3V	PCI66_3 (rising edge)	25	$10^{(2)}$	0.94	0
	PCI66_3 (falling edge)	25	$10^{(2)}$	2.03	3.3
PCI-X, 133 MHz, 3.3V	PCIX (rising edge)	25	$10^{(3)}$	0.94	
	PCIX (falling edge)	25	$10^{(3)}$	2.03	3.3
GTL (Gunning Transceiver Logic)	GTL	25	0	0.8	1.2
GTL Plus	GTLP	25	0	1.0	1.5
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class III	HSTL_III	50	0	0.9	1.5
HSTL, Class IV	HSTL_IV	25	0	0.9	1.5
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSTL, Class III, 1.8V	HSTL_III_18	50	0	1.1	1.8
HSTL, Class IV, 1.8V	HSTL_IV_18	25	0	1.1	1.8

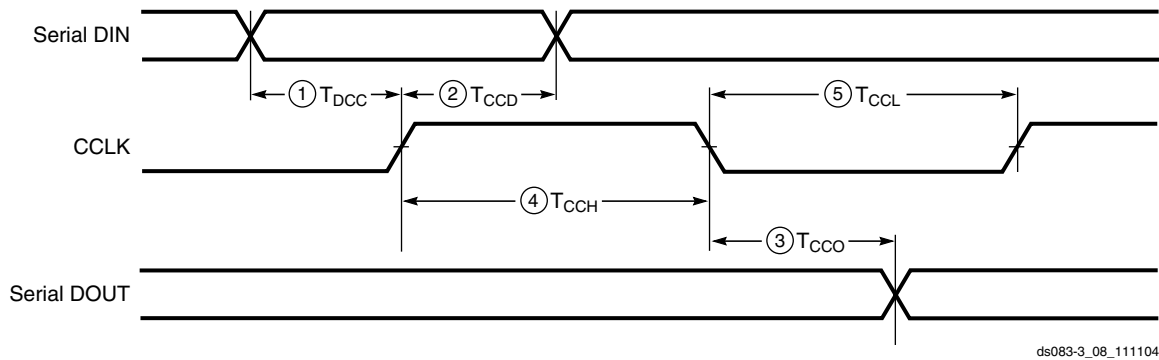


Figure 3: Slave Serial Mode Timing Sequence

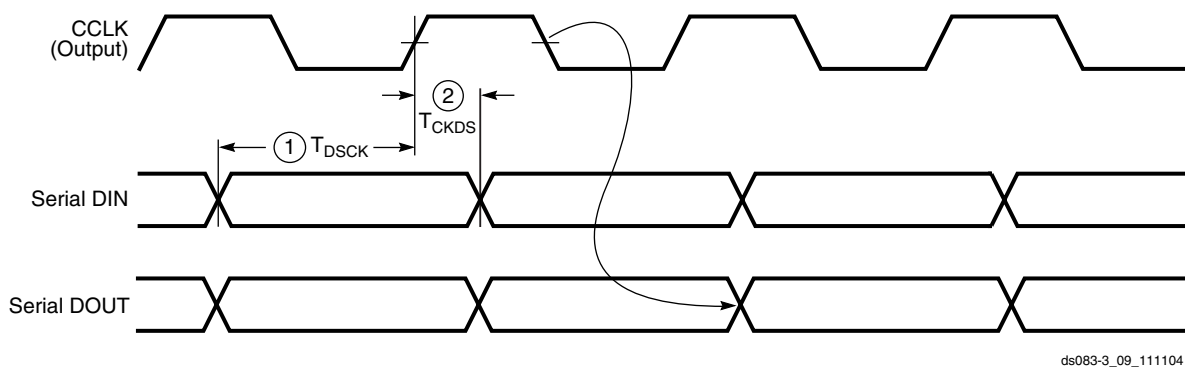


Figure 4: Master Serial Mode Timing Sequence

Table 31: Master/Slave Serial Mode Timing Characteristics

	Description	Figure References	Symbol	Value	Units
CCLK	DIN setup/hold, slave mode (Figure 3)	1/2	T_{DCC}/T_{CCD}	5.0/0.0	ns, min
	DIN setup/hold, master mode (Figure 4)	1/2	T_{DSCK}/T_{CKDS}	5.0/0.0	ns, min
	DOUT	3	T_{CCO}	12.0	ns, max
	High time	4	T_{CCH}	5.0	ns, min
	Low time	5	T_{CCL}	5.0	ns, min
	Maximum start-up frequency		$F_{CC_STARTUP}$	50	MHz, max
	Maximum frequency		F_{CC_SERIAL}	66 ⁽¹⁾	MHz, max
	Frequency tolerance, master mode with respect to nominal			+45% -30%	

Notes:

1. If no provision is made in the design to adjust the frequency of CCLK, F_{CC_SERIAL} should not exceed $F_{CC_STARTUP}$.

Master/Slave SelectMAP Parameters

Figure 5 is a generic timing diagram for data loading using SelectMAP. For other data loading diagrams, refer to the [Virtex-II Pro Platform FPGA User Guide](#).

Table 7: FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
0	IO_L93N_0	B10		
0	IO_L93P_0	A10		
0	IO_L94N_0/VREF_0	E11		
0	IO_L94P_0	F11		
0	IO_L95N_0/GCLK7P	D11		
0	IO_L95P_0/GCLK6S	C11		
0	IO_L96N_0/GCLK5P	B11		
0	IO_L96P_0/GCLK4S	A11		
1	IO_L96N_1/GCLK3P	F12		
1	IO_L96P_1/GCLK2S	F13		
1	IO_L95N_1/GCLK1P	E12		
1	IO_L95P_1/GCLK0S	D12		
1	IO_L94N_1	C12		
1	IO_L94P_1/VREF_1	B12		
1	IO_L93N_1	A13		
1	IO_L93P_1	B13		
1	IO_L92N_1	C13		
1	IO_L92P_1	D13		
1	IO_L91N_1	E13		
1	IO_L91P_1/VREF_1	E14		
1	IO_L54N_1	A14	NC	
1	IO_L54P_1	B14	NC	
1	IO_L52N_1	C14	NC	
1	IO_L52P_1	D14	NC	
1	IO_L51N_1/VREF_1	A15	NC	
1	IO_L51P_1	B15	NC	
1	IO_L49N_1	C15	NC	
1	IO_L49P_1	D15	NC	
1	IO_L24N_1	F14	NC	NC
1	IO_L24P_1	E15	NC	NC
1	IO_L22N_1	A16	NC	NC
1	IO_L22P_1	B16	NC	NC
1	IO_L21N_1/VREF_1	C16	NC	NC

Table 7: FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
2	IO_L45N_2	H19		
2	IO_L45P_2/VREF_2	H20		
2	IO_L46N_2	H21		
2	IO_L46P_2	H22		
2	IO_L48N_2	J17		
2	IO_L48P_2	J18		
2	IO_L49N_2	J19	NC	
2	IO_L49P_2	J20	NC	
2	IO_L51N_2	J21	NC	
2	IO_L51P_2/VREF_2	J22	NC	
2	IO_L52N_2	K17	NC	
2	IO_L52P_2	K18	NC	
2	IO_L54N_2	K19	NC	
2	IO_L54P_2	K20	NC	
2	IO_L91N_2	K21		
2	IO_L91P_2	K22		
2	IO_L93N_2	L17		
2	IO_L93P_2/VREF_2	L18		
2	IO_L94N_2	L19		
2	IO_L94P_2	L20		
2	IO_L96N_2	L21		
2	IO_L96P_2	L22		
3	IO_L96N_3	M21		
3	IO_L96P_3	M20		
3	IO_L94N_3	M19		
3	IO_L94P_3	M18		
3	IO_L93N_3/VREF_3	M17		
3	IO_L93P_3	N17		
3	IO_L91N_3	N22		
3	IO_L91P_3	N21		
3	IO_L54N_3	N20	NC	
3	IO_L54P_3	N19	NC	
3	IO_L52N_3	N18	NC	

Table 7: FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
4	IO_L95N_4/GCLK3S	W12		
4	IO_L95P_4/GCLK2P	Y12		
4	IO_L96N_4/GCLK1S	AA12		
4	IO_L96P_4/GCLK0P	AB12		
5	IO_L96N_5/GCLK7S	AA11		
5	IO_L96P_5/GCLK6P	Y11		
5	IO_L95N_5/GCLK5S	W11		
5	IO_L95P_5/GCLK4P	V11		
5	IO_L94N_5	U11		
5	IO_L94P_5/VREF_5	U10		
5	IO_L93N_5	AB10		
5	IO_L93P_5	AA10		
5	IO_L92N_5	Y10		
5	IO_L92P_5	W10		
5	IO_L91N_5	V10		
5	IO_L91P_5/VREF_5	V9		
5	IO_L54N_5	AB9	NC	
5	IO_L54P_5	AA9	NC	
5	IO_L52N_5	Y9	NC	
5	IO_L52P_5	W9	NC	
5	IO_L51N_5/VREF_5	AB8	NC	
5	IO_L51P_5	AA8	NC	
5	IO_L49N_5	Y8	NC	
5	IO_L49P_5	W8	NC	
5	IO_L24N_5	U9	NC	NC
5	IO_L24P_5	V8	NC	NC
5	IO_L22N_5	AB7	NC	NC
5	IO_L22P_5	AA7	NC	NC
5	IO_L21N_5/VREF_5	Y7	NC	NC
5	IO_L21P_5	W7	NC	NC
5	IO_L19N_5	AB6	NC	NC
5	IO_L19P_5	AA6	NC	NC
5	IO_L06N_5	Y6		

Table 10: BG728 BGA — XC2V3000

Bank	Pin Description	Pin Number
5	IO_L52N_5	AC10
5	IO_L52P_5	AB10
5	IO_L51N_5/VREF_5	Y9
5	IO_L51P_5	Y10
5	IO_L49N_5	AG9
5	IO_L49P_5	AG8
5	IO_L30N_5	AF9
5	IO_L30P_5	AE9
5	IO_L28N_5	AD9
5	IO_L28P_5	AC9
5	IO_L27N_5/VREF_5	AB9
5	IO_L27P_5	AA9
5	IO_L25N_5	AE8
5	IO_L25P_5	AE7
5	IO_L24N_5	AD8
5	IO_L24P_5	AC8
5	IO_L22N_5	AB8
5	IO_L22P_5	AA8
5	IO_L21N_5/VREF_5	AG7
5	IO_L21P_5	AF7
5	IO_L19N_5	AC7
5	IO_L19P_5	AB7
5	IO_L06N_5	AG6
5	IO_L06P_5	AF6
5	IO_L05N_5/VRP_5	AE6
5	IO_L05P_5/VRN_5	AD6
5	IO_L04N_5	AG5
5	IO_L04P_5/VREF_5	AF5
5	IO_L03N_5/D4/ALT_VRP_5	AE5
5	IO_L03P_5/D5/ALT_VRN_5	AD5
5	IO_L02N_5/D6	AG4
5	IO_L02P_5/D7	AF4
5	IO_L01N_5/RDWR_B	AG3
5	IO_L01P_5/CS_B	AF3
6	IO_L01P_6	AE1

Table 10: BG728 BGA — XC2V3000

Bank	Pin Description	Pin Number
6	IO_L52N_6	V3
6	IO_L54P_6	V2
6	IO_L54N_6	V1
6	IO_L67P_6	U8
6	IO_L67N_6	T8
6	IO_L69P_6	U6
6	IO_L69N_6/VREF_6	U7
6	IO_L70P_6	U4
6	IO_L70N_6	U3
6	IO_L72P_6	U2
6	IO_L72N_6	U1
6	IO_L73P_6	T9
6	IO_L73N_6	R9
6	IO_L75P_6	T5
6	IO_L75N_6/VREF_6	T6
6	IO_L76P_6	T4
6	IO_L76N_6	R4
6	IO_L78P_6	T2
6	IO_L78N_6	T1
6	IO_L91P_6	R7
6	IO_L91N_6	R8
6	IO_L93P_6	R5
6	IO_L93N_6/VREF_6	R6
6	IO_L94P_6	R3
6	IO_L94N_6	P3
6	IO_L96P_6	R2
6	IO_L96N_6	R1
7	IO_L96P_7	P5
7	IO_L96N_7	P6
7	IO_L94P_7	P7
7	IO_L94N_7	P8
7	IO_L93P_7/VREF_7	N1
7	IO_L93N_7	N2
7	IO_L91P_7	N3
7	IO_L91N_7	N4

Table 11: FF896 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
7	IO_L04N_7	D29		
7	IO_L03P_7/VREF_7	E28		
7	IO_L03N_7	D28		
7	IO_L02P_7/VRN_7	H23		
7	IO_L02N_7/VRP_7	G23		
7	IO_L01P_7	B30		
7	IO_L01N_7	C30		
0	VCCO_0	K20		
0	VCCO_0	K19		
0	VCCO_0	K18		
0	VCCO_0	K17		
0	VCCO_0	K16		
0	VCCO_0	J21		
0	VCCO_0	J20		
0	VCCO_0	J19		
0	VCCO_0	J18		
0	VCCO_0	C18		
0	VCCO_0	B26		
1	VCCO_1	K15		
1	VCCO_1	K14		
1	VCCO_1	K13		
1	VCCO_1	K12		
1	VCCO_1	K11		
1	VCCO_1	J13		
1	VCCO_1	J12		
1	VCCO_1	J11		
1	VCCO_1	J10		
1	VCCO_1	C13		
1	VCCO_1	B5		
2	VCCO_2	R10		
2	VCCO_2	P10		
2	VCCO_2	N10		
2	VCCO_2	N9		
2	VCCO_2	N3		
2	VCCO_2	M10		
2	VCCO_2	M9		

Table 12: FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
1	IO_L22P_1	A5	
1	IO_L21N_1/VREF_1	F10	
1	IO_L21P_1	G9	
1	IO_L20N_1	J12	
1	IO_L20P_1	J11	
1	IO_L19N_1	B4	
1	IO_L19P_1	B5	
1	IO_L06N_1	D6	
1	IO_L06P_1	C6	
1	IO_L05N_1	H11	
1	IO_L05P_1	J10	
1	IO_L04N_1	D8	
1	IO_L04P_1/VREF_1	E7	
1	IO_L03N_1/VRP_1	F9	
1	IO_L03P_1/VRN_1	F8	
1	IO_L02N_1	H10	
1	IO_L02P_1	H9	
1	IO_L01N_1	C2	
1	IO_L01P_1	B3	
2	IO_L01N_2	E2	
2	IO_L01P_2	D2	
2	IO_L02N_2/VRP_2	K11	
2	IO_L02P_2/VRN_2	K10	
2	IO_L03N_2	F5	
2	IO_L03P_2/VREF_2	G5	
2	IO_L04N_2	E3	
2	IO_L04P_2	D3	
2	IO_L05N_2	J9	
2	IO_L05P_2	K9	
2	IO_L06N_2	F4	
2	IO_L06P_2	E4	
2	IO_L19N_2	E1	
2	IO_L19P_2	D1	
2	IO_L20N_2	J8	
2	IO_L20P_2	K8	

Table 12: FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
5	IO_L02P_5/D7	AG25	
5	IO_L01N_5/RDWR_B	AL30	
5	IO_L01P_5/CS_B	AM31	
6	IO_L01P_6	AE24	
6	IO_L01N_6	AD25	
6	IO_L02P_6/VRN_6	AJ30	
6	IO_L02N_6/VRP_6	AH30	
6	IO_L03P_6	AL32	
6	IO_L03N_6/VREF_6	AK32	
6	IO_L04P_6	AF25	
6	IO_L04N_6	AE25	
6	IO_L05P_6	AJ31	
6	IO_L05N_6	AK31	
6	IO_L06P_6	AH29	
6	IO_L06N_6	AG29	
6	IO_L19P_6	AG26	
6	IO_L19N_6	AF26	
6	IO_L20P_6	AL33	
6	IO_L20N_6	AK33	
6	IO_L21P_6	AJ32	
6	IO_L21N_6/VREF_6	AH32	
6	IO_L22P_6	AG28	
6	IO_L22N_6	AF28	
6	IO_L23P_6	AG30	
6	IO_L23N_6	AF30	
6	IO_L24P_6	AF29	
6	IO_L24N_6	AE29	
6	IO_L25P_6	AF27	
6	IO_L25N_6	AE27	
6	IO_L26P_6	AL34	
6	IO_L26N_6	AK34	
6	IO_L27P_6	AE28	
6	IO_L27N_6/VREF_6	AD28	
6	IO_L28P_6	AE26	
6	IO_L28N_6	AD26	

Table 12: FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
NA	VCCINT	AB17	
NA	VCCINT	AB16	
NA	VCCINT	AB15	
NA	VCCINT	AB14	
NA	VCCINT	AB13	
NA	VCCINT	AA22	
NA	VCCINT	AA13	
NA	VCCINT	Y22	
NA	VCCINT	Y13	
NA	VCCINT	W22	
NA	VCCINT	W13	
NA	VCCINT	V22	
NA	VCCINT	V13	
NA	VCCINT	U22	
NA	VCCINT	U13	
NA	VCCINT	T22	
NA	VCCINT	T13	
NA	VCCINT	R22	
NA	VCCINT	R13	
NA	VCCINT	P22	
NA	VCCINT	P13	
NA	VCCINT	N22	
NA	VCCINT	N21	
NA	VCCINT	N20	
NA	VCCINT	N19	
NA	VCCINT	N18	
NA	VCCINT	N17	
NA	VCCINT	N16	
NA	VCCINT	N15	
NA	VCCINT	N14	
NA	VCCINT	N13	
NA	VCCINT	M23	
NA	VCCINT	M12	
NA	VCCINT	L24	
NA	VCCINT	L11	

Table 12: FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
NA	GND	P20	
NA	GND	P19	
NA	GND	P18	
NA	GND	P17	
NA	GND	P16	
NA	GND	P15	
NA	GND	P14	
NA	GND	P7	
NA	GND	M30	
NA	GND	M5	
NA	GND	K32	
NA	GND	K3	
NA	GND	J19	
NA	GND	J16	
NA	GND	H34	
NA	GND	H27	
NA	GND	H8	
NA	GND	H1	
NA	GND	G28	
NA	GND	G21	
NA	GND	G14	
NA	GND	G7	
NA	GND	F29	
NA	GND	F6	
NA	GND	E30	
NA	GND	E23	
NA	GND	E12	
NA	GND	E5	
NA	GND	D31	
NA	GND	D4	
NA	GND	C34	
NA	GND	C32	
NA	GND	C25	
NA	GND	C10	
NA	GND	C3	
NA	GND	C1	

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
2	IO_L09P_2/VREF_2	H7	NC	
2	IO_L10N_2	G3	NC	
2	IO_L10P_2	F3	NC	
2	IO_L11N_2	J8	NC	
2	IO_L11P_2	K8	NC	
2	IO_L12N_2	H5	NC	
2	IO_L12P_2	G5	NC	
2	IO_L19N_2	G1		
2	IO_L19P_2	F1		
2	IO_L20N_2	K9		
2	IO_L20P_2	L10		
2	IO_L21N_2	K7		
2	IO_L21P_2/VREF_2	J7		
2	IO_L22N_2	H2		
2	IO_L22P_2	G2		
2	IO_L23N_2	L9		
2	IO_L23P_2	M9		
2	IO_L24N_2	H4		
2	IO_L24P_2	G4		
2	IO_L25N_2	J3		
2	IO_L25P_2	H3		
2	IO_L26N_2	M10		
2	IO_L26P_2	N10		
2	IO_L27N_2	K6		
2	IO_L27P_2/VREF_2	J6		
2	IO_L28N_2	K5		
2	IO_L28P_2	J5		
2	IO_L29N_2	N11		
2	IO_L29P_2	P11		
2	IO_L30N_2	M7		
2	IO_L30P_2	L7		
2	IO_L31N_2	J1	NC	
2	IO_L31P_2	H1	NC	
2	IO_L32N_2	L8	NC	
2	IO_L32P_2	M8	NC	
2	IO_L33N_2	K4	NC	

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
5	IO_L55N_5	AV28		
5	IO_L55P_5	AV27		
5	IO_L54N_5	AP27		
5	IO_L54P_5	AP26		
5	IO_L53N_5	AN25		
5	IO_L53P_5	AN26		
5	IO_L52N_5	AU29		
5	IO_L52P_5	AU28		
5	IO_L51N_5/VREF_5	AR28		
5	IO_L51P_5	AR27		
5	IO_L50N_5	AJ24		
5	IO_L50P_5	AJ25		
5	IO_L49N_5	AW30		
5	IO_L49P_5	AW29		
5	IO_L36N_5	AT29	NC	
5	IO_L36P_5	AT28	NC	
5	IO_L35N_5	AK25	NC	
5	IO_L35P_5	AL26	NC	
5	IO_L34N_5	AV31	NC	
5	IO_L34P_5	AV30	NC	
5	IO_L33N_5/VREF_5	AP29	NC	
5	IO_L33P_5	AP28	NC	
5	IO_L32N_5	AK26	NC	
5	IO_L32P_5	AJ26	NC	
5	IO_L31N_5	AW32	NC	
5	IO_L31P_5	AW31	NC	
5	IO_L30N_5	AM27		
5	IO_L30P_5	AM26		
5	IO_L29N_5	AN28		
5	IO_L29P_5	AN29		
5	IO_L28N_5	AU31		
5	IO_L28P_5	AU30		
5	IO_L27N_5/VREF_5	AT31		
5	IO_L27P_5	AT30		
5	IO_L26N_5	AH25		
5	IO_L26P_5	AH26		

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
7	IO_L02P_7/VRN_7	M27		
7	IO_L02N_7/VRP_7	L27		
7	IO_L01P_7	D38		
7	IO_L01N_7	E37		
0	VCCO_0	P25		
0	VCCO_0	P24		
0	VCCO_0	P23		
0	VCCO_0	P22		
0	VCCO_0	P21		
0	VCCO_0	N26		
0	VCCO_0	N25		
0	VCCO_0	N24		
0	VCCO_0	N23		
0	VCCO_0	N22		
0	VCCO_0	N21		
0	VCCO_0	L23		
0	VCCO_0	J25		
0	VCCO_0	G27		
0	VCCO_0	E29		
0	VCCO_0	C22		
0	VCCO_0	B26		
1	VCCO_1	P19		
1	VCCO_1	P18		
1	VCCO_1	P17		
1	VCCO_1	P16		
1	VCCO_1	P15		
1	VCCO_1	N19		
1	VCCO_1	N18		
1	VCCO_1	N17		
1	VCCO_1	N16		
1	VCCO_1	N15		
1	VCCO_1	N14		
1	VCCO_1	L17		
1	VCCO_1	J15		
1	VCCO_1	G13		

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	GND	Y17		
NA	GND	Y16		
NA	GND	Y10		
NA	GND	Y7		
NA	GND	Y4		
NA	GND	Y1		
NA	GND	W24		
NA	GND	W23		
NA	GND	W22		
NA	GND	W21		
NA	GND	W20		
NA	GND	W19		
NA	GND	W18		
NA	GND	W17		
NA	GND	W16		
NA	GND	V24		
NA	GND	V23		
NA	GND	V22		
NA	GND	V21		
NA	GND	V20		
NA	GND	V19		
NA	GND	V18		
NA	GND	V17		
NA	GND	V16		
NA	GND	U36		
NA	GND	U32		
NA	GND	U24		
NA	GND	U23		
NA	GND	U22		
NA	GND	U21		
NA	GND	U20		
NA	GND	U19		
NA	GND	U18		
NA	GND	U17		
NA	GND	U16		
NA	GND	U8		

Table 14: BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000

Bank	Pin Description	Pin Number	No Connect in XC2V2000
1	IO_L21P_1	A4	
1	IO_L20N_1	G10	
1	IO_L20P_1	G9	
1	IO_L19N_1	B6	
1	IO_L19P_1	C5	
1	IO_L06N_1	C6	
1	IO_L06P_1	D6	
1	IO_L05N_1	H9	
1	IO_L05P_1	G8	
1	IO_L04N_1	D7	
1	IO_L04P_1/VREF_1	E6	
1	IO_L03N_1/VRP_1	E8	
1	IO_L03P_1/VRN_1	E7	
1	IO_L02N_1	F8	
1	IO_L02P_1	F7	
1	IO_L01N_1	B5	
1	IO_L01P_1	B3	
2	IO_L01N_2	F5	
2	IO_L01P_2	G4	
2	IO_L02N_2/VRP_2	G6	
2	IO_L02P_2/VRN_2	H6	
2	IO_L03N_2	D3	
2	IO_L03P_2/VREF_2	E4	
2	IO_L04N_2	K10	
2	IO_L04P_2	K9	
2	IO_L05N_2	D2	
2	IO_L05P_2	E3	
2	IO_L06N_2	F4	
2	IO_L06P_2	F3	
2	IO_L19N_2	L10	
2	IO_L19P_2	M10	
2	IO_L20N_2	H7	
2	IO_L20P_2	J8	
2	IO_L21N_2	D1	
2	IO_L21P_2/VREF_2	E1	
2	IO_L22N_2	G5	
2	IO_L22P_2	H5	