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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 64 |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 73728 |
| Number of I/O | 88 |
| Number of Gates | 40000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 256-BGA |
| Supplier Device Package | 256-FBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc2v40-4fgg256c |

### Shift Registers

Each function generator can also be configured as a 16-bit shift register. The write operation is synchronous with a clock input (CLK) and an optional clock enable, as shown in Figure 21. A dynamic read access is performed through the 4-bit address bus, A[3:0]. The configurable 16-bit shift register cannot be set or reset. The read is asynchronous, however the storage element or flip-flop is available to implement a synchronous read. The storage element should always be used with a constant address. For example, when building an 8-bit shift register and configuring the addresses to point to the 7th bit, the 8th bit can be the flip-flop. The overall system performance is improved by using the superior clock-to-out of the flip-flops.

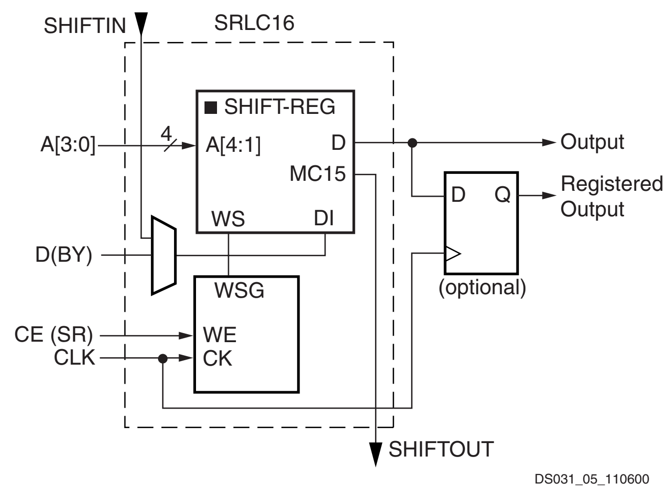


*Figure 21:* **Shift Register Configurations**

An additional dedicated connection between shift registers allows connecting the last bit of one shift register to the first bit of the next, without using the ordinary LUT output. (See Figure 22.) Longer shift registers can be built with dynamic access to any bit in the chain. The shift register chaining and the MUXF5, MUXF6, and MUXF7 multiplexers allow up to a 128-bit shift register with addressable access to be implemented in one CLB.

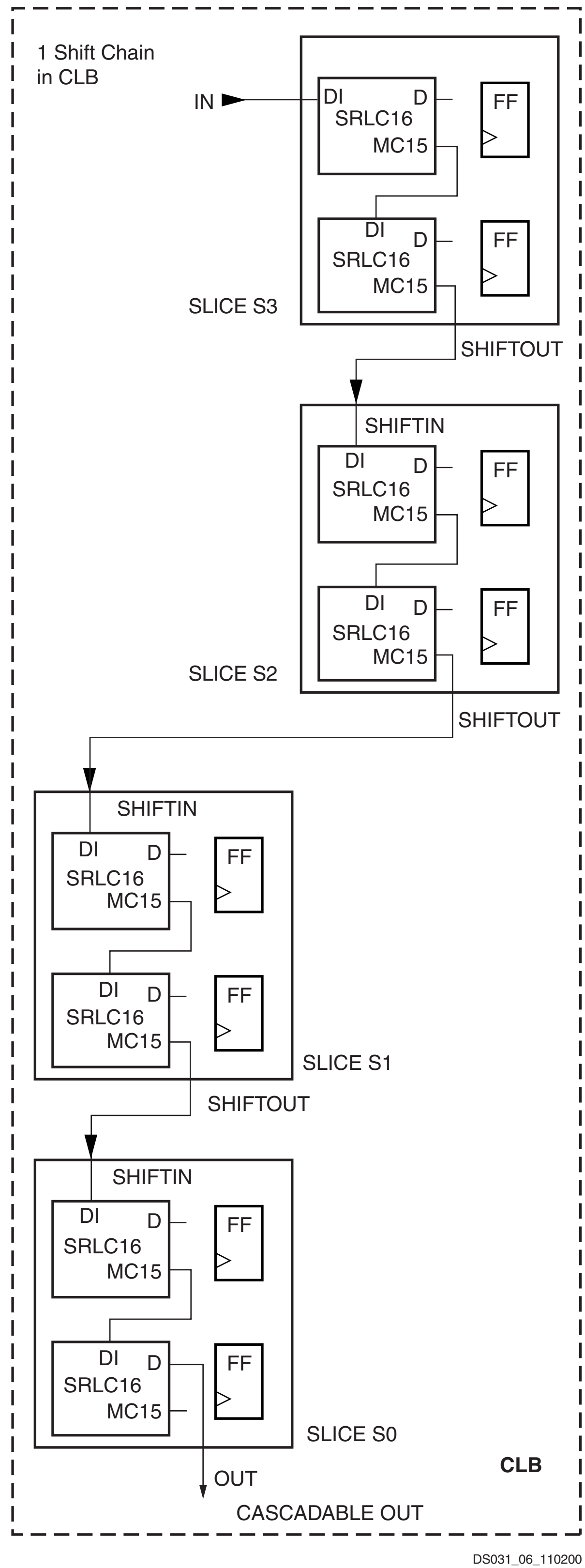


*Figure 22:* **Cascadable Shift Register**

*Table 5:* **Minimum Power On Current Required for Virtex-II Devices**

| | Device (mA) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | XC2V40, XC2V80, XC2V250, XC2V500 | XC2V1000 | XC2V1500 | XC2V2000 | XC2V3000 | XC2V4000 | XC2V6000 | XC2V8000 |
| $I_{CCINTMIN}$ | 200 | 250 | 350 | 400 | 500 | 650 | 800 | 1100 |
| $I_{CCAUXMIN}$ | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 |
| $I_{CCOMIN}$ | 50 | 50 | 100 | 100 | 100 | 100 | 100 | 100 |

**Notes:**
1. Values specified for power on current parameters are Commercial Grade. For Industrial Grade values, multiply Commercial Grade values by 1.25.
2. $I_{CCOMIN}$ values listed here apply to the entire device (all banks).

## General Power Supply Requirements

Proper decoupling of all FPGA power supplies is sessential. Consult Xilinx Application Note **XAPP623** for detailed information on power distribution system design.

$V_{CCAUX}$ powers critical resources in the FPGA. Thus, $V_{CCAUX}$ is especially susceptible to power supply noise.

Changes in $V_{CCAUX}$ voltage outside of 200 mV peak to peak should take place at a rate no faster than 10 mV per millisecond. Techniques to help reduce jitter and period distortion are provided in Xilinx Answer Record 13756, available at **www.support.xilinx.com**.

$V_{CCAUX}$ can share a power plane with 3.3V $V_{CCO}$, but only if $V_{CCO}$ does not have excessive noise. Using simultaneously switching output (SSO) limits are essential for keeping power supply noise to a minimum. Refer to **XAPP689**, "Managing Ground Bounce in Large FPGAs," to determine the number of simultaneously switching outputs allowed per bank at the package level.

## DC Input and Output Levels

Values for $V_{IL}$ and $V_{IH}$ are recommended input voltages. Values for $I_{OL}$ and $I_{OH}$ are guaranteed over the recommended operating conditions at the $V_{OL}$ and $V_{OH}$ test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum $V_{CCO}$ with the respective $V_{OL}$ and $V_{OH}$ voltage levels shown. Other standards are sample tested.

*Table 6:* **DC Input and Output Levels**

| Input/Output Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|
| | V, Min | V, Max | V, Min | V, Max | V, Max | V, Min | mA | mA |
| LVTTL[(1)] | – 0.5 | 0.8 | 2.0 | 3.6 | 0.4 | 2.4 | 24 | – 24 |
| LVCMOS33 | – 0.5 | 0.8 | 2.0 | 3.6 | 0.4 | $V_{CCO}$ – 0.4 | 24 | – 24 |
| LVCMOS25 | – 0.5 | 0.7 | 1.7 | 2.7 | 0.4 | $V_{CCO}$ – 0.4 | 24 | – 24 |
| LVCMOS18 | – 0.5 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | 1.95 | 0.4 | $V_{CCO}$ – 0.4 | 16 | – 16 |
| LVCMOS15 | – 0.5 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | 1.7 | 0.4 | $V_{CCO}$ – 0.4 | 16 | – 16 |
| PCI33_3 | – 0.5 | 30% $V_{CCO}$ | 50% $V_{CCO}$ | $V_{CCO}$ + 0.5 | 10% $V_{CCO}$ | 90% $V_{CCO}$ | Note 2 | Note 2 |
| PCI66_3 | – 0.5 | 30% $V_{CCO}$ | 50% $V_{CCO}$ | $V_{CCO}$ + 0.5 | 10% $V_{CCO}$ | 90% $V_{CCO}$ | Note 2 | Note 2 |
| PCI–X | – 0.5 | Note 2 | Note 2 | Note 2 | Note 2 | Note 2 | Note 2 | Note 2 |
| GTLP | – 0.5 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | $V_{CCO}$ + 0.5 | 0.6 | n/a | 36 | n/a |
| GTL | – 0.5 | $V_{REF}$ – 0.05 | $V_{REF}$ + 0.05 | $V_{CCO}$ + 0.5 | 0.4 | n/a | 40 | n/a |
| HSTL I | – 0.5 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | $V_{CCO}$ + 0.5 | 0.4 | $V_{CCO}$ – 0.4 | 8 | – 8 |
| HSTL II | – 0.5 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | $V_{CCO}$ + 0.5 | 0.4 | $V_{CCO}$ – 0.4 | 16 | – 16 |
| HSTL III | – 0.5 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | $V_{CCO}$ + 0.5 | 0.4 | $V_{CCO}$ – 0.4 | 24 | – 8 |
| HSTL IV | – 0.5 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | $V_{CCO}$ + 0.5 | 0.4 | $V_{CCO}$ – 0.4 | 48 | – 8 |

## Virtex-II Switching Characteristics

Switching characteristics in this document are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Note that Virtex-II Performance Characteristics, page 7 are subject to these guidelines as well. Each designation is defined as follows:

**Advance**: These speed files are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

**Preliminary**: These speed files are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

**Production**: These speed files are released once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 13 correlates the current status of each Virtex-II device with a corresponding speed grade designation.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

### Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the Xilinx static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-II devices.

### IOB Input Switching Characteristics

Input delays associated with the pad are specified for LVTTL levels. For other standards, adjust the delays with the values shown in IOB Input Switching Characteristics Standard Adjustments, page 11.

*Table 13:* **Virtex-II Device Speed Grade Designations**

| Device | Speed Grade Designations | | |
|---|---|---|---|
| | Advance | Preliminary | Production |
| XC2V40 | | | -6, -5, -4 |
| XC2V80 | | | -6, -5, -4 |
| XC2V250 | | | -6, -5, -4 |
| XC2V500 | | | -6, -5, -4 |
| XC2V1000 | | | -6, -5, -4 |
| XC2V1500 | | | -6, -5, -4 |
| XC2V2000 | | | -6, -5, -4 |
| XC2V3000 | | | -6, -5, -4 |
| XC2V4000 | | | -6, -5, -4 |
| XC2V6000 | | | -6, -5, -4 |
| XC2V8000 | | | -5, -4 |

*Table 14:* **IOB Input Switching Characteristics**

| Description | Symbol | Device | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -6 | -5 | -4 | |
| **Propagation Delays** | | | | | | |
| Pad to I output, no delay | $T_{IOPI}$ | All | 0.69 | 0.76 | 0.88 | ns, Max |
| Pad to I output, with delay | $T_{IOPID}$ | XC2V40 | 1.92 | 2.11 | 2.43 | ns, Max |
| | | XC2V80 | 1.92 | 2.11 | 2.43 | ns, Max |
| | | XC2V250 | 1.92 | 2.11 | 2.43 | ns, Max |
| | | XC2V500 | 1.92 | 2.11 | 2.43 | ns, Max |
| | | XC2V1000 | 1.92 | 2.11 | 2.43 | ns, Max |
| | | XC2V1500 | 1.92 | 2.11 | 2.43 | ns, Max |
| | | XC2V2000 | 1.92 | 2.11 | 2.43 | ns, Max |
| | | XC2V3000 | 1.97 | 2.16 | 2.49 | ns, Max |
| | | XC2V4000 | 1.97 | 2.16 | 2.49 | ns, Max |
| | | XC2V6000 | 2.10 | 2.31 | 2.66 | ns, Max |
| | | XC2V8000 | | 2.31 | 2.66 | ns, Max |

## I/O Standard Adjustment Measurement Methodology

### Input Delay Measurements

Table 18 shows the test setup parameters used for measuring Input standard adjustments (see Table 15, page 11).

*Table 18:* **Input Delay Measurement Methodology**

| Description | IOSTANDARD Attribute | $V_L$ (1,2) | $V_H$ (1,2) | $V_{MEAS}$ (1,4,5) | $V_{REF}$ (1,3,5) |
|---|---|---|---|---|---|
| LVTTL (Low-Voltage Transistor-Transistor Logic) | LVTTL | 0 | 3.0 | 1.4 | – |
| LVCMOS (Low-Voltage CMOS), 3.3V | LVCMOS33 | 0 | 3.3 | 1.65 | – |
| LVCMOS, 2.5V | LVCMOS25 | 0 | 2.5 | 1.25 | – |
| LVCMOS, 1.8V | LVCMOS18 | 0 | 1.8 | 0.9 | – |
| LVCMOS, 1.5V | LVCMOS15 | 0 | 1.5 | 0.75 | – |
| PCI (Peripheral Component Interface), 33 MHz, 3.3V | PCI33_3 | Per PCI Specification | | | – |
| PCI, 66 MHz, 3.3V | PCI66_3 | Per PCI Specification | | | – |
| PCI-X, 133 MHz, 3.3V | PCIX | Per PCI-X Specification | | | – |
| GTL (Gunning Transceiver Logic) | GTL | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | $V_{REF}$ | 0.80 |
| GTL Plus | GTLP | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | $V_{REF}$ | 1.0 |
| HSTL (High-Speed Transceiver Logic), Class I & II | HSTL_I, HSTL_II | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | $V_{REF}$ | 0.75 |
| HSTL, Class III & IV | HSTL_III, HSTL_IV | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | $V_{REF}$ | 0.90 |
| HSTL, Class I & II, 1.8V | HSTL_I_18, HSTL_II_18 | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | $V_{REF}$ | 0.90 |
| HSTL, Class III & IV, 1.8V | HSTL_III_18, HSTL_IV_18 | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | $V_{REF}$ | 1.08 |
| SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V | SSTL3_I, SSTL3_II | $V_{REF}$ – 1.00 | $V_{REF}$ + 1.00 | $V_{REF}$ | 1.5 |
| SSTL, Class I & II, 2.5V | SSTL2_I, SSTL2_II | $V_{REF}$ – 0.75 | $V_{REF}$ + 0.75 | $V_{REF}$ | 1.25 |
| SSTL, Class I & II, 1.8V | SSTL18_I, SSTL18_II | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | $V_{REF}$ | 0.90 |
| AGP-2X/AGP (Accelerated Graphics Port) | AGP | $V_{REF}$ – (0.2 x $V_{CCO}$) | $V_{REF}$ + (0.2 x $V_{CCO}$) | $V_{REF}$ | AGP Spec |
| LVDS (Low-Voltage Differential Signaling), 2.5V | LVDS_25 | 1.2 – 0.125 | 1.2 + 0.125 | 1.2 | |
| LVDS, 3.3V | LVDS_33 | 1.2 – 0.125 | 1.2 + 0.125 | 1.2 | |
| LVDSEXT (LVDS Extended Mode), 2.5V | LVDSEXT_25 | 1.2 – 0.125 | 1.2 + 0.125 | 1.2 | |
| LVDSEXT, 3.3V | LVDSEXT_33 | 1.2 – 0.125 | 1.2 + 0.125 | 1.2 | |
| ULVDS (Ultra LVDS), 2.5V | ULVDS_25 | 0.6 – 0.125 | 0.6 + 0.125 | 0.6 | |
| LDT (HyperTransport), 2.5V | LDT_25 | 0.6 – 0.125 | 0.6 + 0.125 | 0.6 | |
| LVPECL (Low-Voltage Positive Electron-Coupled Logic), 3.3V | LVPECL_33 | 1.6 – 0.3 | 1.6 + 0.3 | 1.6 | |

**Notes:**
1. Input delay measurement methodology parameters for LVDCI and HSLVDCI are the same as for LVCMOS standards of the same voltage. Parameters for all other DCI standards are the same as for the corresponding non-DCI standards.
2. Input waveform switches between $V_L$ and $V_H$.
3. Measurements are made at typical, minimum, and maximum $V_{REF}$ values. Reported delays reflect worst case of these measurements. $V_{REF}$ values listed are typical. See **Virtex-II Platform FPGA User Guide** for min/max specifications.
4. Input voltage level from which measurement starts.
5. Note that this is an input voltage reference that bears no relation to the $V_{REF}$ / $V_{MEAS}$ parameters found in IBIS models and/or noted in Figure 1.

*Table 27:* **Enhanced Pipelined Multiplier Switching Characteristics**

| Description | Symbol | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -6 | -5 | -4 | |
| **Setup and Hold Times Before/After Clock** | | | | | |
| Data Inputs | $T_{MULIDCK}/T_{MULCKID}$ | 3.00/0.00 | 3.45/0.00 | 3.89/0.00 | ns, Max |
| Clock Enable | $T_{MULIDCK\_CE}/T_{MULCKID\_CE}$ | 0.72/0.00 | 0.80/0.00 | 0.86/0.00 | ns, Max |
| Reset | $T_{MULIDCK\_RST}/T_{MULCKID\_RST}$ | 0.72/0.00 | 0.80/0.00 | 0.86/0.00 | ns, Max |
| **Clock to Output Pin** | | | | | |
| Clock to Pin 35 | $T_{MULTCK1\_P35}$ | 3.05 | 3.25 | 3.74 | ns, Max |
| Clock to Pin 34 | $T_{MULTCK1\_P34}$ | 2.95 | 3.14 | 3.61 | ns, Max |
| Clock to Pin 33 | $T_{MULTCK1\_P33}$ | 2.85 | 3.04 | 3.49 | ns, Max |
| Clock to Pin 32 | $T_{MULTCK1\_P32}$ | 2.76 | 2.93 | 3.37 | ns, Max |
| Clock to Pin 31 | $T_{MULTCK1\_P31}$ | 2.66 | 2.82 | 3.25 | ns, Max |
| Clock to Pin 30 | $T_{MULTCK1\_P30}$ | 2.56 | 2.72 | 3.12 | ns, Max |
| Clock to Pin 29 | $T_{MULTCK1\_P29}$ | 2.47 | 2.61 | 3.00 | ns, Max |
| Clock to Pin 28 | $T_{MULTCK1\_P28}$ | 2.37 | 2.50 | 2.88 | ns, Max |
| Clock to Pin 27 | $T_{MULTCK1\_P27}$ | 2.27 | 2.40 | 2.75 | ns, Max |
| Clock to Pin 26 | $T_{MULTCK1\_P26}$ | 2.17 | 2.29 | 2.63 | ns, Max |
| Clock to Pin 25 | $T_{MULTCK1\_P25}$ | 2.08 | 2.18 | 2.51 | ns, Max |
| Clock to Pin 24 | $T_{MULTCK1\_P24}$ | 1.98 | 2.07 | 2.38 | ns, Max |
| Clock to Pin 23 | $T_{MULTCK1\_P23}$ | 1.88 | 1.97 | 2.26 | ns, Max |
| Clock to Pin 22 | $T_{MULTCK1\_P22}$ | 1.79 | 1.86 | 2.14 | ns, Max |
| Clock to Pin 21 | $T_{MULTCK1\_P21}$ | 1.69 | 1.75 | 2.02 | ns, Max |
| Clock to Pin 20 | $T_{MULTCK1\_P20}$ | 1.59 | 1.65 | 1.89 | ns, Max |
| Clock to Pin 19 | $T_{MULTCK1\_P19}$ | 1.50 | 1.54 | 1.77 | ns, Max |
| Clock to Pin 18 | $T_{MULTCK1\_P18}$ | 1.40 | 1.43 | 1.65 | ns, Max |
| Clock to Pin 17 | $T_{MULTCK1\_P17}$ | 1.30 | 1.33 | 1.52 | ns, Max |
| Clock to Pin 16 | $T_{MULTCK1\_P16}$ | 1.20 | 1.22 | 1.40 | ns, Max |
| Clock to Pin 15 | $T_{MULTCK1\_P15}$ | 1.11 | 1.11 | 1.28 | ns, Max |
| Clock to Pin 14 | $T_{MULTCK1\_P14}$ | 1.01 | 1.00 | 1.15 | ns, Max |
| Clock to Pin 13 | $T_{MULTCK1\_P13}$ | 0.91 | 1.00 | 1.15 | ns, Max |
| Clock to Pin 12 | $T_{MULTCK1\_P12}$ | 0.91 | 1.00 | 1.15 | ns, Max |
| Clock to Pin 11 | $T_{MULTCK1\_P11}$ | 0.91 | 1.00 | 1.15 | ns, Max |
| Clock to Pin 10 | $T_{MULTCK1\_P10}$ | 0.91 | 1.00 | 1.15 | ns, Max |
| Clock to Pin 9 | $T_{MULTCK1\_P9}$ | 0.91 | 1.00 | 1.15 | ns, Max |
| Clock to Pin 8 | $T_{MULTCK1\_P8}$ | 0.91 | 1.00 | 1.15 | ns, Max |
| Clock to Pin 7 | $T_{MULTCK1\_P7}$ | 0.91 | 1.00 | 1.15 | ns, Max |
| Clock to Pin 6 | $T_{MULTCK1\_P6}$ | 0.91 | 1.00 | 1.15 | ns, Max |
| Clock to Pin 5 | $T_{MULTCK1\_P5}$ | 0.91 | 1.00 | 1.15 | ns, Max |
| Clock to Pin 4 | $T_{MULTCK1\_P4}$ | 0.91 | 1.00 | 1.15 | ns, Max |
| Clock to Pin 3 | $T_{MULTCK1\_P3}$ | 0.91 | 1.00 | 1.15 | ns, Max |
| Clock to Pin 2 | $T_{MULTCK1\_P2}$ | 0.91 | 1.00 | 1.15 | ns, Max |
| Clock to Pin 1 | $T_{MULTCK1\_P1}$ | 0.91 | 1.00 | 1.15 | ns, Max |
| Clock to Pin 0 | $T_{MULTCK1\_P0}$ | 0.91 | 1.00 | 1.15 | ns, Max |

*Table 7:* **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

| Bank | Pin Description | Pin Number | No Connect in XC2V250 | No Connect in XC2V500 |
|---|---|---|---|---|
| 2 | IO_L45N_2 | H19 | | |
| 2 | IO_L45P_2/VREF_2 | H20 | | |
| 2 | IO_L46N_2 | H21 | | |
| 2 | IO_L46P_2 | H22 | | |
| 2 | IO_L48N_2 | J17 | | |
| 2 | IO_L48P_2 | J18 | | |
| 2 | IO_L49N_2 | J19 | NC | |
| 2 | IO_L49P_2 | J20 | NC | |
| 2 | IO_L51N_2 | J21 | NC | |
| 2 | IO_L51P_2/VREF_2 | J22 | NC | |
| 2 | IO_L52N_2 | K17 | NC | |
| 2 | IO_L52P_2 | K18 | NC | |
| 2 | IO_L54N_2 | K19 | NC | |
| 2 | IO_L54P_2 | K20 | NC | |
| 2 | IO_L91N_2 | K21 | | |
| 2 | IO_L91P_2 | K22 | | |
| 2 | IO_L93N_2 | L17 | | |
| 2 | IO_L93P_2/VREF_2 | L18 | | |
| 2 | IO_L94N_2 | L19 | | |
| 2 | IO_L94P_2 | L20 | | |
| 2 | IO_L96N_2 | L21 | | |
| 2 | IO_L96P_2 | L22 | | |
| | | | | |
| 3 | IO_L96N_3 | M21 | | |
| 3 | IO_L96P_3 | M20 | | |
| 3 | IO_L94N_3 | M19 | | |
| 3 | IO_L94P_3 | M18 | | |
| 3 | IO_L93N_3/VREF_3 | M17 | | |
| 3 | IO_L93P_3 | N17 | | |
| 3 | IO_L91N_3 | N22 | | |
| 3 | IO_L91P_3 | N21 | | |
| 3 | IO_L54N_3 | N20 | NC | |
| 3 | IO_L54P_3 | N19 | NC | |
| 3 | IO_L52N_3 | N18 | NC | |

*Table 7:* **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

| Bank | Pin Description | Pin Number | No Connect in XC2V250 | No Connect in XC2V500 |
|---|---|---|---|---|
| 7 | IO_L51N_7 | J2 | NC | |
| 7 | IO_L49P_7 | J3 | NC | |
| 7 | IO_L49N_7 | J4 | NC | |
| 7 | IO_L48P_7 | H1 | | |
| 7 | IO_L48N_7 | H2 | | |
| 7 | IO_L46P_7 | H3 | | |
| 7 | IO_L46N_7 | H4 | | |
| 7 | IO_L45P_7/VREF_7 | J6 | | |
| 7 | IO_L45N_7 | H5 | | |
| 7 | IO_L43P_7 | G1 | | |
| 7 | IO_L43N_7 | G2 | | |
| 7 | IO_L24P_7 | G3 | NC | NC |
| 7 | IO_L24N_7 | G4 | NC | NC |
| 7 | IO_L22P_7 | F1 | NC | NC |
| 7 | IO_L22N_7 | F2 | NC | NC |
| 7 | IO_L21P_7/VREF_7 | F3 | NC | NC |
| 7 | IO_L21N_7 | F4 | NC | NC |
| 7 | IO_L19P_7 | G5 | NC | NC |
| 7 | IO_L19N_7 | F5 | NC | NC |
| 7 | IO_L06P_7 | E1 | | |
| 7 | IO_L06N_7 | E2 | | |
| 7 | IO_L04P_7 | E3 | | |
| 7 | IO_L04N_7 | E4 | | |
| 7 | IO_L03P_7/VREF_7 | D1 | | |
| 7 | IO_L03N_7 | D2 | | |
| 7 | IO_L02P_7/VRN_7 | C1 | | |
| 7 | IO_L02N_7/VRP_7 | C2 | | |
| 7 | IO_L01P_7 | E5 | | |
| 7 | IO_L01N_7 | E6 | | |
| | | | | |
| 0 | VCCO_0 | G11 | | |
| 0 | VCCO_0 | G10 | | |
| 0 | VCCO_0 | G9 | | |
| 0 | VCCO_0 | F8 | | |

## FG676/FGG676 Fine-Pitch BGA Package

As shown in Table 8, XC2V1500, XC2V2000, and XC2V3000 Virtex-II devices are available in the FG676/FGG676 fine-pitch BGA package. Pins in the XC2V1500, XC2V2000, and XC2V3000 devices are the same, except for the pin differences in the XC2V1500 and XC2V2000 devices shown in the No Connect columns. Following this table are the FG676/FGG676 Fine-Pitch BGA Package Specifications (1.00mm pitch).

*Table 8:* **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

| Bank | Pin Description | Pin Number | No Connect in XC2V1500 | No Connect in XC2V2000 |
|---|---|---|---|---|
| 0 | IO_L01N_0 | D6 | | |
| 0 | IO_L01P_0 | C6 | | |
| 0 | IO_L02N_0 | B1 | | |
| 0 | IO_L02P_0 | A2 | | |
| 0 | IO_L03N_0/VRP_0 | D7 | | |
| 0 | IO_L03P_0/VRN_0 | C7 | | |
| 0 | IO_L04N_0/VREF_0 | B3 | | |
| 0 | IO_L04P_0 | A3 | | |
| 0 | IO_L05N_0 | G6 | | |
| 0 | IO_L05P_0 | G7 | | |
| 0 | IO_L06N_0 | E6 | | |
| 0 | IO_L06P_0 | E7 | | |
| 0 | IO_L19N_0 | B4 | | |
| 0 | IO_L19P_0 | A4 | | |
| 0 | IO_L21N_0 | B5 | | |
| 0 | IO_L21P_0/VREF_0 | A5 | | |
| 0 | IO_L22N_0 | B6 | | |
| 0 | IO_L22P_0 | A6 | | |
| 0 | IO_L24N_0 | A7 | | |
| 0 | IO_L24P_0 | A8 | | |
| 0 | IO_L25N_0 | E8 | NC | NC |
| 0 | IO_L25P_0 | D8 | NC | NC |
| 0 | IO_L27N_0 | G8 | NC | NC |
| 0 | IO_L27P_0/VREF_0 | F8 | NC | NC |
| 0 | IO_L49N_0 | C8 | | |
| 0 | IO_L49P_0 | B8 | | |
| 0 | IO_L51N_0 | D9 | | |
| 0 | IO_L51P_0/VREF_0 | E9 | | |
| 0 | IO_L52N_0 | F9 | | |
| 0 | IO_L52P_0 | G9 | | |
| 0 | IO_L54N_0 | B9 | | |
| 0 | IO_L54P_0 | A9 | | |
| 0 | IO_L67N_0 | C9 | | |

*Table 10:* **BG728 BGA — XC2V3000**

| Bank | Pin Description | Pin Number |
|---|---|---|
| 4 | IO_L27P_4/VREF_4 | AG19 |
| 4 | IO_L28N_4 | AB19 |
| 4 | IO_L28P_4 | AA19 |
| 4 | IO_L30N_4 | AC19 |
| 4 | IO_L30P_4 | AD19 |
| 4 | IO_L49N_4 | AE19 |
| 4 | IO_L49P_4 | AF19 |
| 4 | IO_L51N_4 | AA18 |
| 4 | IO_L51P_4/VREF_4 | Y18 |
| 4 | IO_L52N_4 | AB18 |
| 4 | IO_L52P_4 | AC18 |
| 4 | IO_L54N_4 | AD18 |
| 4 | IO_L54P_4 | AE18 |
| 4 | IO_L67N_4 | AF18 |
| 4 | IO_L67P_4 | AG18 |
| 4 | IO_L69N_4 | AA17 |
| 4 | IO_L69P_4/VREF_4 | Y17 |
| 4 | IO_L70N_4 | AB17 |
| 4 | IO_L70P_4 | AB16 |
| 4 | IO_L72N_4 | AD17 |
| 4 | IO_L72P_4 | AE17 |
| 4 | IO_L73N_4 | AF17 |
| 4 | IO_L73P_4 | AG17 |
| 4 | IO_L75N_4 | Y16 |
| 4 | IO_L75P_4/VREF_4 | W16 |
| 4 | IO_L76N_4 | AC16 |
| 4 | IO_L76P_4 | AD16 |
| 4 | IO_L78N_4 | AF16 |
| 4 | IO_L78P_4 | AG16 |
| 4 | IO_L91N_4/VREF_4 | W15 |
| 4 | IO_L91P_4 | Y15 |
| 4 | IO_L92N_4 | AB15 |
| 4 | IO_L92P_4 | AA15 |
| 4 | IO_L93N_4 | AC15 |
| 4 | IO_L93P_4 | AD15 |
| 4 | IO_L94N_4/VREF_4 | AE15 |

*Table 10:* **BG728 BGA — XC2V3000**

| Bank | Pin Description | Pin Number |
|---|---|---|
| 6 | IO_L52N_6 | V3 |
| 6 | IO_L54P_6 | V2 |
| 6 | IO_L54N_6 | V1 |
| 6 | IO_L67P_6 | U8 |
| 6 | IO_L67N_6 | T8 |
| 6 | IO_L69P_6 | U6 |
| 6 | IO_L69N_6/VREF_6 | U7 |
| 6 | IO_L70P_6 | U4 |
| 6 | IO_L70N_6 | U3 |
| 6 | IO_L72P_6 | U2 |
| 6 | IO_L72N_6 | U1 |
| 6 | IO_L73P_6 | T9 |
| 6 | IO_L73N_6 | R9 |
| 6 | IO_L75P_6 | T5 |
| 6 | IO_L75N_6/VREF_6 | T6 |
| 6 | IO_L76P_6 | T4 |
| 6 | IO_L76N_6 | R4 |
| 6 | IO_L78P_6 | T2 |
| 6 | IO_L78N_6 | T1 |
| 6 | IO_L91P_6 | R7 |
| 6 | IO_L91N_6 | R8 |
| 6 | IO_L93P_6 | R5 |
| 6 | IO_L93N_6/VREF_6 | R6 |
| 6 | IO_L94P_6 | R3 |
| 6 | IO_L94N_6 | P3 |
| 6 | IO_L96P_6 | R2 |
| 6 | IO_L96N_6 | R1 |
| | | |
| 7 | IO_L96P_7 | P5 |
| 7 | IO_L96N_7 | P6 |
| 7 | IO_L94P_7 | P7 |
| 7 | IO_L94N_7 | P8 |
| 7 | IO_L93P_7/VREF_7 | N1 |
| 7 | IO_L93N_7 | N2 |
| 7 | IO_L91P_7 | N3 |
| 7 | IO_L91N_7 | N4 |

*Table 10:* **BG728 BGA — XC2V3000**

| Bank | Pin Description | Pin Number |
|---|---|---|
| NA | VCCAUX | P26 |
| NA | VCCAUX | P2 |
| NA | VCCAUX | C26 |
| NA | VCCAUX | C2 |
| NA | VCCAUX | B14 |
| NA | VCCINT | V18 |
| NA | VCCINT | V14 |
| NA | VCCINT | V10 |
| NA | VCCINT | U17 |
| NA | VCCINT | U16 |
| NA | VCCINT | U15 |
| NA | VCCINT | U14 |
| NA | VCCINT | U13 |
| NA | VCCINT | U12 |
| NA | VCCINT | U11 |
| NA | VCCINT | T17 |
| NA | VCCINT | T11 |
| NA | VCCINT | R17 |
| NA | VCCINT | R11 |
| NA | VCCINT | P18 |
| NA | VCCINT | P17 |
| NA | VCCINT | P11 |
| NA | VCCINT | P10 |
| NA | VCCINT | N17 |
| NA | VCCINT | N11 |
| NA | VCCINT | M17 |
| NA | VCCINT | M11 |
| NA | VCCINT | L17 |
| NA | VCCINT | L16 |
| NA | VCCINT | L15 |
| NA | VCCINT | L14 |
| NA | VCCINT | L13 |
| NA | VCCINT | L12 |
| NA | VCCINT | L11 |
| NA | VCCINT | K18 |
| NA | VCCINT | K14 |

*Table 11:* **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

| Bank | Pin Description | Pin Number | No Connect in the XC2V1000 | No Connect in the XC2V1500 |
|---|---|---|---|---|
| 4 | IO_L73P_4 | AJ12 | NC | NC |
| 4 | IO_L74N_4 | AE13 | NC | NC |
| 4 | IO_L74P_4 | AE14 | NC | NC |
| 4 | IO_L75N_4 | AF13 | NC | NC |
| 4 | IO_L75P_4/VREF_4 | AG13 | NC | NC |
| 4 | IO_L76N_4 | AK13 | NC | NC |
| 4 | IO_L76P_4 | AK12 | NC | NC |
| 4 | IO_L77N_4 | AB14 | NC | NC |
| 4 | IO_L77P_4 | AB15 | NC | NC |
| 4 | IO_L78N_4 | AF15 | NC | NC |
| 4 | IO_L78P_4 | AF14 | NC | NC |
| 4 | IO_L91N_4/VREF_4 | AJ14 | | |
| 4 | IO_L91P_4 | AJ15 | | |
| 4 | IO_L92N_4 | AC14 | | |
| 4 | IO_L92P_4 | AC15 | | |
| 4 | IO_L93N_4 | AG15 | | |
| 4 | IO_L93P_4 | AG14 | | |
| 4 | IO_L94N_4/VREF_4 | AK14 | | |
| 4 | IO_L94P_4 | AK15 | | |
| 4 | IO_L95N_4/GCLK3S | AD15 | | |
| 4 | IO_L95P_4/GCLK2P | AE15 | | |
| 4 | IO_L96N_4/GCLK1S | AH14 | | |
| 4 | IO_L96P_4/GCLK0P | AH15 | | |
| | | | | |
| 5 | IO_L96N_5/GCLK7S | AH16 | | |
| 5 | IO_L96P_5/GCLK6P | AH17 | | |
| 5 | IO_L95N_5/GCLK5S | AE16 | | |
| 5 | IO_L95P_5/GCLK4P | AD16 | | |
| 5 | IO_L94N_5 | AJ16 | | |
| 5 | IO_L94P_5/VREF_5 | AJ17 | | |
| 5 | IO_L93N_5 | AG17 | | |
| 5 | IO_L93P_5 | AG16 | | |
| 5 | IO_L92N_5 | AC16 | | |
| 5 | IO_L92P_5 | AC17 | | |
| 5 | IO_L91N_5 | AK17 | | |
| 5 | IO_L91P_5/VREF_5 | AK18 | | |
| 5 | IO_L78N_5 | AF17 | NC | NC |

*Table 11:* **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

| Bank | Pin Description | Pin Number | No Connect in the XC2V1000 | No Connect in the XC2V1500 |
|---|---|---|---|---|
| NA | VCCINT | N20 | | |
| NA | VCCINT | N11 | | |
| NA | VCCINT | M20 | | |
| NA | VCCINT | M11 | | |
| NA | VCCINT | L20 | | |
| NA | VCCINT | L19 | | |
| NA | VCCINT | L18 | | |
| NA | VCCINT | L17 | | |
| NA | VCCINT | L16 | | |
| NA | VCCINT | L15 | | |
| NA | VCCINT | L14 | | |
| NA | VCCINT | L13 | | |
| NA | VCCINT | L12 | | |
| NA | VCCINT | L11 | | |
| NA | VCCINT | K21 | | |
| NA | VCCINT | K10 | | |
| NA | VCCINT | J22 | | |
| NA | VCCINT | J9 | | |
| NA | GND | AK23 | | |
| NA | GND | AK8 | | |
| NA | GND | AJ29 | | |
| NA | GND | AJ2 | | |
| NA | GND | AH28 | | |
| NA | GND | AH21 | | |
| NA | GND | AH10 | | |
| NA | GND | AH3 | | |
| NA | GND | AG27 | | |
| NA | GND | AG4 | | |
| NA | GND | AF26 | | |
| NA | GND | AF19 | | |
| NA | GND | AF12 | | |
| NA | GND | AF5 | | |
| NA | GND | AE25 | | |
| NA | GND | AE6 | | |
| NA | GND | AD17 | | |
| NA | GND | AD14 | | |
| NA | GND | AC30 | | |

*Table 12:* **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

| Bank | Pin Description | Pin Number | No Connect in the XC2V3000 |
|---|---|---|---|
| 0 | IO_L77N_0 | J20 | |
| 0 | IO_L77P_0 | K19 | |
| 0 | IO_L78N_0 | D20 | |
| 0 | IO_L78P_0 | D21 | |
| 0 | IO_L79N_0 | A21 | NC |
| 0 | IO_L79P_0 | A22 | NC |
| 0 | IO_L80N_0 | L19 | NC |
| 0 | IO_L80P_0 | L18 | NC |
| 0 | IO_L81N_0 | B19 | NC |
| 0 | IO_L81P_0/VREF_0 | A20 | NC |
| 0 | IO_L82N_0 | A18 | NC |
| 0 | IO_L82P_0 | B18 | NC |
| 0 | IO_L83N_0 | H19 | NC |
| 0 | IO_L83P_0 | H18 | NC |
| 0 | IO_L84N_0 | C20 | NC |
| 0 | IO_L84P_0 | C21 | NC |
| 0 | IO_L91N_0/VREF_0 | D19 | |
| 0 | IO_L91P_0 | D18 | |
| 0 | IO_L92N_0 | G18 | |
| 0 | IO_L92P_0 | G19 | |
| 0 | IO_L93N_0 | F18 | |
| 0 | IO_L93P_0 | F19 | |
| 0 | IO_L94N_0/VREF_0 | C19 | |
| 0 | IO_L94P_0 | C18 | |
| 0 | IO_L95N_0/GCLK7P | K18 | |
| 0 | IO_L95P_0/GCLK6S | J18 | |
| 0 | IO_L96N_0/GCLK5P | E19 | |
| 0 | IO_L96P_0/GCLK4S | E18 | |
| | | | |
| 1 | IO_L96N_1/GCLK3P | E17 | |
| 1 | IO_L96P_1/GCLK2S | E16 | |
| 1 | IO_L95N_1/GCLK1P | H17 | |
| 1 | IO_L95P_1/GCLK0S | H16 | |
| 1 | IO_L94N_1 | D17 | |
| 1 | IO_L94P_1/VREF_1 | D16 | |
| 1 | IO_L93N_1 | F16 | |

*Table 12:* **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

| Bank | Pin Description | Pin Number | No Connect in the XC2V3000 |
|---|---|---|---|
| 1 | IO_L93P_1 | F17 | |
| 1 | IO_L92N_1 | G16 | |
| 1 | IO_L92P_1 | G17 | |
| 1 | IO_L91N_1 | C16 | |
| 1 | IO_L91P_1/VREF_1 | C15 | |
| 1 | IO_L84N_1 | D14 | NC |
| 1 | IO_L84P_1 | D15 | NC |
| 1 | IO_L83N_1 | J17 | NC |
| 1 | IO_L83P_1 | K17 | NC |
| 1 | IO_L82N_1 | B17 | NC |
| 1 | IO_L82P_1 | A17 | NC |
| 1 | IO_L81N_1/VREF_1 | A15 | NC |
| 1 | IO_L81P_1 | B16 | NC |
| 1 | IO_L80N_1 | L17 | NC |
| 1 | IO_L80P_1 | L16 | NC |
| 1 | IO_L79N_1 | A13 | NC |
| 1 | IO_L79P_1 | A14 | NC |
| 1 | IO_L78N_1 | C13 | |
| 1 | IO_L78P_1 | C14 | |
| 1 | IO_L77N_1 | K16 | |
| 1 | IO_L77P_1 | K15 | |
| 1 | IO_L76N_1 | B13 | |
| 1 | IO_L76P_1 | B14 | |
| 1 | IO_L75N_1/VREF_1 | F15 | |
| 1 | IO_L75P_1 | G15 | |
| 1 | IO_L74N_1 | H15 | |
| 1 | IO_L74P_1 | H14 | |
| 1 | IO_L73N_1 | A11 | |
| 1 | IO_L73P_1 | A12 | |
| 1 | IO_L72N_1 | E13 | |
| 1 | IO_L72P_1 | E14 | |
| 1 | IO_L71N_1 | J15 | |
| 1 | IO_L71P_1 | J14 | |
| 1 | IO_L70N_1 | D12 | |
| 1 | IO_L70P_1 | D13 | |
| 1 | IO_L69N_1/VREF_1 | F14 | |

*Table 12:* **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

| Bank | Pin Description | Pin Number | No Connect in the XC2V3000 |
|---|---|---|---|
| 4 | IO_L20N_4 | AJ10 | |
| 4 | IO_L20P_4 | AJ9 | |
| 4 | IO_L21N_4 | AH9 | |
| 4 | IO_L21P_4/VREF_4 | AH10 | |
| 4 | IO_L22N_4 | AN5 | |
| 4 | IO_L22P_4 | AN4 | |
| 4 | IO_L23N_4 | AE12 | |
| 4 | IO_L23P_4 | AE13 | |
| 4 | IO_L24N_4 | AM9 | |
| 4 | IO_L24P_4 | AL8 | |
| 4 | IO_L25N_4 | AP5 | |
| 4 | IO_L25P_4 | AP4 | |
| 4 | IO_L26N_4 | AG11 | |
| 4 | IO_L26P_4 | AG12 | |
| 4 | IO_L27N_4 | AN7 | |
| 4 | IO_L27P_4/VREF_4 | AN6 | |
| 4 | IO_L28N_4 | AL10 | |
| 4 | IO_L28P_4 | AL9 | |
| 4 | IO_L29N_4 | AF12 | |
| 4 | IO_L29P_4 | AF13 | |
| 4 | IO_L30N_4 | AK10 | |
| 4 | IO_L30P_4 | AK11 | |
| 4 | IO_L49N_4 | AP7 | |
| 4 | IO_L49P_4 | AP6 | |
| 4 | IO_L50N_4 | AH13 | |
| 4 | IO_L50P_4 | AH12 | |
| 4 | IO_L51N_4 | AJ11 | |
| 4 | IO_L51P_4/VREF_4 | AJ12 | |
| 4 | IO_L52N_4 | AP9 | |
| 4 | IO_L52P_4 | AN8 | |
| 4 | IO_L53N_4 | AG13 | |
| 4 | IO_L53P_4 | AG14 | |
| 4 | IO_L54N_4 | AM11 | |
| 4 | IO_L54P_4 | AL11 | |
| 4 | IO_L60N_4 | AN10 | NC |
| 4 | IO_L60P_4 | AN9 | NC |

*Table 12:* **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

| Bank | Pin Description | Pin Number | No Connect in the XC2V3000 |
|---|---|---|---|
| 5 | IO_L50P_5 | AG22 | |
| 5 | IO_L49N_5 | AN29 | |
| 5 | IO_L49P_5 | AN28 | |
| 5 | IO_L30N_5 | AK24 | |
| 5 | IO_L30P_5 | AK25 | |
| 5 | IO_L29N_5 | AH23 | |
| 5 | IO_L29P_5 | AH22 | |
| 5 | IO_L28N_5 | AP31 | |
| 5 | IO_L28P_5 | AP30 | |
| 5 | IO_L27N_5/VREF_5 | AH24 | |
| 5 | IO_L27P_5 | AH25 | |
| 5 | IO_L26N_5 | AF22 | |
| 5 | IO_L26P_5 | AF23 | |
| 5 | IO_L25N_5 | AM27 | |
| 5 | IO_L25P_5 | AM26 | |
| 5 | IO_L24N_5 | AL27 | |
| 5 | IO_L24P_5 | AL26 | |
| 5 | IO_L23N_5 | AH26 | |
| 5 | IO_L23P_5 | AJ25 | |
| 5 | IO_L22N_5 | AN31 | |
| 5 | IO_L22P_5 | AN30 | |
| 5 | IO_L21N_5/VREF_5 | AK26 | |
| 5 | IO_L21P_5 | AK27 | |
| 5 | IO_L20N_5 | AG23 | |
| 5 | IO_L20P_5 | AF24 | |
| 5 | IO_L19N_5 | AM33 | |
| 5 | IO_L19P_5 | AN32 | |
| 5 | IO_L06N_5 | AJ27 | |
| 5 | IO_L06P_5 | AJ26 | |
| 5 | IO_L05N_5/VRP_5 | AE22 | |
| 5 | IO_L05P_5/VRN_5 | AE23 | |
| 5 | IO_L04N_5 | AM28 | |
| 5 | IO_L04P_5/VREF_5 | AM29 | |
| 5 | IO_L03N_5/D4/ALT_VRP_5 | AK28 | |
| 5 | IO_L03P_5/D5/ALT_VRN_5 | AL29 | |
| 5 | IO_L02N_5/D6 | AG24 | |

*Table 12:* **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

| Bank | Pin Description | Pin Number | No Connect in the XC2V3000 |
|---|---|---|---|
| 5 | IO_L02P_5/D7 | AG25 | |
| 5 | IO_L01N_5/RDWR_B | AL30 | |
| 5 | IO_L01P_5/CS_B | AM31 | |
| | | | |
| 6 | IO_L01P_6 | AE24 | |
| 6 | IO_L01N_6 | AD25 | |
| 6 | IO_L02P_6/VRN_6 | AJ30 | |
| 6 | IO_L02N_6/VRP_6 | AH30 | |
| 6 | IO_L03P_6 | AL32 | |
| 6 | IO_L03N_6/VREF_6 | AK32 | |
| 6 | IO_L04P_6 | AF25 | |
| 6 | IO_L04N_6 | AE25 | |
| 6 | IO_L05P_6 | AJ31 | |
| 6 | IO_L05N_6 | AK31 | |
| 6 | IO_L06P_6 | AH29 | |
| 6 | IO_L06N_6 | AG29 | |
| 6 | IO_L19P_6 | AG26 | |
| 6 | IO_L19N_6 | AF26 | |
| 6 | IO_L20P_6 | AL33 | |
| 6 | IO_L20N_6 | AK33 | |
| 6 | IO_L21P_6 | AJ32 | |
| 6 | IO_L21N_6/VREF_6 | AH32 | |
| 6 | IO_L22P_6 | AG28 | |
| 6 | IO_L22N_6 | AF28 | |
| 6 | IO_L23P_6 | AG30 | |
| 6 | IO_L23N_6 | AF30 | |
| 6 | IO_L24P_6 | AF29 | |
| 6 | IO_L24N_6 | AE29 | |
| 6 | IO_L25P_6 | AF27 | |
| 6 | IO_L25N_6 | AE27 | |
| 6 | IO_L26P_6 | AL34 | |
| 6 | IO_L26N_6 | AK34 | |
| 6 | IO_L27P_6 | AE28 | |
| 6 | IO_L27N_6/VREF_6 | AD28 | |
| 6 | IO_L28P_6 | AE26 | |
| 6 | IO_L28N_6 | AD26 | |

*Table 12:* **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

| Bank | Pin Description | Pin Number | No Connect in the XC2V3000 |
|---|---|---|---|
| NA | GND | B34 | |
| NA | GND | B33 | |
| NA | GND | B20 | |
| NA | GND | B15 | |
| NA | GND | B2 | |
| NA | GND | B1 | |
| NA | GND | A33 | |
| NA | GND | A32 | |
| NA | GND | A27 | |
| NA | GND | A8 | |
| NA | GND | A3 | |
| NA | GND | A2 | |

**Notes:**
1. See Table 4 for an explanation of the signals available on this pin.

*Table 13:* **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

| Bank | Pin Description | Pin Number | No Connect in the XC2V4000 | No Connect in the XC2V6000 |
|---|---|---|---|---|
| 7 | IO_L74P_7 | U31 | | |
| 7 | IO_L74N_7 | T31 | | |
| 7 | IO_L73P_7 | R38 | | |
| 7 | IO_L73N_7 | T38 | | |
| 7 | IO_L72P_7 | T33 | | |
| 7 | IO_L72N_7 | U33 | | |
| 7 | IO_L71P_7 | U30 | | |
| 7 | IO_L71N_7 | T30 | | |
| 7 | IO_L70P_7 | R37 | | |
| 7 | IO_L70N_7 | T37 | | |
| 7 | IO_L69P_7/VREF_7 | R36 | | |
| 7 | IO_L69N_7 | T36 | | |
| 7 | IO_L68P_7 | T32 | | |
| 7 | IO_L68N_7 | R32 | | |
| 7 | IO_L67P_7 | P39 | | |
| 7 | IO_L67N_7 | R39 | | |
| 7 | IO_L60P_7 | R35 | | |
| 7 | IO_L60N_7 | T35 | | |
| 7 | IO_L59P_7 | U28 | | |
| 7 | IO_L59N_7 | T28 | | |
| 7 | IO_L58P_7 | N37 | | |
| 7 | IO_L58N_7 | P37 | | |
| 7 | IO_L57P_7/VREF_7 | R34 | | |
| 7 | IO_L57N_7 | T34 | | |
| 7 | IO_L56P_7 | T29 | | |
| 7 | IO_L56N_7 | R29 | | |
| 7 | IO_L55P_7 | M39 | | |
| 7 | IO_L55N_7 | N39 | | |
| 7 | IO_L54P_7 | N36 | | |
| 7 | IO_L54N_7 | P36 | | |
| 7 | IO_L53P_7 | R30 | | |
| 7 | IO_L53N_7 | P30 | | |
| 7 | IO_L52P_7 | M38 | | |
| 7 | IO_L52N_7 | N38 | | |
| 7 | IO_L51P_7/VREF_7 | P33 | | |
| 7 | IO_L51N_7 | R33 | | |