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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	64
Number of Logic Elements/Cells	-
Total RAM Bits	73728
Number of I/O	88
Number of Gates	40000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-TFBGA, CSPBGA
Supplier Device Package	144-LCSBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v40-5csg144c

Virtex-II Platform FPGAs: Introduction and Overview

DS031-1 (v3.5) November 5, 2007 **Product Specification**

Summary of Virtex-II™ Features

- Industry First Platform FPGA Solution
- IP-Immersion Architecture
  - Densities from 40K to 8M system gates
  - 420 MHz internal clock speed (Advance Data)
  - 840+ Mb/s I/O (Advance Data)
- SelectRAM™ Memory Hierarchy
  - 3 Mb of dual-port RAM in 18 Kbit block SelectRAM resources
  - Up to 1.5 Mb of distributed SelectRAM resources
- High-Performance Interfaces to External Memory
  - DRAM interfaces
    - SDR / DDR SDRAM
    - Network FCRAM
    - Reduced Latency DRAM
  - SRAM interfaces
    - SDR / DDR SRAM
    - QDR™ SRAM
  - CAM interfaces
- Arithmetic Functions
  - Dedicated 18-bit x 18-bit multiplier blocks
  - Fast look-ahead carry logic chains
- Flexible Logic Resources
  - Up to 93,184 internal registers / latches with Clock Enable
  - Up to 93,184 look-up tables (LUTs) or cascadable 16-bit shift registers
  - Wide multiplexers and wide-input function support
  - Horizontal cascade chain and sum-of-products support
  - Internal 3-state bussing
- High-Performance Clock Management Circuitry
  - Up to 12 DCM (Digital Clock Manager) modules
    - Precise clock de-skew
    - Flexible frequency synthesis
    - High-resolution phase shifting
  - 16 global clock multiplexer buffers
- Active Interconnect Technology
  - Fourth generation segmented routing structure
  - Predictable, fast routing delay, independent of fanout
- SelectIO™-Ultra Technology
  - Up to 1,108 user I/Os
  - 19 single-ended and six differential standards
  - Programmable sink current (2 mA to 24 mA) per I/O
  - Digitally Controlled Impedance (DCI) I/O: on-chip termination resistors for single-ended I/O standards
  - PCI-X compatible (133 MHz and 66 MHz) at 3.3V
  - PCI compliant (66 MHz and 33 MHz) at 3.3V
  - CardBus compliant (33 MHz) at 3.3V
  - Differential Signaling
    - 840 Mb/s Low-Voltage Differential Signaling I/O (LVDS) with current mode drivers
    - Bus LVDS I/O
    - Lightning Data Transport (LDT) I/O with current driver buffers
    - Low-Voltage Positive Emitter-Coupled Logic (LVPECL) I/O
    - Built-in DDR input and output registers
  - Proprietary high-performance SelectLink Technology
    - High-bandwidth data path
    - Double Data Rate (DDR) link
    - Web-based HDL generation methodology
- Supported by Xilinx Foundation™ and Alliance Series™ Development Systems
  - Integrated VHDL and Verilog design flows
  - Compilation of 10M system gates designs
  - Internet Team Design (ITD) tool
- SRAM-Based In-System Configuration
  - Fast SelectMAP configuration
  - Triple Data Encryption Standard (DES) security option (Bitstream Encryption)
  - IEEE 1532 support
  - Partial reconfiguration
  - Unlimited reprogrammability
  - Readback capability
- 0.15 µm 8-Layer Metal Process with 0.12 µm High-Speed Transistors
- 1.5V (V_{CCINT}) Core Power Supply, Dedicated 3.3V V_{CCAUX} Auxiliary and V_{CCO} I/O Power Supplies
- IEEE 1149.1 Compatible Boundary-Scan Logic Support
- Flip-Chip and Wire-Bond Ball Grid Array (BGA) Packages in Three Standard Fine Pitches (0.80 mm, 1.00 mm, and 1.27 mm)
- Wire-Bond BGA Devices Available in Pb-Free Packaging (www.xilinx.com/pbfree)
- 100% Factory Tested

Boundary Scan

Boundary scan instructions and associated data registers support a standard methodology for accessing and configuring Virtex-II devices that complies with IEEE standards 1149.1 — 1993 and 1532. A system mode and a test mode are implemented. In system mode, a Virtex-II device performs its intended mission even while executing non-test boundary-scan instructions. In test mode, boundary-scan test instructions control the I/O pins for testing purposes. The Virtex-II Test Access Port (TAP) supports BYPASS, PRELOAD, SAMPLE, IDCODE, and USERCODE non-test instructions. The EXTEST, INTEST, and HIGHZ test instructions are also supported.

Configuration

Virtex-II devices are configured by loading data into internal configuration memory, using the following five modes:

- Slave-serial mode
- Master-serial mode
- Slave SelectMAP mode
- Master SelectMAP mode
- Boundary-Scan mode (IEEE 1532)

A Data Encryption Standard (DES) decryptor is available on-chip to secure the bitstreams. One or two triple-DES key sets can be used to optionally encrypt the configuration information.

Readback and Integrated Logic Analyzer

Configuration data stored in Virtex-II configuration memory can be read back for verification. Along with the configuration data, the contents of all flip-flops/latches, distributed SelectRAM, and block SelectRAM memory resources can be read back. This capability is useful for real-time debugging.

The Integrated Logic Analyzer (ILA) core and software provides a complete solution for accessing and verifying Virtex-II devices.

Virtex-II Device/Package Combinations and Maximum I/O

Wire-bond and flip-chip packages are available. Table 4 and Table 5 show the maximum possible number of user I/Os in wire-bond and flip-chip packages, respectively. Table 6 shows the number of available user I/Os for all device/package combinations.

- CS denotes wire-bond chip-scale ball grid array (BGA) (0.80 mm pitch).
- CSG denotes Pb-free wire-bond chip-scale ball grid array (BGA) (0.80 mm pitch).
- FG denotes wire-bond fine-pitch BGA (1.00 mm pitch).
- FGG denotes Pb-free wire-bond fine-pitch BGA (1.00 mm pitch).
- BG denotes standard BGA (1.27 mm pitch).
- BGG denotes Pb-free standard BGA (1.27 mm pitch).
- FF denotes flip-chip fine-pitch BGA (1.00 mm pitch).
- BF denotes flip-chip BGA (1.27 mm pitch).

The number of I/Os per package include all user I/Os except the 15 control pins (CCLK, DONE, M0, M1, M2, PROG_B, PWRDWN_B, TCK, TDI, TDO, TMS, HSWAP_EN, DXN, DXP, and RSVD) and VBATT.

Table 4: **Wire-Bond Packages Information**

Package[1]	CS144/ CSG144	FG256/ FGG256	FG456/ FGG456	FG676/ FGG676	BG575/ BGG575	BG728/ BGG728
Pitch (mm)	0.80	1.00	1.00	1.00	1.27	1.27
Size (mm)	12 x 12	17 x 17	23 x 23	27 x 27	31 x 31	35 x 35
I/Os	92	172	324	484	408	516

Notes:
1. Wire-bond packages include FGG*nnn* Pb-free versions. See Virtex-II Ordering Examples (Module 1).

Table 5: **Flip-Chip Packages Information**

Package	FF896	FF1152	FF1517	BF957
Pitch (mm)	1.00	1.00	1.00	1.27
Size (mm)	31 x 31	35 x 35	40 x 40	40 x 40
I/Os	624	824	1,108	684

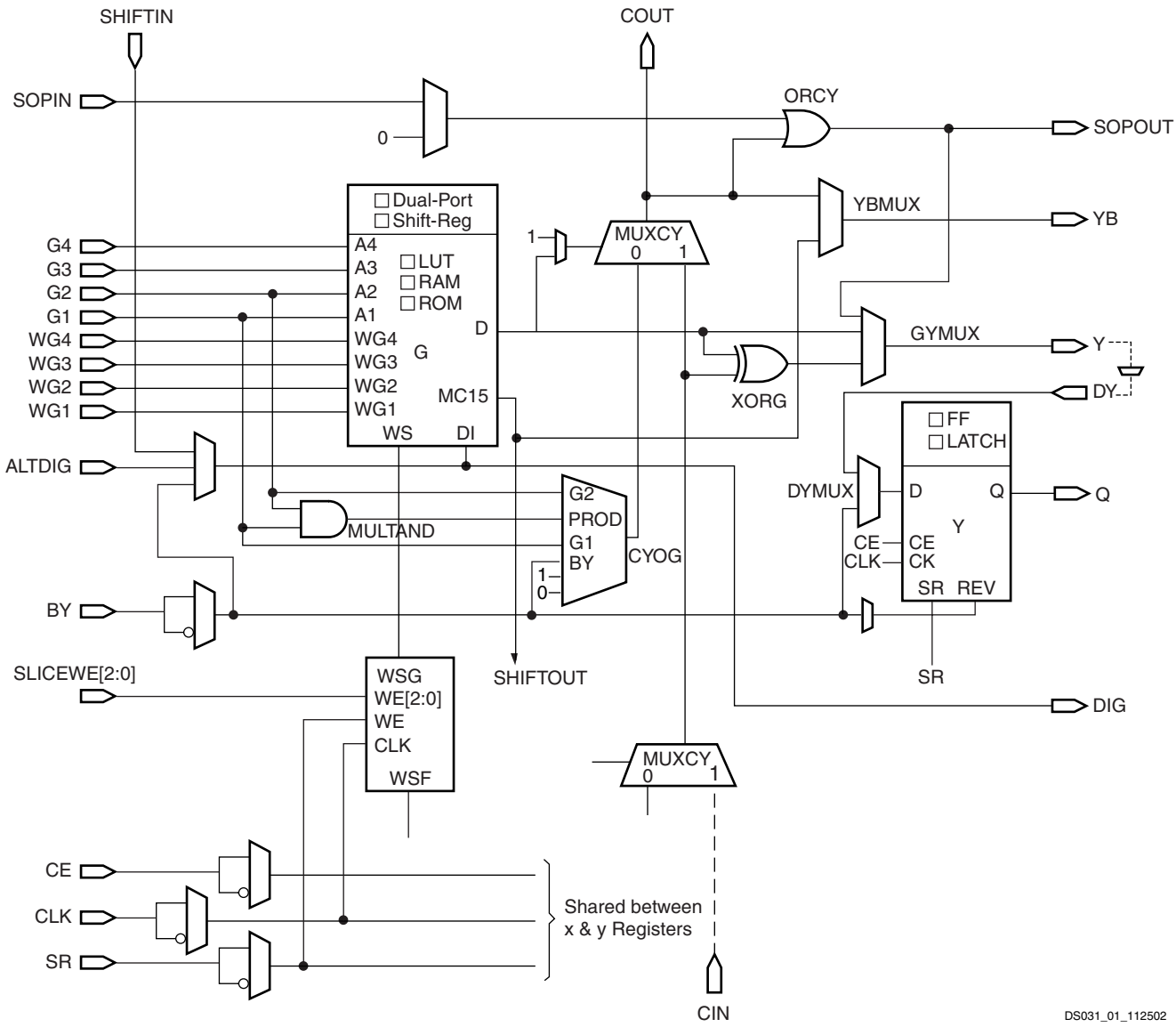


Figure 16: **Virtex-II Slice (Top Half)**

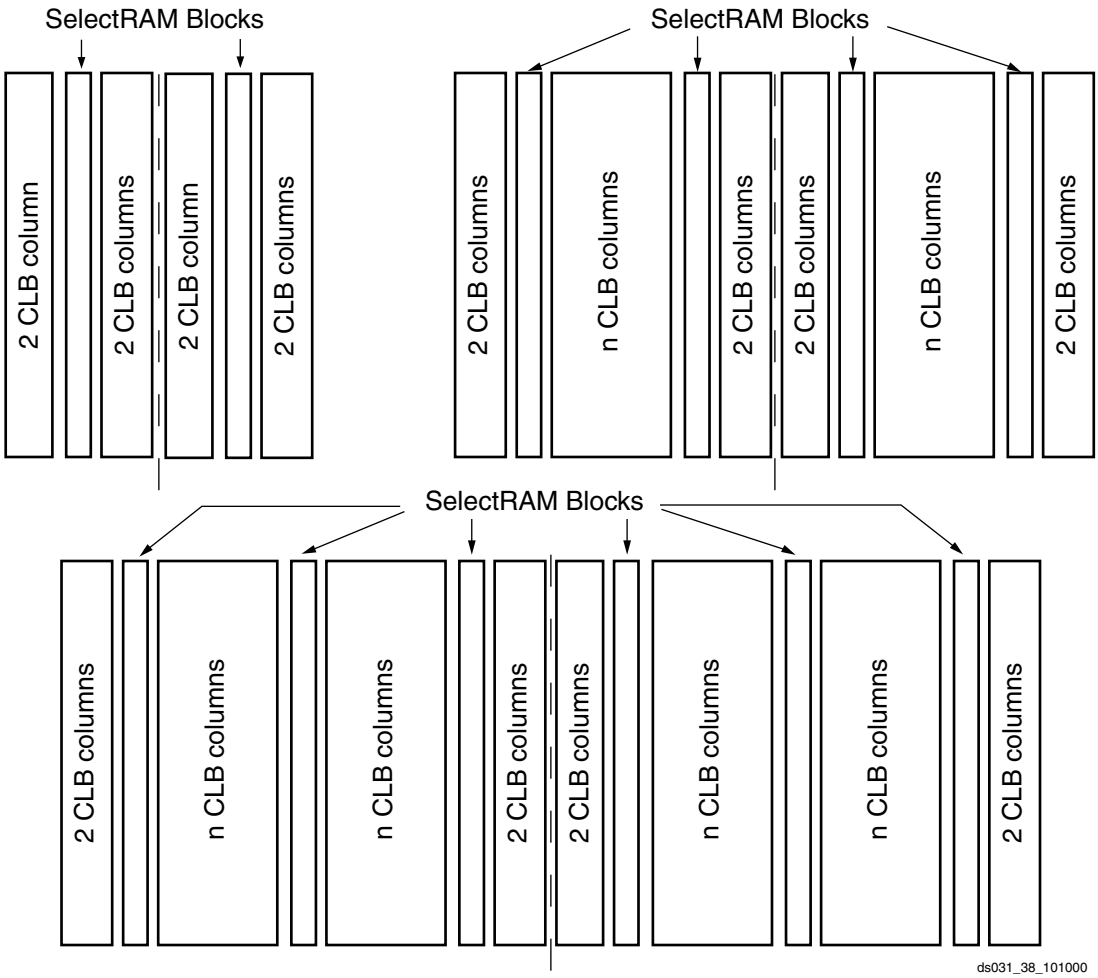


Figure 34: **Block SelectRAM (2-column, 4-column, and 6-column)**

Total Amount of SelectRAM Memory

Table 19 shows the amount of block SelectRAM memory available for each Virtex-II device. The 18 Kbit SelectRAM blocks are cascadable to implement deeper or wider single- or dual-port memory resources.

Table 19: **Virtex-II SelectRAM Memory Available**

Device	Total SelectRAM Memory		
	Blocks	in Kbits	in Bits
XC2V40	4	72	73,728
XC2V80	8	144	147,456
XC2V250	24	432	442,368
XC2V500	32	576	589,824
XC2V1000	40	720	737,280
XC2V1500	48	864	884,736
XC2V2000	56	1,008	1,032,192
XC2V3000	96	1,728	1,769,472
XC2V4000	120	2,160	2,211,840
XC2V6000	144	2,592	2,654,208
XC2V8000	168	3,024	3,096,576

18-Bit x 18-Bit Multipliers

Introduction

A Virtex-II multiplier block is an 18-bit by 18-bit 2's complement signed multiplier. Virtex-II devices incorporate many embedded multiplier blocks. These multipliers can be associated with an 18 Kbit block SelectRAM resource or can be used independently. They are optimized for high-speed operations and have a lower power consumption compared to an 18-bit x 18-bit multiplier in slices.

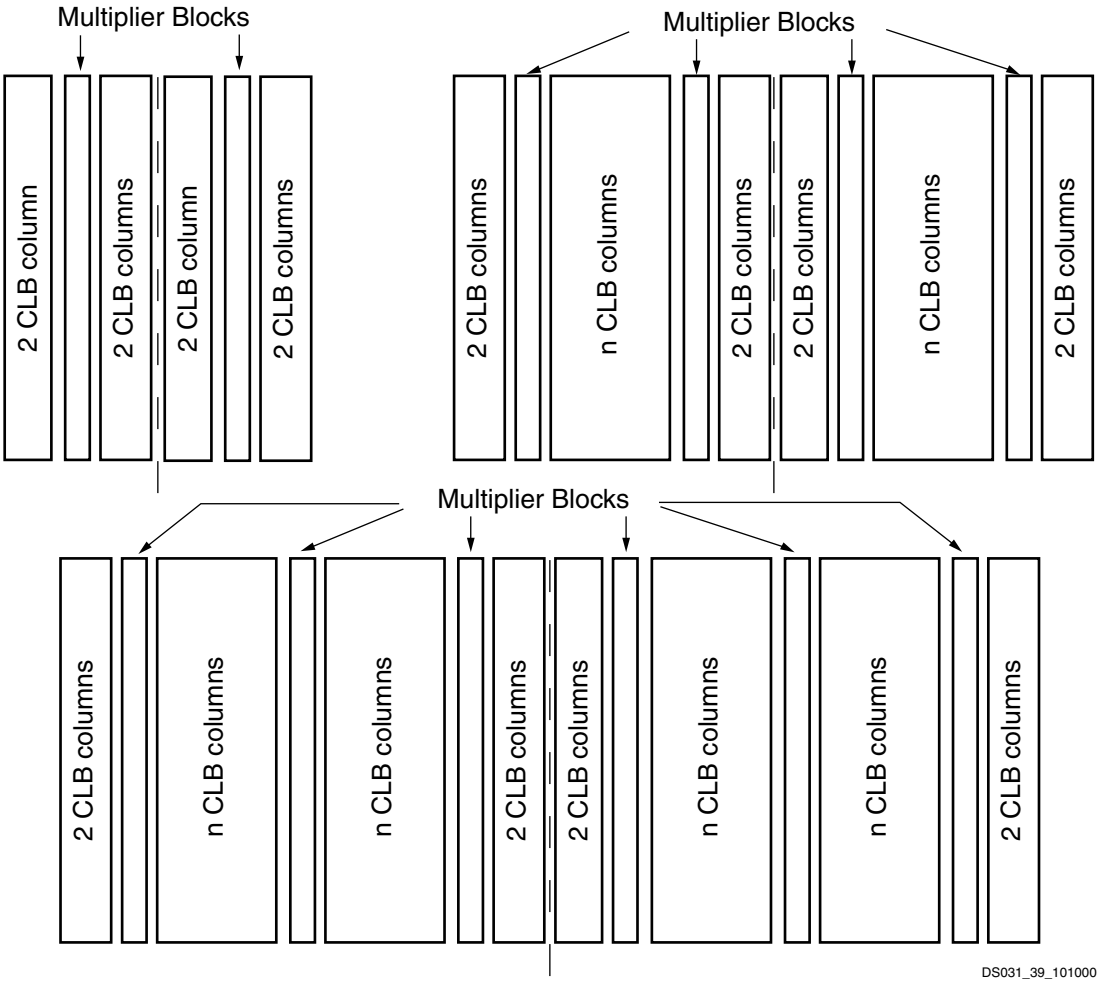


Figure 37: **Multipliers (2-column, 4-column, and 6-column)**

Global Clock Multiplexer Buffers

Virtex-II devices have 16 clock input pins that can also be used as regular user I/Os. Eight clock pads are on the top edge of the device, in the middle of the array, and eight are on the bottom edge, as illustrated in Figure 38.

The global clock multiplexer buffer represents the input to dedicated low-skew clock tree distribution in Virtex-II devices. Like the clock pads, eight global clock multiplexer buffers are on the top edge of the device and eight are on the bottom edge.

Each global clock buffer can either be driven by the clock pad to distribute a clock directly to the device, or driven by the Digital Clock Manager (DCM), discussed in Digital Clock Manager (DCM), page 29. Each global clock buffer can also be driven by local interconnects. The DCM has clock output(s) that can be connected to global clock buffer inputs, as shown in Figure 39.

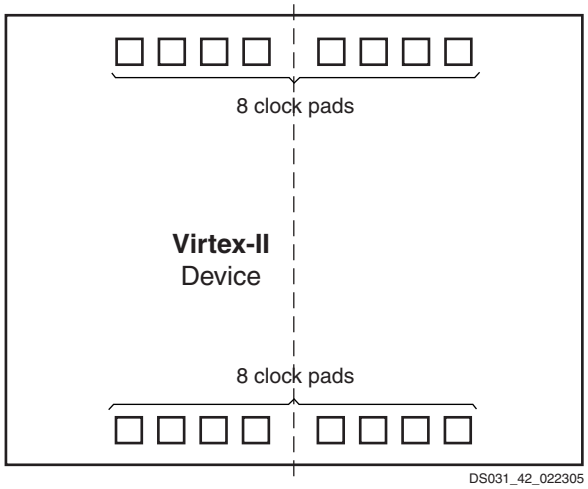


Figure 38: **Virtex-II Clock Pads**

Table 4: **Quiescent Supply Current**

Symbol	Description	Device	Min	Typical	Max	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC2V40		3	125	mA
		XC2V80		5	125	
		XC2V250		8	150	
		XC2V500		10	200	
		XC2V1000		12	250	
		XC2V1500		15	350	
		XC2V2000		20	400	
		XC2V3000		27	500	
		XC2V4000		35	650	
		XC2V6000		45	800	
		XC2V8000		60	1100	
I_{CCOQ}	Quiescent V_{CCO} supply current(1,2)	XC2V40		1	2	mA
		XC2V80		1	2	
		XC2V250		1	2	
		XC2V500		1	2	
		XC2V1000		1	2	
		XC2V1500		2	4	
		XC2V2000		2	4	
		XC2V3000		2	4	
		XC2V4000		2	4	
		XC2V6000		2	4	
		XC2V8000		2	4	
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current(1,2)	XC2V40		5	25	mA
		XC2V80		5	25	
		XC2V250		5	25	
		XC2V500		5	25	
		XC2V1000		5	25	
		XC2V1500		7.5	50	
		XC2V2000		7.5	50	
		XC2V3000		10	75	
		XC2V4000		10	75	
		XC2V6000		12.5	100	
		XC2V8000		12.5	100	

Notes:
1. With no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
2. If DCI or differential signaling is used, more accurate values can be obtained by using the Power Estimator or XPOWER™.
3. Data are retained even if V_{CCO} drops to 0 V.
4. Values specified for quiescent supply current parameters are Commercial Grade. For Industrial Grade values, multiply Commercial Grade values by 1.25.

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device operation. The actual current consumed depends on the power-on ramp rate of the power supply.

The V_{CCINT}, V_{CCAUX}, and V_{CCO} power supplies shall each ramp on, monotonically, no faster than 200 µs and no slower than 50 ms. Ramp on is defined as: 0 V_{DC} to minimum supply voltages.

Table 5 shows the minimum current required by Virtex-II devices for proper power on and configuration.

Power supplies can be turned on in any sequence.(1)

If any V_{CCO} bank powers up before V_{CCAUX}, then each bank draws up to 300 mA, worst case, until the V_{CCAUX} powers up.(2) This does not harm the device. If the current is limited to the minimum value above, or larger, the device powers on properly after all three supplies have passed through their power-on reset threshold voltages.

Once initialized and configured, use the power calculator to estimate current drain on these supplies.

Notes:
1. If the V_{CCINT} ramp rate is longer than 10 ms, then V_{CCINT} must be applied before V_{CCO} and V_{CCAUX}. The device will not be damaged if this requirement is violated, but configuration will probably fail.
2. The 300 mA is transient current (peak); it eventually disappears even if V_{CCAUX} does not power up.

Extended LVDS DC Specifications (LVDSEXT_33 & LVDSEXT_25)

Table 9: **Extended LVDS DC Specifications**

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}			3.3 or 2.5		V
Output High voltage for Q and $\overline{Q}$	V_{OH}	R_T = 100 Ω across Q and $\overline{Q}$ signals			1.785	V
Output Low voltage for Q and $\overline{Q}$	V_{OL}	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.705			V
Differential output voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{ODIFF}	R_T = 100 Ω across Q and $\overline{Q}$ signals	440		820	mV
Output common-mode voltage	V_{OCM}	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.200	1.375	V
Differential input voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{IDIFF}	Common-mode input voltage = 1.25 V	100	350	N/A	mV
Input common-mode voltage	V_{ICM}	Differential input voltage = ±350 mV	0.2	1.25	V_{CCO} – 0.5	V

LVPECL DC Specifications

These values are valid when driving a 100 Ω differential load only, i.e., a 100 Ω resistor between the two receiver pins. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. Table 10 summarizes the DC output specifications of LVPECL. For more information on using LVPECL, see the *Virtex-II User Guide*.

Table 10: **LVPECL DC Specifications**

DC Parameter	Min	Max	Min	Max	Min	Max	Units
V_{CCO}	3.0		3.3		3.6		V
V_{OH}	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{OL}	0.96	1.27	1.06	1.43	1.30	1.57	V
V_{IH}	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	0.86	2.125	0.86	2.125	0.86	2.125	V
Differential Input Voltage	0.3	–	0.3	–	0.3	–	V

IOB Input Switching Characteristics Standard Adjustments

Table 15 gives all standard-specific data input delay adjustments.

Table 15: **IOB Input Switching Characteristics Standard Adjustments**

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-6	-5	-4	
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL	T_{ILVTTL}	0.00	0.00	0.00	ns
LVCMOS (Low-Voltage CMOS), 3.3V	LVCMOS33	$T_{ILVCMOS33}$	0.00	0.00	0.00	ns
LVCMOS, 2.5V	LVCMOS25	$T_{ILVCMOS25}$	0.11	0.11	0.12	ns
LVCMOS, 1.8V	LVCMOS18	$T_{ILVCMOS18}$	0.42	0.43	0.49	ns
LVCMOS, 1.5V	LVCMOS15	$T_{ILVCMOS15}$	0.98	1.00	1.15	ns
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	T_{ILVDS_25}	0.60	0.60	0.69	ns
LVDS, 3.3V	LVDS_33	T_{ILVDS_33}	0.60	0.60	0.69	ns
LVDSEXT (Extended Mode), 2.5V	LVDSEXT_25	$T_{ILVDSEXT\_25}$	0.68	0.69	0.79	ns
LVDSEXT, 3.3V	LVDSEXT_33	$T_{ILVDSEXT\_33}$	0.56	0.56	0.65	ns
ULVDS (Ultra LVDS), 2.5V	ULVDS_25	T_{IULVDS_25}	0.48	0.49	0.56	ns
BLVDS (Bus LVDS), 2.5V	BLVDS_25	T_{IBLVDS_25}	0.68	0.69	0.79	ns
LDT (HyperTransport), 2.5V	LDT_25	T_{ILDT_25}	0.48	0.49	0.56	ns
LVPECL (Low-Voltage Positive Electron-Coupled Logic), 3.3V	LVPECL_33	$T_{ILVPECL\_33}$	0.60	0.60	0.69	ns
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3	T_{IPCI33_3}	0.00	0.00	0.00	ns
PCI, 66 MHz, 3.3V	PCI66_3	T_{IPCI66_3}	0.00	0.00	0.00	ns
PCI-X, 133 MHz, 3.3V	PCIX	T_{IPCIX}	0.00	0.00	0.00	ns
GTL (Gunning Transceiver Logic)	GTL	T_{IGTL}	0.42	0.42	0.48	ns
GTL Plus	GTLP	T_{IGTLP}	0.42	0.42	0.48	ns
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	T_{IHSTL_I}	0.42	0.42	0.48	ns
HSTL, Class II	HSTL_II	T_{IHSTL_II}	0.42	0.42	0.48	ns
HSTL, Class III	HSTL_III	T_{IHSTL_III}	0.42	0.42	0.48	ns
HSTL, Class IV	HSTL_IV	T_{IHSTL_IV}	0.42	0.42	0.48	ns
HSTL, Class I, 1.8V	HSTL_I_18	$T_{IHSTL\_I\_18}$	0.42	0.42	0.48	ns
HSTL, Class II, 1.8V	HSTL_II_18	$T_{IHSTL\_II\_18}$	0.42	0.42	0.48	ns
HSTL, Class III, 1.8V	HSTL_III_18	$T_{IHSTL\_III\_18}$	0.42	0.42	0.48	ns
HSTL, Class IV, 1.8V	HSTL_IV_18	$T_{IHSTL\_IV\_18}$	0.42	0.42	0.48	ns
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	$T_{ISSTL18\_I}$	0.42	0.42	0.48	ns
SSTL, Class II, 1.8V	SSTL18_II	$T_{ISSTL18\_II}$	0.42	0.42	0.48	ns
SSTL, Class I, 2.5V	SSTL2_I	T_{ISSTL2_I}	0.42	0.42	0.48	ns
SSTL, Class II, 2.5V	SSTL2_II	T_{ISSTL2_II}	0.42	0.42	0.48	ns
SSTL, Class I, 3.3V	SSTL3_I	T_{ISSTL3_I}	0.35	0.35	0.40	ns
SSTL, Class II, 3.3V	SSTL3_ II	T_{ISSTL3_II}	0.35	0.35	0.40	ns
AGP-2X/AGP (Accelerated Graphics Port)	AGP	T_{IAGP}	0.35	0.35	0.40	ns
LVDCI (Low-Voltage Digitally Controlled Impedance), 3.3V	LVDCI_33	T_{ILVDCI_33}	0.00	0.00	0.00	ns
LVDCI, 2.5V	LVDCI_25	T_{ILVDCI_25}	0.11	0.11	0.12	ns
LVDCI, 1.8V	LVDCI_18	T_{ILVDCI_18}	0.42	0.43	0.49	ns
LVDCI, 1.5V	LVDCI_15	T_{ILVDCI_15}	0.98	1.00	1.14	ns

Table 6: **FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
NA	GND	T16		
NA	GND	T1		
NA	GND	R15		
NA	GND	R2		
NA	GND	P14		
NA	GND	P3		
NA	GND	L11		
NA	GND	L6		
NA	GND	K10		
NA	GND	K9		
NA	GND	K8		
NA	GND	K7		
NA	GND	J10		
NA	GND	J9		
NA	GND	J8		
NA	GND	J7		
NA	GND	H10		
NA	GND	H9		
NA	GND	H8		
NA	GND	H7		
NA	GND	G10		
NA	GND	G9		
NA	GND	G8		
NA	GND	G7		
NA	GND	F11		
NA	GND	F6		
NA	GND	C14		
NA	GND	C3		
NA	GND	B15		
NA	GND	B2		
NA	GND	A16		
NA	GND	A1		

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
7	VCCO_7	H6		
7	VCCO_7	G6		
NA	CCLK	Y19		
NA	PROG_B	A2		
NA	DONE	AB20		
NA	M0	AB2		
NA	M1	W3		
NA	M2	AB3		
NA	HSWAP_EN	B3		
NA	TCK	C19		
NA	TDI	D3		
NA	TDO	D20		
NA	TMS	B20		
NA	PWRDWN_B	AB21		
NA	DXN	D5		
NA	DXP	A3		
NA	VBATT	A21		
NA	RSVD	A20		
NA	VCCAUX	AB11		
NA	VCCAUX	AA22		
NA	VCCAUX	AA1		
NA	VCCAUX	M22		
NA	VCCAUX	L1		
NA	VCCAUX	B22		
NA	VCCAUX	B1		
NA	VCCAUX	A12		
NA	VCCINT	U17		
NA	VCCINT	U6		
NA	VCCINT	T16		
NA	VCCINT	T15		
NA	VCCINT	T8		
NA	VCCINT	T7		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
3	IO_L24N_3	AC8		
3	IO_L24P_3	AB8		
3	IO_L23N_3	AE2		
3	IO_L23P_3	AF3		
3	IO_L22N_3	AD3		
3	IO_L22P_3	AE3		
3	IO_L21N_3/VREF_3	AD6		
3	IO_L21P_3	AD7		
3	IO_L20N_3	AF1		
3	IO_L20P_3	AG1		
3	IO_L19N_3	AD4		
3	IO_L19P_3	AE4		
3	IO_L06N_3	AD8		
3	IO_L06P_3	AE7		
3	IO_L05N_3	AG2		
3	IO_L05P_3	AH2		
3	IO_L04N_3	AD5		
3	IO_L04P_3	AE5		
3	IO_L03N_3/VREF_3	AC9		
3	IO_L03P_3	AD9		
3	IO_L02N_3/VRP_3	AH1		
3	IO_L02P_3/VRN_3	AJ1		
3	IO_L01N_3	AF4		
3	IO_L01P_3	AG3		
4	IO_L01N_4/BUSY/DOUT(1)	AK2		
4	IO_L01P_4/INIT_B	AJ3		
4	IO_L02N_4/D0/DIN(1)	AE8		
4	IO_L02P_4/D1	AF9		
4	IO_L03N_4/D2/ALT_VRP_4	AH5		
4	IO_L03P_4/D3/ALT_VRN_4	AH6		
4	IO_L04N_4/VREF_4	AJ4		
4	IO_L04P_4	AK4		
4	IO_L05N_4/VRP_4	AC10		
4	IO_L05P_4/VRN_4	AC11		
4	IO_L06N_4	AH7		
4	IO_L06P_4	AG6		

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
1	IO_L69P_1	F13	
1	IO_L68N_1	C11	
1	IO_L68P_1	C12	
1	IO_L67N_1	B11	
1	IO_L67P_1	B12	
1	IO_L60N_1	F11	NC
1	IO_L60P_1	F12	NC
1	IO_L54N_1	D10	
1	IO_L54P_1	D11	
1	IO_L53N_1	G12	
1	IO_L53P_1	G13	
1	IO_L52N_1	B9	
1	IO_L52P_1	B10	
1	IO_L51N_1/VREF_1	B8	
1	IO_L51P_1	A9	
1	IO_L50N_1	K14	
1	IO_L50P_1	K13	
1	IO_L49N_1	A6	
1	IO_L49P_1	A7	
1	IO_L30N_1	D9	
1	IO_L30P_1	C9	
1	IO_L29N_1	H13	
1	IO_L29P_1	H12	
1	IO_L28N_1	C7	
1	IO_L28P_1	C8	
1	IO_L27N_1/VREF_1	E11	
1	IO_L27P_1	E10	
1	IO_L26N_1	J13	
1	IO_L26P_1	K12	
1	IO_L25N_1	B6	
1	IO_L25P_1	B7	
1	IO_L24N_1	E8	
1	IO_L24P_1	E9	
1	IO_L23N_1	G10	
1	IO_L23P_1	G11	
1	IO_L22N_1	A4	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
1	IO_L22P_1	A5	
1	IO_L21N_1/VREF_1	F10	
1	IO_L21P_1	G9	
1	IO_L20N_1	J12	
1	IO_L20P_1	J11	
1	IO_L19N_1	B4	
1	IO_L19P_1	B5	
1	IO_L06N_1	D6	
1	IO_L06P_1	C6	
1	IO_L05N_1	H11	
1	IO_L05P_1	J10	
1	IO_L04N_1	D8	
1	IO_L04P_1/VREF_1	E7	
1	IO_L03N_1/VRP_1	F9	
1	IO_L03P_1/VRN_1	F8	
1	IO_L02N_1	H10	
1	IO_L02P_1	H9	
1	IO_L01N_1	C2	
1	IO_L01P_1	B3	
2	IO_L01N_2	E2	
2	IO_L01P_2	D2	
2	IO_L02N_2/VRP_2	K11	
2	IO_L02P_2/VRN_2	K10	
2	IO_L03N_2	F5	
2	IO_L03P_2/VREF_2	G5	
2	IO_L04N_2	E3	
2	IO_L04P_2	D3	
2	IO_L05N_2	J9	
2	IO_L05P_2	K9	
2	IO_L06N_2	F4	
2	IO_L06P_2	E4	
2	IO_L19N_2	E1	
2	IO_L19P_2	D1	
2	IO_L20N_2	J8	
2	IO_L20P_2	K8	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
4	IO_L67N_4	AN12	
4	IO_L67P_4	AN11	
4	IO_L68N_4	AE14	
4	IO_L68P_4	AE15	
4	IO_L69N_4	AJ13	
4	IO_L69P_4/VREF_4	AJ14	
4	IO_L70N_4	AL13	
4	IO_L70P_4	AL12	
4	IO_L71N_4	AF14	
4	IO_L71P_4	AF15	
4	IO_L72N_4	AM13	
4	IO_L72P_4	AM12	
4	IO_L73N_4	AP12	
4	IO_L73P_4	AP11	
4	IO_L74N_4	AG15	
4	IO_L74P_4	AG16	
4	IO_L75N_4	AN14	
4	IO_L75P_4/VREF_4	AN13	
4	IO_L76N_4	AP14	
4	IO_L76P_4	AP13	
4	IO_L77N_4	AD16	
4	IO_L77P_4	AD17	
4	IO_L78N_4	AK14	
4	IO_L78P_4	AK13	
4	IO_L79N_4	AN16	NC
4	IO_L79P_4	AP15	NC
4	IO_L80N_4	AE16	NC
4	IO_L80P_4	AE17	NC
4	IO_L81N_4	AH15	NC
4	IO_L81P_4/VREF_4	AJ15	NC
4	IO_L82N_4	AP17	NC
4	IO_L82P_4	AN17	NC
4	IO_L83N_4	AH17	NC
4	IO_L83P_4	AH16	NC
4	IO_L84N_4	AL15	NC
4	IO_L84P_4	AL14	NC

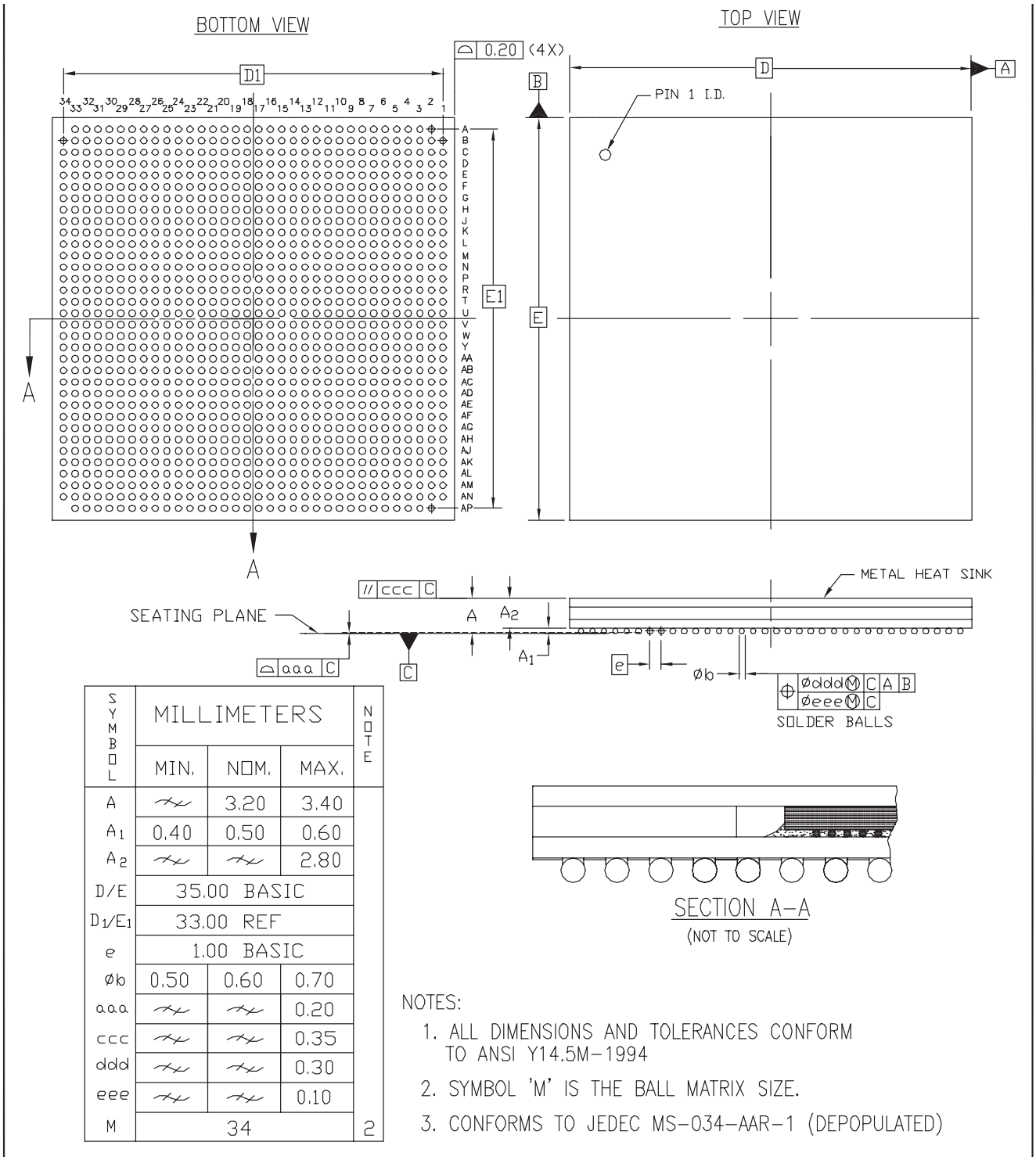
Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
5	IO_L79P_5	AP21	NC
5	IO_L78N_5	AK22	
5	IO_L78P_5	AK21	
5	IO_L77N_5	AD18	
5	IO_L77P_5	AD19	
5	IO_L76N_5	AN22	
5	IO_L76P_5	AN21	
5	IO_L75N_5/VREF_5	AJ20	
5	IO_L75P_5	AH20	
5	IO_L74N_5	AG19	
5	IO_L74P_5	AG20	
5	IO_L73N_5	AP24	
5	IO_L73P_5	AP23	
5	IO_L72N_5	AL23	
5	IO_L72P_5	AL22	
5	IO_L71N_5	AF20	
5	IO_L71P_5	AF21	
5	IO_L70N_5	AM24	
5	IO_L70P_5	AM23	
5	IO_L69N_5/VREF_5	AJ21	
5	IO_L69P_5	AJ22	
5	IO_L68N_5	AJ24	
5	IO_L68P_5	AJ23	
5	IO_L67N_5	AN24	
5	IO_L67P_5	AN23	
5	IO_L60N_5	AN26	NC
5	IO_L60P_5	AN25	NC
5	IO_L54N_5	AL25	
5	IO_L54P_5	AL24	
5	IO_L53N_5	AE20	
5	IO_L53P_5	AE21	
5	IO_L52N_5	AN27	
5	IO_L52P_5	AP26	
5	IO_L51N_5/VREF_5	AP29	
5	IO_L51P_5	AP28	
5	IO_L50N_5	AG21	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
6	IO_L29P_6	AF31	
6	IO_L29N_6	AG31	
6	IO_L30P_6	AF32	
6	IO_L30N_6	AG32	
6	IO_L43P_6	AC25	
6	IO_L43N_6	AB25	
6	IO_L44P_6	AJ33	
6	IO_L44N_6	AH33	
6	IO_L45P_6	AE31	
6	IO_L45N_6/VREF_6	AD32	
6	IO_L46P_6	AD27	
6	IO_L46N_6	AC27	
6	IO_L47P_6	AJ34	
6	IO_L47N_6	AH34	
6	IO_L48P_6	AE30	
6	IO_L48N_6	AD30	
6	IO_L49P_6	AC26	
6	IO_L49N_6	AB26	
6	IO_L50P_6	AD29	
6	IO_L50N_6	AC29	
6	IO_L51P_6	AF33	
6	IO_L51N_6/VREF_6	AG33	
6	IO_L52P_6	AC28	
6	IO_L52N_6	AB28	
6	IO_L53P_6	AF34	
6	IO_L53N_6	AE33	
6	IO_L54P_6	AB27	
6	IO_L54N_6	AA27	
6	IO_L67P_6	AA25	
6	IO_L67N_6	Y25	
6	IO_L68P_6	AD33	
6	IO_L68N_6	AC33	
6	IO_L69P_6	AC32	
6	IO_L69N_6/VREF_6	AB32	
6	IO_L70P_6	AA26	
6	IO_L70N_6	Y26	

FF1152 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A		3.20	3.40	
A_1	0.40	0.50	0.60	
A_2			2.80	
D/E	35.00 BASIC			
D_1/E_1	33.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.35	
ddd			0.30	
eee			0.10	
M	34			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAR–1 (DEPOPULATED)

Figure 8: **FF1152 Flip-Chip Fine-Pitch BGA Package Specifications**

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
2	IO_L81P_2/VREF_2	U5		
2	IO_L82N_2	V2		
2	IO_L82P_2	U2		
2	IO_L83N_2	V8		
2	IO_L83P_2	W8		
2	IO_L84N_2	W7		
2	IO_L84P_2	V7		
2	IO_L91N_2	W1		
2	IO_L91P_2	V1		
2	IO_L92N_2	Y11		
2	IO_L92P_2	Y12		
2	IO_L93N_2	W4		
2	IO_L93P_2/VREF_2	V4		
2	IO_L94N_2	W2		
2	IO_L94P_2	W3		
2	IO_L95N_2	Y8		
2	IO_L95P_2	Y9		
2	IO_L96N_2	W5		
2	IO_L96P_2	W6		
3	IO_L96N_3	AB8		
3	IO_L96P_3	AA8		
3	IO_L95N_3	Y3		
3	IO_L95P_3	AA3		
3	IO_L94N_3	Y6		
3	IO_L94P_3	AA6		
3	IO_L93N_3/VREF_3	AB9		
3	IO_L93P_3	AA9		
3	IO_L92N_3	AA1		
3	IO_L92P_3	AB1		
3	IO_L91N_3	Y5		
3	IO_L91P_3	AA5		
3	IO_L84N_3	AB10		
3	IO_L84P_3	AA10		
3	IO_L83N_3	AA2		
3	IO_L83P_3	AB2		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
5	IO_L79N_5	AV24		
5	IO_L79P_5	AV23		
5	IO_L78N_5	AP23		
5	IO_L78P_5	AP22		
5	IO_L77N_5	AJ21		
5	IO_L77P_5	AJ22		
5	IO_L76N_5	AU24		
5	IO_L76P_5	AU23		
5	IO_L75N_5/VREF_5	AT25		
5	IO_L75P_5	AT24		
5	IO_L74N_5	AH21		
5	IO_L74P_5	AH22		
5	IO_L73N_5	AW26		
5	IO_L73P_5	AW25		
5	IO_L72N_5	AR25		
5	IO_L72P_5	AR24		
5	IO_L71N_5	AN23		
5	IO_L71P_5	AN24		
5	IO_L70N_5	AU25		
5	IO_L70P_5	AV25		
5	IO_L69N_5/VREF_5	AL24		
5	IO_L69P_5	AL23		
5	IO_L68N_5	AK23		
5	IO_L68P_5	AK24		
5	IO_L67N_5	AU27		
5	IO_L67P_5	AU26		
5	IO_L60N_5	AP25		
5	IO_L60P_5	AP24		
5	IO_L59N_5	AM24		
5	IO_L59P_5	AM25		
5	IO_L58N_5	AW28		
5	IO_L58P_5	AW27		
5	IO_L57N_5/VREF_5	AT27		
5	IO_L57P_5	AT26		
5	IO_L56N_5	AH23		
5	IO_L56P_5	AH24		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
3	VCCO_3	AA13		
4	VCCO_4	AV14		
4	VCCO_4	AU18		
4	VCCO_4	AR11		
4	VCCO_4	AN13		
4	VCCO_4	AL15		
4	VCCO_4	AJ17		
4	VCCO_4	AG19		
4	VCCO_4	AG18		
4	VCCO_4	AG17		
4	VCCO_4	AG16		
4	VCCO_4	AG15		
4	VCCO_4	AG14		
4	VCCO_4	AF19		
4	VCCO_4	AF18		
4	VCCO_4	AF17		
4	VCCO_4	AF16		
4	VCCO_4	AF15		
5	VCCO_5	AV26		
5	VCCO_5	AU22		
5	VCCO_5	AR29		
5	VCCO_5	AN27		
5	VCCO_5	AL25		
5	VCCO_5	AJ23		
5	VCCO_5	AG26		
5	VCCO_5	AG25		
5	VCCO_5	AG24		
5	VCCO_5	AG23		
5	VCCO_5	AG22		
5	VCCO_5	AG21		
5	VCCO_5	AF25		
5	VCCO_5	AF24		
5	VCCO_5	AF23		
5	VCCO_5	AF22		
5	VCCO_5	AF21		
6	VCCO_6	AJ35		