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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	64
Number of Logic Elements/Cells	-
Total RAM Bits	73728
Number of I/O	88
Number of Gates	40000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	144-TFBGA, CSPBGA
Supplier Device Package	144-LCSBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v40-5csg144i

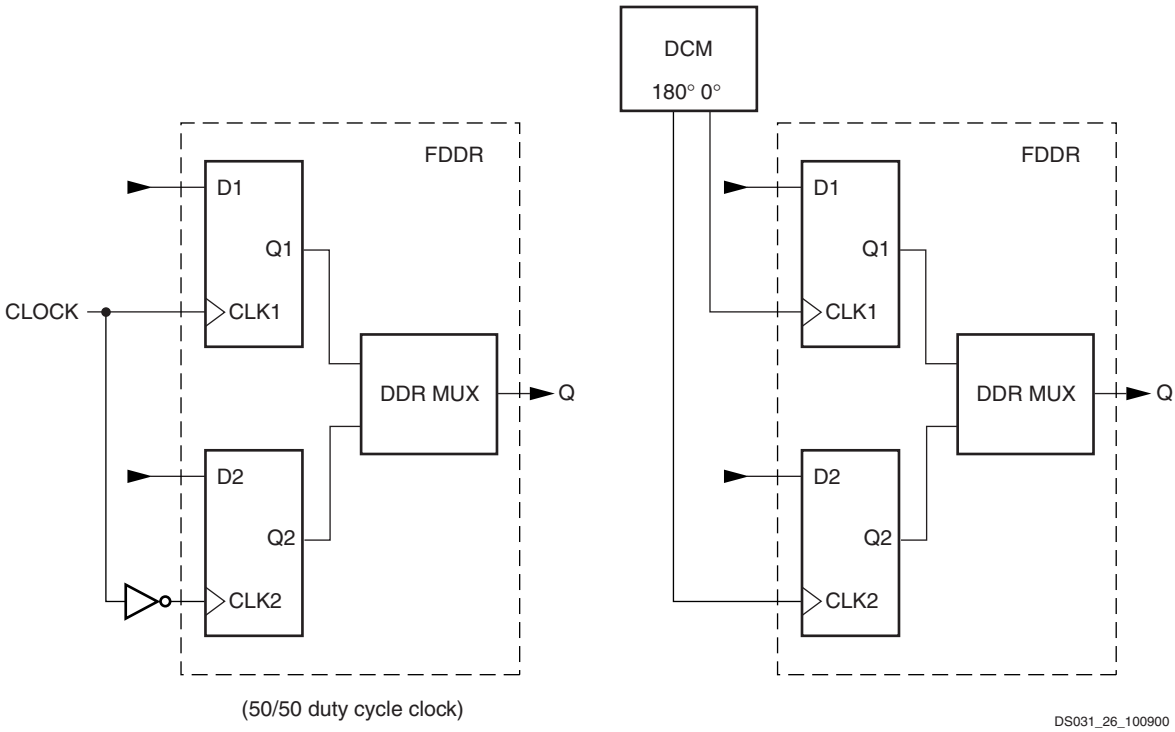


Figure 3: **Double Data Rate Registers**

The DDR mechanism shown in Figure 3 can be used to mirror a copy of the clock on the output. This is useful for propagating a clock along the data that has an identical delay. It is also useful for multiple clock generation, where there is a unique clock driver for every clock load. Virtex-II devices can produce many copies of a clock with very little skew.

Each group of two registers has a clock enable signal (ICE for the input registers, OCE for the output registers, and TCE for the 3-state registers). The clock enable signals are active High by default. If left unconnected, the clock enable for that storage element defaults to the active state.

Each IOB block has common synchronous or asynchronous set and reset (SR and REV signals).

SR forces the storage element into the state specified by the SRHIGH or SRLOW attribute. SRHIGH forces a logic “1”. SRLOW forces a logic “0”. When SR is used, a second input (REV) forces the storage element into the opposite state. The reset condition predominates over the set condition. The initial state after configuration or global initialization state is defined by a separate INIT0 and INIT1 attribute. By default, the SRLOW attribute forces INIT0, and the SRHIGH attribute forces INIT1.

For each storage element, the SRHIGH, SRLOW, INIT0, and INIT1 attributes are independent. Synchronous or asynchronous set / reset is consistent in an IOB block.

All the control signals have independent polarity. Any inverter placed on a control input is automatically absorbed.

Each register or latch (independent of all other registers or latches) (see Figure 4) can be configured as follows:

- No set or reset
- Synchronous set
- Synchronous reset
- Synchronous set and reset
- Asynchronous set (preset)
- Asynchronous reset (clear)
- Asynchronous set and reset (preset and clear)

The synchronous reset overrides a set, and an asynchronous clear overrides a preset.

Table 4: **LVTTL and LVCMOS Programmable Currents (Sink and Source)**

SelectI/O-Ultra	Programmable Current (Worst-Case Guaranteed Minimum)						
LVTTL	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA
LVCMOS33	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA
LVCMOS25	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA
LVCMOS18	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	n/a
LVCMOS15	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	n/a

Figure 6 shows the SSTL2, SSTL3, and HSTL configurations. HSTL can sink current up to 48 mA. (HSTL IV)

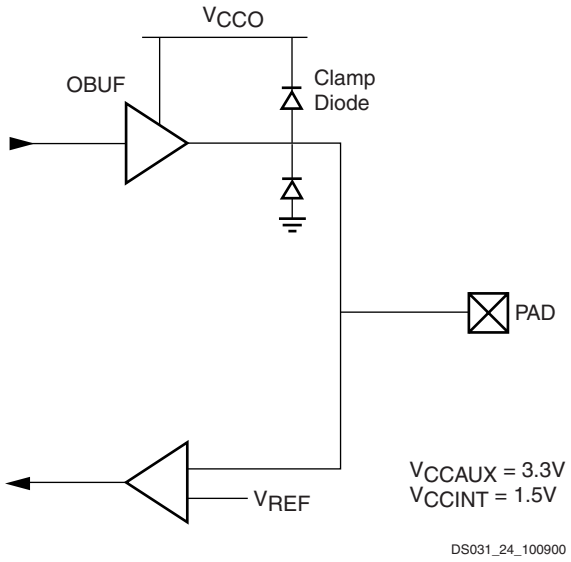


Figure 6: **SSTL or HSTL SelectI/O-Ultra Standards**

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. Virtex-II uses two memory cells to control the configuration of an I/O as an input. This is to reduce the probability of an I/O configured as an input from flipping to an output when subjected to a single event upset (SEU) in space applications.

Prior to configuration, all outputs not involved in configuration are forced into their high-impedance state. The pull-down resistors and the weak-keeper circuits are inactive. The dedicated pin HSWAP_EN controls the pull-up resistors prior to configuration. By default, HSWAP_EN is set high, which disables the pull-up resistors on user I/O pins. When HSWAP_EN is set low, the pull-up resistors are activated on user I/O pins.

All Virtex-II IOBs support IEEE 1149.1 compatible Boundary-Scan testing.

Input Path

The Virtex-II IOB input path routes input signals directly to internal logic and / or through an optional input flip-flop or latch, or through the DDR input registers. An optional delay element at the D-input of the storage element eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the Virtex-II device, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signaling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, V_{REF}. The need to supply V_{REF} imposes constraints on which standards can be used in the same bank. See I/O banking description.

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output and / or the 3-state signal can be routed to the buffer directly from the internal logic or through an output / 3-state flip-flop or latch, or through the DDR output / 3-state registers.

Each output driver can be individually programmed for a wide range of low-voltage signaling standards. In most signaling standards, the output High voltage depends on an externally supplied V_{CCO} voltage. The need to supply V_{CCO} imposes constraints on which standards can be used in the same bank. See I/O banking description.

I/O Banking

Some of the I/O standards described above require V_{CCO} and V_{REF} voltages. These voltages are externally supplied and connected to device pins that serve groups of IOB blocks, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from dividing each edge of the FPGA into two banks, as shown in Figure 7 and Figure 8. Each bank has multiple V_{CCO} pins, all of which must be connected to the same voltage. This voltage is determined by the output standards in use.

JTAG Test Access Port Switching Characteristics

Characterization data for some of the most commonly requested timing parameters shown in Figure 6 is listed in Table 33.

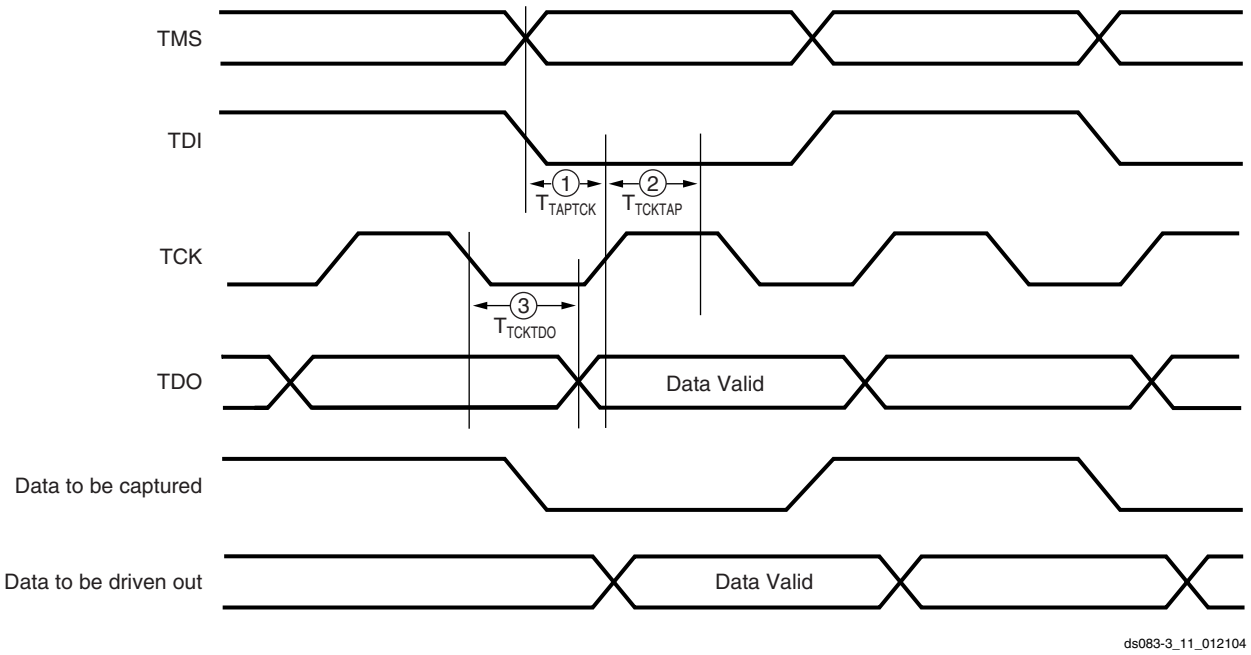


Figure 6: **Virtex-II Pro Boundary Scan Port Timing Waveforms**

Table 33: **Boundary-Scan Port Timing Specifications**

	Description	Figure References	Symbol	Value	Units
TCK	TMS and TDI setup time	1	T_{TAPTCK}	5.5	ns, min
	TMS and TDI hold times	2	T_{TCKTAP}	0.0	ns, min
	Falling edge to TDO output valid	3	T_{TCKTDO}	10.0	ns, max
	Maximum frequency		F_{TCK}	33.0	MHz, max

Global Clock Setup and Hold for LVTTL Standard, *Without* DCM

Table 37: **Global Clock Setup and Hold for LVTTL Standard, *Without* DCM**

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard.(2) For data input with different standards, adjust the setup time delay by the values shown in IOB Input Switching Characteristics Standard Adjustments, page 11.						
Full Delay Global Clock and IFF(1) without DCM	T_{PSFD}/T_{PHFD}	XC2V40	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V80	2.10/ 0.00	2.10/ 0.00	2.21/ 0.00	ns
		XC2V250	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V500	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V1000	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V1500	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V2000	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V3000	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V4000	2.00/ 0.00	2.00/ 0.00	2.30/ 0.00	ns
		XC2V6000	1.92/ 0.50	1.92/ 0.50	2.21/ 0.50	ns
		XC2V8000		2.38/ 0.00	2.60/ 0.00	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. These values are parametrically measured.

Pin Definitions

Table 4 provides a description of each pin type listed in Virtex-II pinout tables.

Table 4: **Virtex-II Pin Definitions**

Pin Name	Direction	Description
User I/O Pins		
IO_LXXY_#	Input/Output/ Bidirectional	All user I/O pins are capable of differential signalling and can implement LVDS, ULVDS, BLVDS, LVPECL, or LDT pairs. Each user I/O is labeled "**IO_LXXY_#**", where: **IO** indicates a user I/O pin. **LXXY** indicates a differential pair, with **XX** a unique pair in the bank and **Y = P/N** for the positive and negative sides of the differential pair. **#** indicates the bank number (0 through 7)
Dual-Function Pins		
IO_LXXY_#/ZZZ		The dual-function pins are labelled "**IO_LXXY_#/ZZZ**", where **ZZZ** can be one of the following pins: Per Bank - **VRP, VRN,** or **VREF** Globally - **GCLKX(S/P), BUSY/DOUT, INIT_B, D0/DIN – D7, RDWR_B,** or **CS_B**
With /ZZZ:		
D0/DIN, D1, D2, D3, D4, D5, D6, D7	Input/Output	• *In* SelectMAP *mode,* D0 through D7 are configuration data pins. These pins become user I/Os after configuration, unless the SelectMAP port is retained. • *In bit-serial modes,* DIN (D0) is the single-data input. This pin becomes a user I/O after configuration.
CS_B	Input	In SelectMAP mode, this is the active-low Chip Select signal. The pin becomes a user I/O after configuration, unless the SelectMAP port is retained.
RDWR_B	Input	In SelectMAP mode, this is the active-low Write Enable signal. The pin becomes a user I/O after configuration, unless the SelectMAP port is retained.
BUSY/DOUT	Output	• *In* SelectMAP *mode,* BUSY controls the rate at which configuration data is loaded. The pin becomes a user I/O after configuration, unless the SelectMAP port is retained. • *In bit-serial modes,* DOUT provides preamble and configuration data to downstream devices in a daisy-chain. The pin becomes a user I/O after configuration.
INIT_B	Bidirectional (open-drain)	When Low, this pin indicates that the configuration memory is being cleared. When held Low, the start of configuration is delayed. During configuration, a Low on this output indicates that a configuration data error has occurred. The pin becomes a user I/O after configuration.
GCLKx (S/P)	Input/Output	These are clock input pins that connect to Global Clock Buffers. These pins become regular user I/Os when not needed for clocks.
VRP	Input	This pin is for the DCI voltage reference resistor of P transistor (per bank).
VRN	Input	This pin is for the DCI voltage reference resistor of N transistor (per bank).
ALT_VRP	Input	This is the alternative pin for the DCI voltage reference resistor of P transistor.
ALT_VRN	Input	This is the alternative pin for the DCI voltage reference resistor of N transistor.
V_{REF}	Input	These are input threshold voltage pins. They become user I/Os when an external threshold voltage is not needed (per bank).
Dedicated Pins(1)		
CCLK	Input/Output	Configuration clock. Output in Master mode or Input in Slave mode.

Table 6: **FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
3	IO_L96N_3	J16		
3	IO_L96P_3	J15		
3	IO_L94N_3	J14		
3	IO_L94P_3	J13		
3	IO_L93N_3/VREF_3	K16	NC	
3	IO_L93P_3	K15	NC	
3	IO_L91N_3	K14	NC	
3	IO_L91P_3	K13	NC	
3	IO_L45N_3/VREF_3	K12	NC	NC
3	IO_L45P_3	L12	NC	NC
3	IO_L43N_3	L16	NC	NC
3	IO_L43P_3	L15	NC	NC
3	IO_L06N_3	L14	NC	
3	IO_L06P_3	L13	NC	
3	IO_L04N_3	M16	NC	
3	IO_L04P_3	M15	NC	
3	IO_L03N_3/VREF_3	M14		
3	IO_L03P_3	M13		
3	IO_L02N_3/VRP_3	N15		
3	IO_L02P_3/VRN_3	N14		
3	IO_L01N_3	N16		
3	IO_L01P_3	P16		
4	IO_L01N_4/BUSY/DOUT(1)	T14		
4	IO_L01P_4/INIT_B	T13		
4	IO_L02N_4/D0/DIN(1)	P13		
4	IO_L02P_4/D1	R13		
4	IO_L03N_4/D2/ALT_VRP_4	N12		
4	IO_L03P_4/D3/ALT_VRN_4	P12		
4	IO_L04N_4/VREF_4	R12	NC	NC
4	IO_L04P_4	T12	NC	NC
4	IO_L05N_4/VRP_4	N11	NC	NC
4	IO_L05P_4/VRN_4	P11	NC	NC

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
7	IO_L21P_7/VREF_7	F3		
7	IO_L21N_7	F2		
7	IO_L19P_7	H6		
7	IO_L19N_7	H7		
7	IO_L06P_7	E1		
7	IO_L06N_7	E2		
7	IO_L04P_7	D1		
7	IO_L04N_7	D2		
7	IO_L03P_7/VREF_7	C1		
7	IO_L03N_7	C2		
7	IO_L02P_7/VRN_7	E3		
7	IO_L02N_7/VRP_7	E4		
7	IO_L01P_7	G5		
7	IO_L01N_7	F4		
0	VCCO_0	J13		
0	VCCO_0	J12		
0	VCCO_0	J11		
0	VCCO_0	H10		
0	VCCO_0	H9		
0	VCCO_0	B10		
0	VCCO_0	B7		
1	VCCO_1	B17		
1	VCCO_1	J16		
1	VCCO_1	J15		
1	VCCO_1	J14		
1	VCCO_1	H18		
1	VCCO_1	H17		
1	VCCO_1	B20		
2	VCCO_2	N18		
2	VCCO_2	M18		
2	VCCO_2	L18		
2	VCCO_2	K25		
2	VCCO_2	K19		
2	VCCO_2	J19		
2	VCCO_2	G25		
3	VCCO_3	Y25		

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
1	IO_L70N_1	B15	NC	
1	IO_L70P_1	C15	NC	
1	IO_L69N_1/VREF_1	E15	NC	
1	IO_L69P_1	F15	NC	
1	IO_L67N_1	G15	NC	
1	IO_L67P_1	H15	NC	
1	IO_L54N_1	B16		
1	IO_L54P_1	C16		
1	IO_L52N_1	D16		
1	IO_L52P_1	E16		
1	IO_L51N_1/VREF_1	F16		
1	IO_L51P_1	G16		
1	IO_L49N_1	A17		
1	IO_L49P_1	A19		
1	IO_L24N_1	B17		
1	IO_L24P_1	B18		
1	IO_L22N_1	C17		
1	IO_L22P_1	D17		
1	IO_L21N_1/VREF_1	F17		
1	IO_L21P_1	E17		
1	IO_L19N_1	A20		
1	IO_L19P_1	A21		
1	IO_L06N_1	B19		
1	IO_L06P_1	B20		
1	IO_L05N_1	C18		
1	IO_L05P_1	D18		
1	IO_L04N_1	C20		
1	IO_L04P_1/VREF_1	D20		
1	IO_L03N_1/VRP_1	D19		
1	IO_L03P_1/VRN_1	E19		
1	IO_L02N_1	E18		
1	IO_L02P_1	F18		
1	IO_L01N_1	H16		
1	IO_L01P_1	G17		
2	IO_L01N_2	D22		

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
4	IO_L91P_4	AB14		
4	IO_L92N_4	V14		
4	IO_L92P_4	Y14		
4	IO_L93N_4	AB13		
4	IO_L93P_4	AC13		
4	IO_L94N_4/VREF_4	Y13		
4	IO_L94P_4	AA13		
4	IO_L95N_4/GCLK3S	V13		
4	IO_L95P_4/GCLK2P	W13		
4	IO_L96N_4/GCLK1S	U14		
4	IO_L96P_4/GCLK0P	U13		
5	IO_L96N_5/GCLK7S	AD12		
5	IO_L96P_5/GCLK6P	AD11		
5	IO_L95N_5/GCLK5S	AC12		
5	IO_L95P_5/GCLK4P	AB12		
5	IO_L94N_5	AA12		
5	IO_L94P_5/VREF_5	Y12		
5	IO_L93N_5	W12		
5	IO_L93P_5	V12		
5	IO_L92N_5	U12		
5	IO_L92P_5	U11		
5	IO_L91N_5	AB11		
5	IO_L91P_5/VREF_5	AA11		
5	IO_L73N_5	Y11	NC	NC
5	IO_L73P_5	V11	NC	NC
5	IO_L72N_5	AD10	NC	
5	IO_L72P_5	AD9	NC	
5	IO_L70N_5	AC10	NC	
5	IO_L70P_5	AB10	NC	
5	IO_L69N_5/VREF_5	Y10	NC	
5	IO_L69P_5	W10	NC	
5	IO_L67N_5	V10	NC	
5	IO_L67P_5	U10	NC	
5	IO_L54N_5	AC9		
5	IO_L54P_5	AB9		

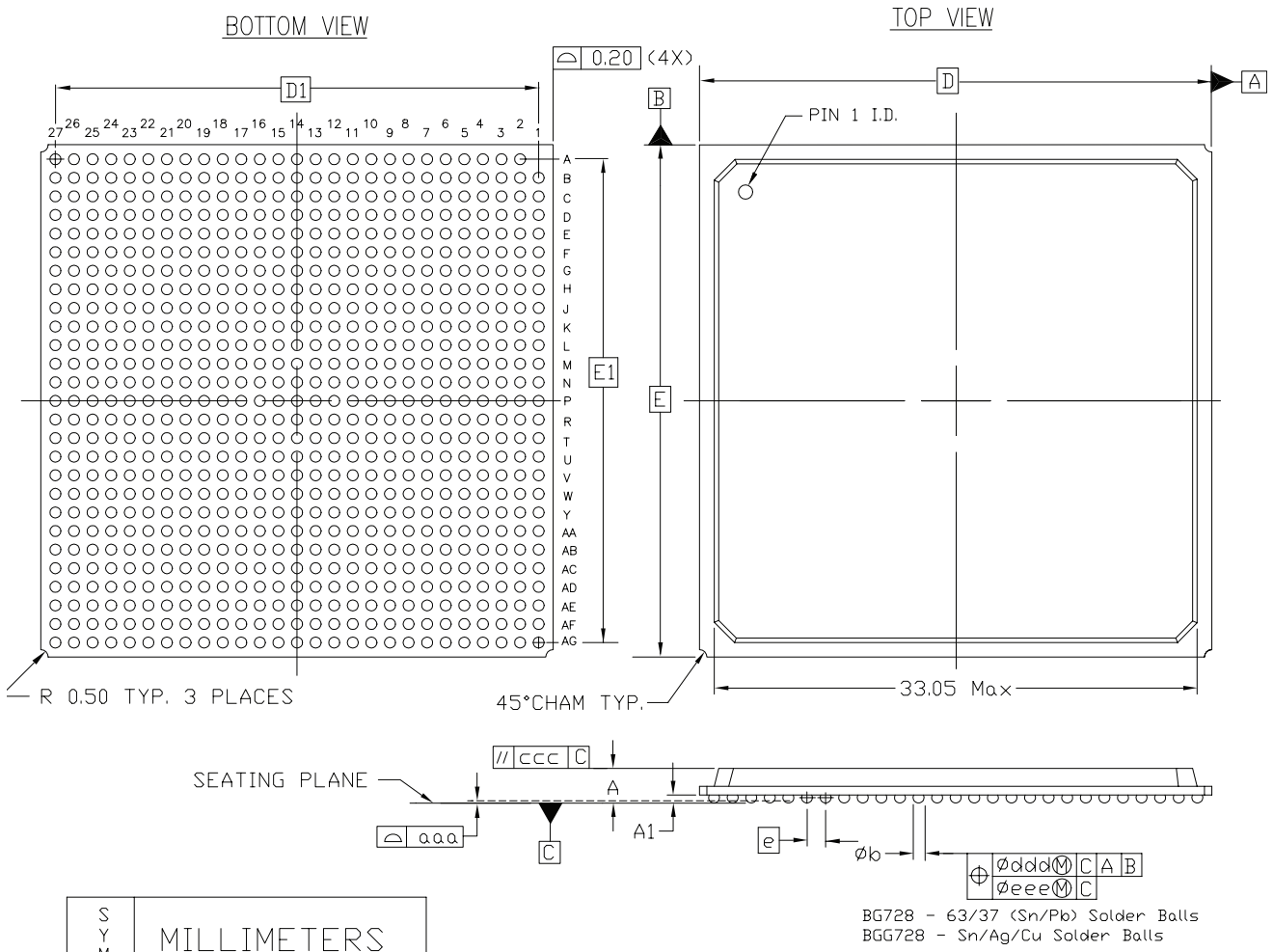
Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
1	IO_L94N_1	C15
1	IO_L94P_1/VREF_1	D15
1	IO_L93N_1	E15
1	IO_L93P_1	F15
1	IO_L92N_1	G15
1	IO_L92P_1	H15
1	IO_L91N_1	J15
1	IO_L91P_1/VREF_1	J16
1	IO_L78N_1	A16
1	IO_L78P_1	B16
1	IO_L76N_1	D16
1	IO_L76P_1	E16
1	IO_L75N_1/VREF_1	F16
1	IO_L75P_1	F17
1	IO_L73N_1	H16
1	IO_L73P_1	H17
1	IO_L72N_1	A17
1	IO_L72P_1	B17
1	IO_L70N_1	C17
1	IO_L70P_1	D17
1	IO_L69N_1/VREF_1	G18
1	IO_L69P_1	G17
1	IO_L67N_1	A18
1	IO_L67P_1	B18
1	IO_L54N_1	C18
1	IO_L54P_1	D18
1	IO_L52N_1	E18
1	IO_L52P_1	F18
1	IO_L51N_1/VREF_1	H19
1	IO_L51P_1	H18
1	IO_L49N_1	A19
1	IO_L49P_1	A20
1	IO_L30N_1	B19
1	IO_L30P_1	C19
1	IO_L28N_1	D19
1	IO_L28P_1	E19

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
1	VCCO_1	G16
1	VCCO_1	D21
1	VCCO_1	C16
2	VCCO_2	N18
2	VCCO_2	M25
2	VCCO_2	M21
2	VCCO_2	M18
2	VCCO_2	L19
2	VCCO_2	L18
2	VCCO_2	K19
2	VCCO_2	G24
3	VCCO_3	AA24
3	VCCO_3	V19
3	VCCO_3	U19
3	VCCO_3	U18
3	VCCO_3	T25
3	VCCO_3	T21
3	VCCO_3	T18
3	VCCO_3	R18
4	VCCO_4	AE16
4	VCCO_4	AD21
4	VCCO_4	AA16
4	VCCO_4	W18
4	VCCO_4	W17
4	VCCO_4	V17
4	VCCO_4	V16
4	VCCO_4	V15
5	VCCO_5	AE12
5	VCCO_5	AD7
5	VCCO_5	AA12
5	VCCO_5	W11
5	VCCO_5	W10
5	VCCO_5	V13
5	VCCO_5	V12
5	VCCO_5	V11
6	VCCO_6	AA4

BG728/BGG728 Standard BGA Package Specifications (1.27mm pitch)



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	2.33	2.60
A_1	0.50	0.60	0.70
D/E	35.00 BSC		
D_1/E_1	33.02 REF		
e	1.27BSC		
øb	0.60	0.75	0.90
aaa	---	---	0.20
ccc	---	---	0.35
ddd	---	---	0.30
eee	---	---	0.15
M	27		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-BAR-1
4. NO SOLDER BALL AND LAND ON A1.

728-BALL MOLDED BGA (BG728/BGG728)

Figure 6: **BG728/BGG728 Standard BGA Package Specifications**

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
NA	GND	T13		
NA	GND	T12		
NA	GND	R19		
NA	GND	R18		
NA	GND	R17		
NA	GND	R16		
NA	GND	R15		
NA	GND	R14		
NA	GND	R13		
NA	GND	R12		
NA	GND	P24		
NA	GND	P19		
NA	GND	P18		
NA	GND	P17		
NA	GND	P16		
NA	GND	P15		
NA	GND	P14		
NA	GND	P13		
NA	GND	P12		
NA	GND	P7		
NA	GND	N19		
NA	GND	N18		
NA	GND	N17		
NA	GND	N16		
NA	GND	N15		
NA	GND	N14		
NA	GND	N13		
NA	GND	N12		
NA	GND	M26		
NA	GND	M19		
NA	GND	M18		
NA	GND	M17		
NA	GND	M16		
NA	GND	M15		
NA	GND	M14		
NA	GND	M13		
NA	GND	M12		

device shown in the No Connect column. Following this table are the FF1152 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
0	IO_L01N_0	D29	
0	IO_L01P_0	C29	
0	IO_L02N_0	H26	
0	IO_L02P_0	G26	
0	IO_L03N_0/VRP_0	E28	
0	IO_L03P_0/VRN_0	E27	
0	IO_L04N_0/VREF_0	F25	
0	IO_L04P_0	F26	
0	IO_L05N_0	H25	
0	IO_L05P_0	H24	
0	IO_L06N_0	E26	
0	IO_L06P_0	F27	
0	IO_L19N_0	B32	
0	IO_L19P_0	C33	
0	IO_L20N_0	J24	
0	IO_L20P_0	J23	
0	IO_L21N_0	C27	
0	IO_L21P_0/VREF_0	C28	
0	IO_L22N_0	B30	
0	IO_L22P_0	B31	
0	IO_L23N_0	K23	
0	IO_L23P_0	K22	
0	IO_L24N_0	C26	
0	IO_L24P_0	D27	
0	IO_L25N_0	A30	
0	IO_L25P_0	A31	
0	IO_L26N_0	G24	
0	IO_L26P_0	G25	
0	IO_L27N_0	E25	
0	IO_L27P_0/VREF_0	E24	
0	IO_L28N_0	D25	
0	IO_L28P_0	D26	
0	IO_L29N_0	H23	
0	IO_L29P_0	H22	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
1	IO_L22P_1	A5	
1	IO_L21N_1/VREF_1	F10	
1	IO_L21P_1	G9	
1	IO_L20N_1	J12	
1	IO_L20P_1	J11	
1	IO_L19N_1	B4	
1	IO_L19P_1	B5	
1	IO_L06N_1	D6	
1	IO_L06P_1	C6	
1	IO_L05N_1	H11	
1	IO_L05P_1	J10	
1	IO_L04N_1	D8	
1	IO_L04P_1/VREF_1	E7	
1	IO_L03N_1/VRP_1	F9	
1	IO_L03P_1/VRN_1	F8	
1	IO_L02N_1	H10	
1	IO_L02P_1	H9	
1	IO_L01N_1	C2	
1	IO_L01P_1	B3	
2	IO_L01N_2	E2	
2	IO_L01P_2	D2	
2	IO_L02N_2/VRP_2	K11	
2	IO_L02P_2/VRN_2	K10	
2	IO_L03N_2	F5	
2	IO_L03P_2/VREF_2	G5	
2	IO_L04N_2	E3	
2	IO_L04P_2	D3	
2	IO_L05N_2	J9	
2	IO_L05P_2	K9	
2	IO_L06N_2	F4	
2	IO_L06P_2	E4	
2	IO_L19N_2	E1	
2	IO_L19P_2	D1	
2	IO_L20N_2	J8	
2	IO_L20P_2	K8	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
6	IO_L47N_6	AJ39		
6	IO_L48P_6	AG35		
6	IO_L48N_6	AH35		
6	IO_L49P_6	AG32		
6	IO_L49N_6	AF32		
6	IO_L50P_6	AH37		
6	IO_L50N_6	AG37		
6	IO_L51P_6	AD29		
6	IO_L51N_6/VREF_6	AE29		
6	IO_L52P_6	AD28		
6	IO_L52N_6	AC28		
6	IO_L53P_6	AH38		
6	IO_L53N_6	AG38		
6	IO_L54P_6	AF34		
6	IO_L54N_6	AG34		
6	IO_L55P_6	AE32		
6	IO_L55N_6	AD32		
6	IO_L56P_6	AH39		
6	IO_L56N_6	AG39		
6	IO_L57P_6	AE33		
6	IO_L57N_6/VREF_6	AF33		
6	IO_L58P_6	AD30		
6	IO_L58N_6	AC30		
6	IO_L59P_6	AF37		
6	IO_L59N_6	AE37		
6	IO_L60P_6	AF36		
6	IO_L60N_6	AG36		
6	IO_L67P_6	AD31		
6	IO_L67N_6	AC31		
6	IO_L68P_6	AE34		
6	IO_L68N_6	AD34		
6	IO_L69P_6	AD35		
6	IO_L69N_6/VREF_6	AE35		
6	IO_L70P_6	AB28		
6	IO_L70N_6	AA28		
6	IO_L71P_6	AF39		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
6	VCCO_6	AG33		
6	VCCO_6	AF38		
6	VCCO_6	AF27		
6	VCCO_6	AE31		
6	VCCO_6	AE27		
6	VCCO_6	AE26		
6	VCCO_6	AD27		
6	VCCO_6	AD26		
6	VCCO_6	AC29		
6	VCCO_6	AC27		
6	VCCO_6	AC26		
6	VCCO_6	AB37		
6	VCCO_6	AB27		
6	VCCO_6	AB26		
6	VCCO_6	AA27		
6	VCCO_6	AA26		
7	VCCO_7	W27		
7	VCCO_7	W26		
7	VCCO_7	V37		
7	VCCO_7	V27		
7	VCCO_7	V26		
7	VCCO_7	U29		
7	VCCO_7	U27		
7	VCCO_7	U26		
7	VCCO_7	T27		
7	VCCO_7	T26		
7	VCCO_7	R31		
7	VCCO_7	R27		
7	VCCO_7	R26		
7	VCCO_7	P38		
7	VCCO_7	P27		
7	VCCO_7	N33		
7	VCCO_7	L35		
NA	CCLK	AT5		
NA	PROG_B	H31		

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
2	IO_L70N_2	K1	
2	IO_L70P_2	L1	
2	IO_L71N_2	N9	
2	IO_L71P_2	P9	
2	IO_L72N_2	N5	
2	IO_L72P_2	P5	
2	IO_L73N_2	M3	
2	IO_L73P_2	N3	
2	IO_L74N_2	R8	
2	IO_L74P_2	R9	
2	IO_L75N_2	M2	
2	IO_L75P_2/VREF_2	N2	
2	IO_L76N_2	M1	
2	IO_L76P_2	N1	
2	IO_L77N_2	P7	
2	IO_L77P_2	R7	
2	IO_L78N_2	N4	
2	IO_L78P_2	P4	
2	IO_L91N_2	T8	
2	IO_L91P_2	T9	
2	IO_L92N_2	P6	
2	IO_L92P_2	R6	
2	IO_L93N_2	P2	
2	IO_L93P_2/VREF_2	R2	
2	IO_L94N_2	R5	
2	IO_L94P_2	T5	
2	IO_L95N_2	P1	
2	IO_L95P_2	R1	
2	IO_L96N_2	R4	
2	IO_L96P_2	R3	
3	IO_L96N_3	T6	
3	IO_L96P_3	U5	
3	IO_L95N_3	U6	
3	IO_L95P_3	V6	
3	IO_L94N_3	T3	
3	IO_L94P_3	U3	
3	IO_L93N_3/VREF_3	U1	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
3	IO_L50P_3	AB3	
3	IO_L49N_3	AB5	
3	IO_L49P_3	AC5	
3	IO_L48N_3	W9	
3	IO_L48P_3	Y9	
3	IO_L47N_3	AC1	
3	IO_L47P_3	AD1	
3	IO_L46N_3	AC3	
3	IO_L46P_3	AD3	
3	IO_L45N_3/VREF_3	Y8	
3	IO_L45P_3	AA8	
3	IO_L44N_3	AC2	
3	IO_L44P_3	AE2	
3	IO_L43N_3	AB7	
3	IO_L43P_3	AC7	
3	IO_L27N_3/VREF_3	Y10	NC
3	IO_L27P_3	AA10	NC
3	IO_L25N_3	AE1	NC
3	IO_L25P_3	AF1	NC
3	IO_L24N_3	AF2	
3	IO_L24P_3	AG2	
3	IO_L23N_3	AA9	
3	IO_L23P_3	AB9	
3	IO_L22N_3	AD4	
3	IO_L22P_3	AE4	
3	IO_L21N_3/VREF_3	AD5	
3	IO_L21P_3	AE5	
3	IO_L20N_3	AB8	
3	IO_L20P_3	AC8	
3	IO_L19N_3	AG1	
3	IO_L19P_3	AH1	
3	IO_L06N_3	AF4	
3	IO_L06P_3	AG4	
3	IO_L05N_3	AB10	
3	IO_L05P_3	AB11	
3	IO_L04N_3	AF3	
3	IO_L04P_3	AG3	
3	IO_L03N_3/VREF_3	AD6	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
5	IO_L73P_5	AJ20	
5	IO_L72N_5	AG18	
5	IO_L72P_5	AG19	
5	IO_L71N_5	AF18	
5	IO_L71P_5	AF19	
5	IO_L70N_5	AK20	
5	IO_L70P_5	AK21	
5	IO_L69N_5/VREF_5	AH20	
5	IO_L69P_5	AH21	
5	IO_L68N_5	AD19	
5	IO_L68P_5	AD20	
5	IO_L67N_5	AL21	
5	IO_L67P_5	AL22	
5	IO_L54N_5	AG20	
5	IO_L54P_5	AG21	
5	IO_L53N_5	AB19	
5	IO_L53P_5	AB20	
5	IO_L52N_5	AJ21	
5	IO_L52P_5	AJ22	
5	IO_L51N_5/VREF_5	AF20	
5	IO_L51P_5	AF21	
5	IO_L50N_5	AE20	
5	IO_L50P_5	AE21	
5	IO_L49N_5	AK22	
5	IO_L49P_5	AK23	
5	IO_L30N_5	AJ23	NC
5	IO_L30P_5	AJ24	NC
5	IO_L29N_5	AC20	NC
5	IO_L29P_5	AC21	NC
5	IO_L28N_5	AL23	NC
5	IO_L28P_5	AL24	NC
5	IO_L27N_5/VREF_5	AL25	NC
5	IO_L27P_5	AL26	NC
5	IO_L26N_5	AD21	NC
5	IO_L26P_5	AD22	NC
5	IO_L25N_5	AH23	NC
5	IO_L25P_5	AH24	NC
5	IO_L24N_5	AG22	