



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	64
Number of Logic Elements/Cells	-
Total RAM Bits	73728
Number of I/O	88
Number of Gates	40000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-TFBGA, CSPBGA
Supplier Device Package	144-LCSBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v40-6csg144c

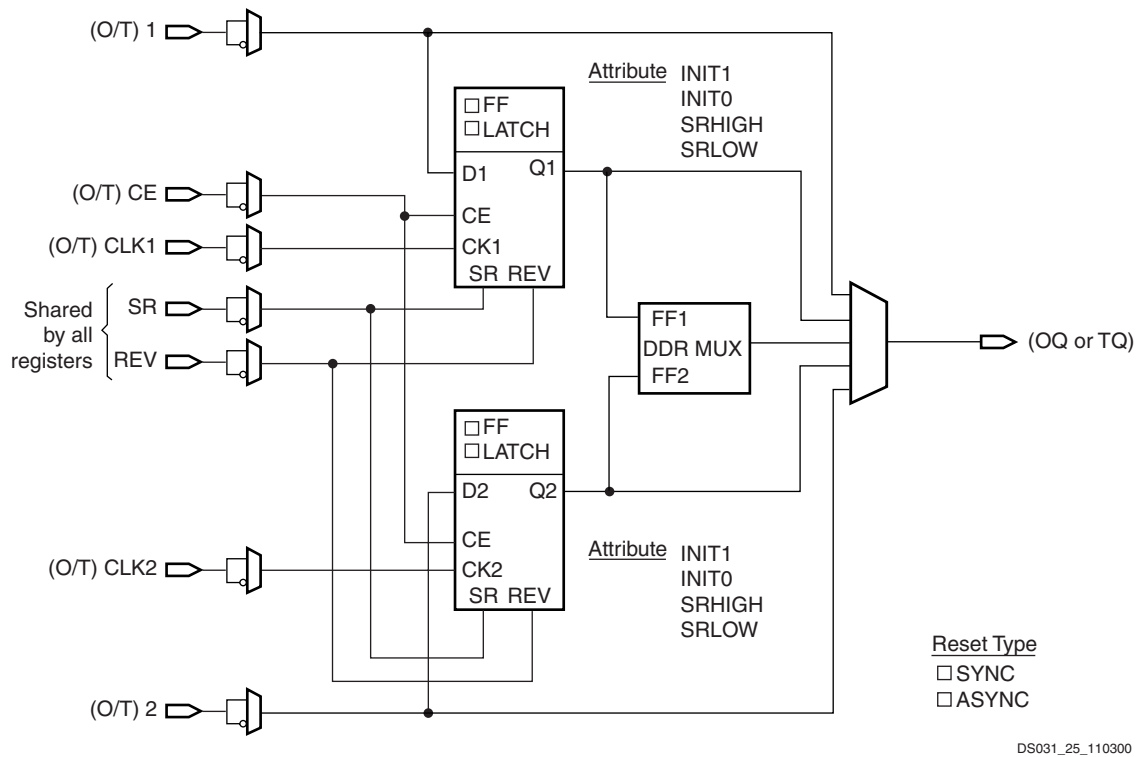


Figure 4: Register / Latch Configuration in an IOB Block

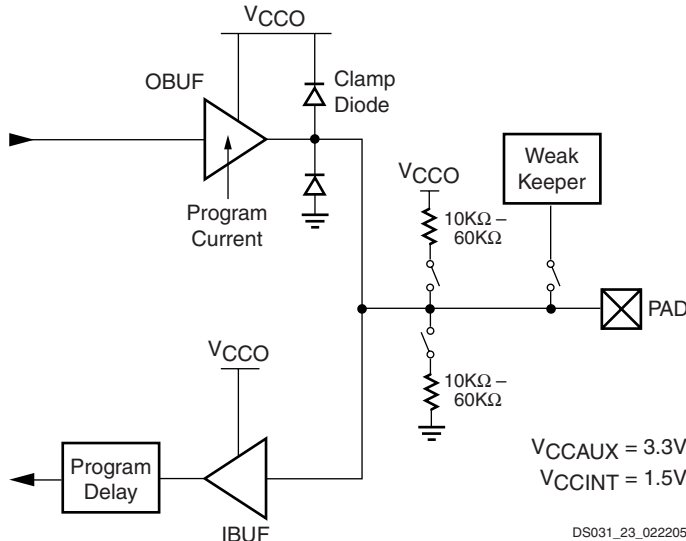


Figure 5: LVTTL, LVCMOS or PCI Select/O-Ultra Standards

Input/Output Individual Options

Each device pad has optional pull-up and pull-down in all SelectI/O-Ultra configurations. Each device pad has optional weak-keeper in LVTTTL, LVCMOS, and PCI SelectI/O-Ultra configurations, as illustrated in **Figure 5**. Values of the optional pull-up and pull-down resistors are in the range 10 - 60 K Ω , which is the specification for V_{CCO} when operating at 3.3V (from 3.0 to 3.6V only). The clamp diode is always present, even when power is not.

The optional weak-keeper circuit is connected to each user I/O pad. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low. If the pin is connected to a multiple-source signal, the weak-keeper holds the signal in its last state if all drivers are disabled. Maintaining a valid logic level in this way eliminates bus chatter. An enabled pull-up or pull-down overrides the weak-keeper circuit.

LVTTL sinks and sources current up to 24 mA. The current is programmable for LVTTL and LVCMOS SelectI/O-Ultra standards (see [Table 4](#)). Drive-strength and slew-rate controls for each output driver, minimize bus transients. For LVDCI and LVDCI_DV2 standards, drive strength and slew-rate controls are not available.

Shift Registers

Each function generator can also be configured as a 16-bit shift register. The write operation is synchronous with a clock input (CLK) and an optional clock enable, as shown in **Figure 21**. A dynamic read access is performed through the 4-bit address bus, A[3:0]. The configurable 16-bit shift register cannot be set or reset. The read is asynchronous, however the storage element or flip-flop is available to implement a synchronous read. The storage element should always be used with a constant address. For example, when building an 8-bit shift register and configuring the addresses to point to the 7th bit, the 8th bit can be the flip-flop. The overall system performance is improved by using the superior clock-to-out of the flip-flops.

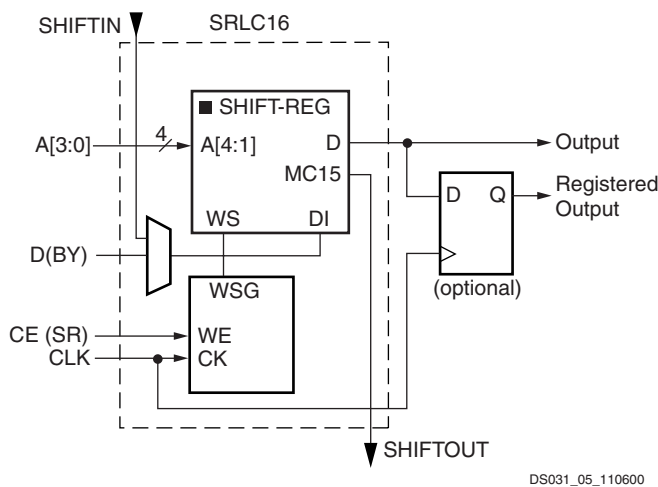


Figure 21: Shift Register Configurations

An additional dedicated connection between shift registers allows connecting the last bit of one shift register to the first bit of the next, without using the ordinary LUT output. (See **Figure 22**.) Longer shift registers can be built with dynamic access to any bit in the chain. The shift register chaining and the MUXF5, MUXF6, and MUXF7 multiplexers allow up to a 128-bit shift register with addressable access to be implemented in one CLB.

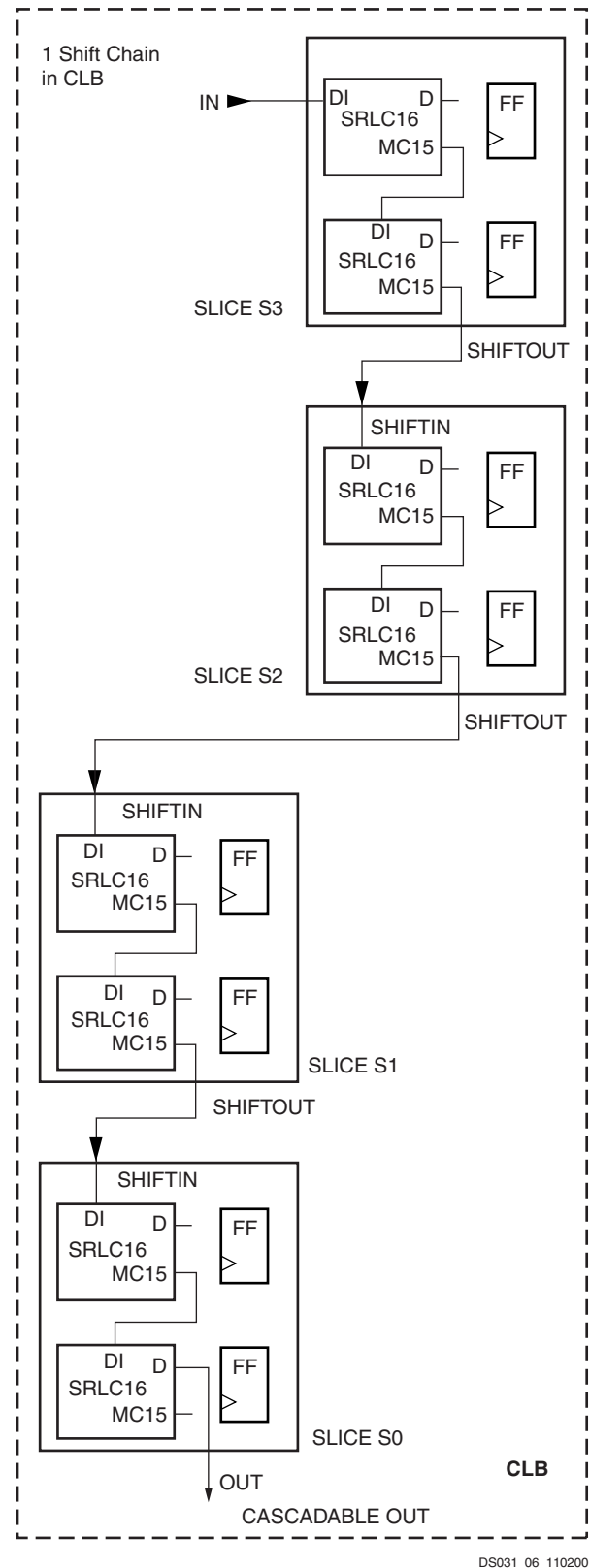


Figure 22: Cascadable Shift Register

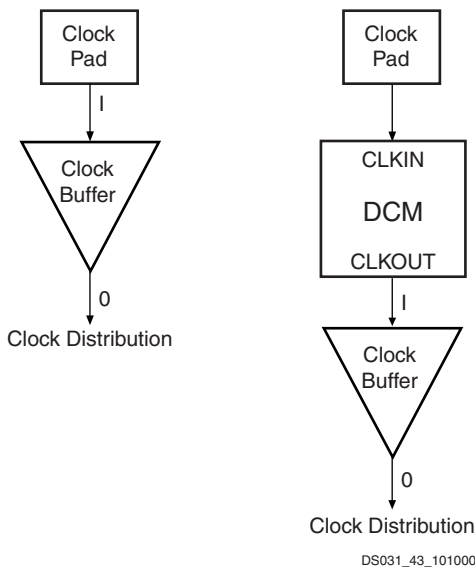


Figure 39: Virtex-II Clock Distribution Configurations

Global clock buffers are used to distribute the clock to some or all synchronous logic elements (such as registers in CLBs and IOBs, and SelectRAM blocks).

Eight global clocks can be used in each quadrant of the Virtex-II device. Designers should consider the clock distribution detail of the device prior to pin-locking and floorplanning (see the Virtex-II *User Guide*).

Figure 40 shows clock distribution in Virtex-II devices.

In each quadrant, up to eight clocks are organized in clock rows. A clock row supports up to 16 CLB rows (eight up and eight down). For the largest devices a new clock row is added, as necessary.

To reduce power consumption, any unused clock branches remain static.

Global clocks are driven by dedicated clock buffers (BUFG), which can also be used to gate the clock (BUFGCE) or to multiplex between two independent clock inputs (BUFGMUX).

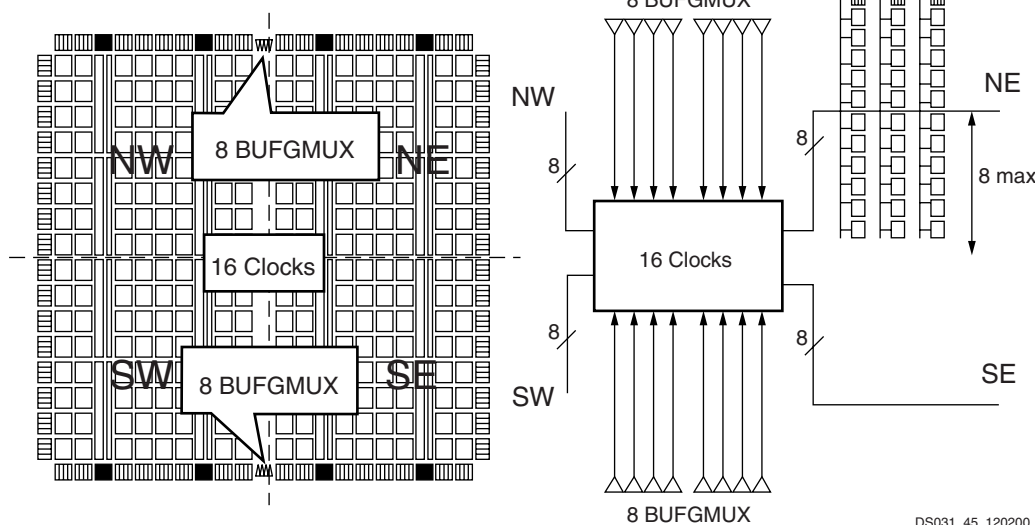


Figure 40: Virtex-II Clock Distribution

The most common configuration option of this element is as a buffer. A BUFG function in this (global buffer) mode, is shown in Figure 41.

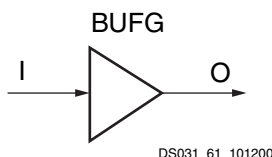


Figure 41: Virtex-II BUFG Function

The Virtex-II global clock buffer BUFG can also be configured as a clock enable/disable circuit (Figure 42), as well as a two-input clock multiplexer (Figure 43). A functional description of these two options is provided below. Each of

them can be used in either of two modes, selected by configuration: rising clock edge or falling clock edge.

This section describes the rising clock edge option. For the opposite option, falling clock edge, just change all "rising" references to "falling" and all "High" references to "Low", except for the description of the CE or S levels. The rising clock edge option uses the BUFGCE and BUFGMUX primitives. The falling clock edge option uses the BUFGCE_1 and BUFGMUX_1 primitives.

BUFGCE

If the CE input is active (High) prior to the incoming rising clock edge, this Low-to-High-to-Low clock pulse passes through the clock buffer. Any level change of CE during the incoming clock High time has no effect.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *Without* DCM

Table 35: Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *Without* DCM

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
LVTTL Global Clock Input to Output Delay using Output flip-flop, 12 mA, Fast Slew Rate, <i>without</i> DCM. For data <i>output</i> with different standards, adjust the delays with the values shown in <i>IOB Output Switching Characteristics Standard Adjustments</i> , page 14.						
Global Clock and OFF without DCM	T _{ICKOF}	XC2V40	3.46	3.58	3.69	ns
		XC2V80	3.62	3.58	3.69	ns
		XC2V250	3.79	3.88	4.47	ns
		XC2V500	3.85	3.88	4.47	ns
		XC2V1000	4.02	4.28	4.62	ns
		XC2V1500	4.16	4.28	4.62	ns
		XC2V2000	4.30	4.43	5.10	ns
		XC2V3000	4.49	4.64	5.34	ns
		XC2V4000	4.82	4.99	5.74	ns
		XC2V6000	5.19	5.38	5.93	ns
		XC2V8000		6.09	7.00	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with test setup shown in [Figure 1](#). For other I/O standards, see [Table 19](#).

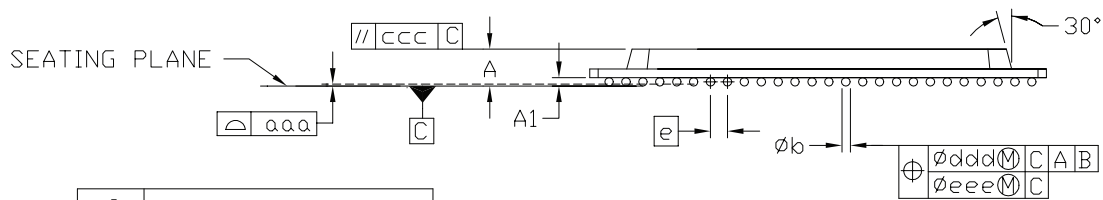
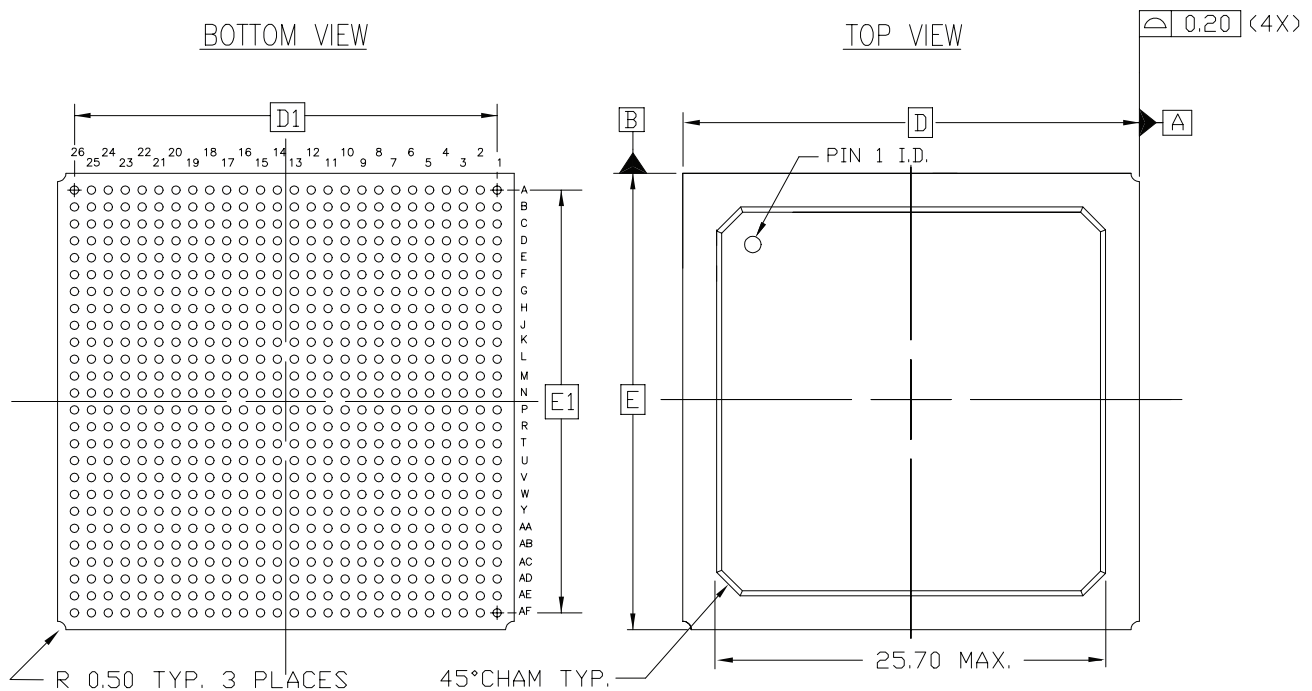
Table 6: FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
7	IO_L45N_7	F5	NC	NC
7	IO_L43P_7	F1	NC	NC
7	IO_L43N_7	F2	NC	NC
7	IO_L06P_7	F3	NC	
7	IO_L06N_7	F4	NC	
7	IO_L04P_7	E1	NC	
7	IO_L04N_7	E2	NC	
7	IO_L03P_7/VREF_7	E3		
7	IO_L03N_7	E4		
7	IO_L02P_7/VRN_7	D2		
7	IO_L02N_7/VRP_7	D3		
7	IO_L01P_7	D1		
7	IO_L01N_7	C1		
0	VCCO_0	F8		
0	VCCO_0	F7		
0	VCCO_0	E8		
1	VCCO_1	F10		
1	VCCO_1	F9		
1	VCCO_1	E9		
2	VCCO_2	H12		
2	VCCO_2	H11		
2	VCCO_2	G11		
3	VCCO_3	K11		
3	VCCO_3	J12		
3	VCCO_3	J11		
4	VCCO_4	M9		
4	VCCO_4	L10		
4	VCCO_4	L9		
5	VCCO_5	M8		
5	VCCO_5	L8		
5	VCCO_5	L7		
6	VCCO_6	K6		
6	VCCO_6	J6		

Table 8: FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
2	IO_L96P_2	N23		
3	IO_L96N_3	N26		
3	IO_L96P_3	P26		
3	IO_L94N_3	P23		
3	IO_L94P_3	P22		
3	IO_L93N_3/VREF_3	P19		
3	IO_L93P_3	N19		
3	IO_L91N_3	P21		
3	IO_L91P_3	P20		
3	IO_L78N_3	R26	NC	
3	IO_L78P_3	R25	NC	
3	IO_L76N_3	R20	NC	
3	IO_L76P_3	R19	NC	
3	IO_L75N_3/VREF_3	R24	NC	
3	IO_L75P_3	R23	NC	
3	IO_L73N_3	R22	NC	
3	IO_L73P_3	R21	NC	
3	IO_L72N_3	T26		
3	IO_L72P_3	T25		
3	IO_L70N_3	T20		
3	IO_L70P_3	T19		
3	IO_L69N_3/VREF_3	T24		
3	IO_L69P_3	T23		
3	IO_L67N_3	T22		
3	IO_L67P_3	T21		
3	IO_L54N_3	U26		
3	IO_L54P_3	V26		
3	IO_L52N_3	U24		
3	IO_L52P_3	U23		
3	IO_L51N_3/VREF_3	U22		
3	IO_L51P_3	U21		
3	IO_L49N_3	V25		
3	IO_L49P_3	V24		
3	IO_L48N_3	V23		
3	IO_L48P_3	V22		
3	IO_L46N_3	W26		

FG676/FGG676 Fine-Pitch BGA Package Specifications (1.00mm pitch)



FG676 - 63/37 (Sn/Pb) Solder Balls
FGG676 - Sn/Ag/Cu Solder Balls

SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A	$\sim$	2.25	2.60
A ₁	0.40	0.50	0.60
D/E	27.00 BSC		
D ₁ /E ₁	25.00 REF		
e	1.00 BSC		
øb	0.50	0.60	0.70
aaa	$\sim$	$\sim$	0.20
ccc	$\sim$	$\sim$	0.35
ddd	$\sim$	$\sim$	0.30
eee	$\sim$	$\sim$	0.10
M	26		

NOTES:

- ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
- SYMBOL 'M' IS THE BALL MATRIX SIZE.
- CONFORMS TO JEDEC MS-034-AAL-1

676-BALL FINE PITCH BGA (FG676/FGG676)

Figure 4: FG676/FGG676 Fine-Pitch BGA Package Specifications

Table 9: BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
0	IO_L69P_0/VREF_0	B9	NC	
0	IO_L70N_0	F10	NC	
0	IO_L70P_0	E10	NC	
0	IO_L72N_0	A10	NC	
0	IO_L72P_0	A11	NC	
0	IO_L73N_0	C10	NC	NC
0	IO_L73P_0	B10	NC	NC
0	IO_L91N_0/VREF_0	D11		
0	IO_L91P_0	C11		
0	IO_L92N_0	G11		
0	IO_L92P_0	E11		
0	IO_L93N_0	C12		
0	IO_L93P_0	B12		
0	IO_L94N_0/VREF_0	E12		
0	IO_L94P_0	D12		
0	IO_L95N_0/GCLK7P	G12		
0	IO_L95P_0/GCLK6S	F12		
0	IO_L96N_0/GCLK5P	H11		
0	IO_L96P_0/GCLK4S	H12		
1	IO_L96N_1/GCLK3P	A13		
1	IO_L96P_1/GCLK2S	A14		
1	IO_L95N_1/GCLK1P	B13		
1	IO_L95P_1/GCLK0S	C13		
1	IO_L94N_1	D13		
1	IO_L94P_1/VREF_1	E13		
1	IO_L93N_1	F13		
1	IO_L93P_1	G13		
1	IO_L92N_1	H13		
1	IO_L92P_1	H14		
1	IO_L91N_1	C14		
1	IO_L91P_1/VREF_1	D14		
1	IO_L73N_1	E14	NC	NC
1	IO_L73P_1	G14	NC	NC
1	IO_L72N_1	A15	NC	
1	IO_L72P_1	A16	NC	

Table 9: BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
2	IO_L01P_2	D23		
2	IO_L02N_2/VRP_2	E21		
2	IO_L02P_2/VRN_2	E22		
2	IO_L03N_2	F21		
2	IO_L03P_2/VREF_2	F20		
2	IO_L04N_2	G20		
2	IO_L04P_2	G19		
2	IO_L06N_2	H18		
2	IO_L06P_2	J17		
2	IO_L19N_2	D24		
2	IO_L19P_2	E23		
2	IO_L21N_2	E24		
2	IO_L21P_2/VREF_2	F24		
2	IO_L22N_2	F23		
2	IO_L22P_2	G23		
2	IO_L24N_2	G21		
2	IO_L24P_2	G22		
2	IO_L43N_2	H19		
2	IO_L43P_2	H20		
2	IO_L45N_2	J18		
2	IO_L45P_2/VREF_2	J19		
2	IO_L46N_2	K17		
2	IO_L46P_2	K18		
2	IO_L48N_2	H23		
2	IO_L48P_2	H24		
2	IO_L49N_2	H21		
2	IO_L49P_2	H22		
2	IO_L51N_2	J24		
2	IO_L51P_2/VREF_2	K24		
2	IO_L52N_2	J22		
2	IO_L52P_2	J23		
2	IO_L54N_2	J20		
2	IO_L54P_2	J21		
2	IO_L67N_2	K19	NC	
2	IO_L67P_2	K20	NC	
2	IO_L69N_2	L17	NC	

Table 10: BG728 BGA — XC2V3000

Bank	Pin Description	Pin Number
3	IO_L19N_3	AB26
3	IO_L19P_3	AB25
3	IO_L06N_3	AB24
3	IO_L06P_3	AB23
3	IO_L04N_3	AC27
3	IO_L04P_3	AC26
3	IO_L03N_3/VREF_3	AC25
3	IO_L03P_3	AC24
3	IO_L02N_3/VRP_3	AD27
3	IO_L02P_3/VRN_3	AE27
3	IO_L01N_3	AD26
3	IO_L01P_3	AD25
4	IO_L01N_4/BUSY/DOOUT ⁽¹⁾	AF25
4	IO_L01P_4/INIT_B	AG25
4	IO_L02N_4/D0/DIN ⁽¹⁾	AF24
4	IO_L02P_4/D1	AG24
4	IO_L03N_4/D2/ALT_VRP_4	AD23
4	IO_L03P_4/D3/ALT_VRN_4	AE23
4	IO_L04N_4/VREF_4	AF23
4	IO_L04P_4	AG23
4	IO_L05N_4/VRP_4	AD22
4	IO_L05P_4/VRN_4	AE22
4	IO_L06N_4	AF22
4	IO_L06P_4	AG22
4	IO_L19N_4	AC21
4	IO_L19P_4	AB21
4	IO_L21N_4	AE21
4	IO_L21P_4/VREF_4	AE20
4	IO_L22N_4	AF21
4	IO_L22P_4	AG21
4	IO_L24N_4	AB20
4	IO_L24P_4	AA20
4	IO_L25N_4	AC20
4	IO_L25P_4	AD20
4	IO_L27N_4	AG20

Table 11: FF896 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
4	IO_L73P_4	AJ12	NC	NC
4	IO_L74N_4	AE13	NC	NC
4	IO_L74P_4	AE14	NC	NC
4	IO_L75N_4	AF13	NC	NC
4	IO_L75P_4/VREF_4	AG13	NC	NC
4	IO_L76N_4	AK13	NC	NC
4	IO_L76P_4	AK12	NC	NC
4	IO_L77N_4	AB14	NC	NC
4	IO_L77P_4	AB15	NC	NC
4	IO_L78N_4	AF15	NC	NC
4	IO_L78P_4	AF14	NC	NC
4	IO_L91N_4/VREF_4	AJ14		
4	IO_L91P_4	AJ15		
4	IO_L92N_4	AC14		
4	IO_L92P_4	AC15		
4	IO_L93N_4	AG15		
4	IO_L93P_4	AG14		
4	IO_L94N_4/VREF_4	AK14		
4	IO_L94P_4	AK15		
4	IO_L95N_4/GCLK3S	AD15		
4	IO_L95P_4/GCLK2P	AE15		
4	IO_L96N_4/GCLK1S	AH14		
4	IO_L96P_4/GCLK0P	AH15		
5	IO_L96N_5/GCLK7S	AH16		
5	IO_L96P_5/GCLK6P	AH17		
5	IO_L95N_5/GCLK5S	AE16		
5	IO_L95P_5/GCLK4P	AD16		
5	IO_L94N_5	AJ16		
5	IO_L94P_5/VREF_5	AJ17		
5	IO_L93N_5	AG17		
5	IO_L93P_5	AG16		
5	IO_L92N_5	AC16		
5	IO_L92P_5	AC17		
5	IO_L91N_5	AK17		
5	IO_L91P_5/VREF_5	AK18		
5	IO_L78N_5	AF17	NC	NC

Table 11: FF896 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
5	IO_L23N_5	AD20		
5	IO_L23P_5	AD21		
5	IO_L22N_5	AK25		
5	IO_L22P_5	AK24		
5	IO_L21N_5/VREF_5	AH24		
5	IO_L21P_5	AH25		
5	IO_L20N_5	AE21		
5	IO_L20P_5	AD22		
5	IO_L19N_5	AJ25		
5	IO_L19P_5	AJ24		
5	IO_L06N_5	AG25		
5	IO_L06P_5	AG24		
5	IO_L05N_5/VRP_5	AC20		
5	IO_L05P_5/VRN_5	AC21		
5	IO_L04N_5	AK26		
5	IO_L04P_5/VREF_5	AK27		
5	IO_L03N_5/D4/ALT_VRP_5	AH26		
5	IO_L03P_5/D5/ALT_VRN_5	AJ27		
5	IO_L02N_5/D6	AE22		
5	IO_L02P_5/D7	AE23		
5	IO_L01N_5/RDWR_B	AJ28		
5	IO_L01P_5/CS_B	AK29		
6	IO_L01P_6	AC22		
6	IO_L01N_6	AB23		
6	IO_L02P_6/VRN_6	AG28		
6	IO_L02N_6/VRP_6	AF28		
6	IO_L03P_6	AJ30		
6	IO_L03N_6/VREF_6	AH30		
6	IO_L04P_6	AD23		
6	IO_L04N_6	AC23		
6	IO_L05P_6	AF27		
6	IO_L05N_6	AE27		
6	IO_L06P_6	AG29		
6	IO_L06N_6	AH29		
6	IO_L19P_6	AE24		
6	IO_L19N_6	AD24		

Table 11: FF896 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
7	IO_L95N_7	R24		
7	IO_L94P_7	R29		
7	IO_L94N_7	T29		
7	IO_L93P_7/VREF_7	R27		
7	IO_L93N_7	P27		
7	IO_L92P_7	R23		
7	IO_L92N_7	P23		
7	IO_L91P_7	N30		
7	IO_L91N_7	P30		
7	IO_L78P_7	P26	NC	NC
7	IO_L78N_7	R26	NC	NC
7	IO_L77P_7	R22	NC	NC
7	IO_L77N_7	P22	NC	NC
7	IO_L76P_7	N29	NC	NC
7	IO_L76N_7	P29	NC	NC
7	IO_L75P_7/VREF_7	N27	NC	NC
7	IO_L75N_7	N26	NC	NC
7	IO_L74P_7	P25	NC	NC
7	IO_L74N_7	N25	NC	NC
7	IO_L73P_7	L30	NC	NC
7	IO_L73N_7	M30	NC	NC
7	IO_L72P_7	L28	NC	
7	IO_L72N_7	M28	NC	
7	IO_L71P_7	N24	NC	
7	IO_L71N_7	M24	NC	
7	IO_L70P_7	L29	NC	
7	IO_L70N_7	M29	NC	
7	IO_L69P_7/VREF_7	M27	NC	
7	IO_L69N_7	L27	NC	
7	IO_L68P_7	N23	NC	
7	IO_L68N_7	M23	NC	
7	IO_L67P_7	J30	NC	
7	IO_L67N_7	K30	NC	
7	IO_L54P_7	K26		
7	IO_L54N_7	L26		
7	IO_L53P_7	M25		
7	IO_L53N_7	L25		

Table 11: FF896 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
NA	GND	T13		
NA	GND	T12		
NA	GND	R19		
NA	GND	R18		
NA	GND	R17		
NA	GND	R16		
NA	GND	R15		
NA	GND	R14		
NA	GND	R13		
NA	GND	R12		
NA	GND	P24		
NA	GND	P19		
NA	GND	P18		
NA	GND	P17		
NA	GND	P16		
NA	GND	P15		
NA	GND	P14		
NA	GND	P13		
NA	GND	P12		
NA	GND	P7		
NA	GND	N19		
NA	GND	N18		
NA	GND	N17		
NA	GND	N16		
NA	GND	N15		
NA	GND	N14		
NA	GND	N13		
NA	GND	N12		
NA	GND	M26		
NA	GND	M19		
NA	GND	M18		
NA	GND	M17		
NA	GND	M16		
NA	GND	M15		
NA	GND	M14		
NA	GND	M13		
NA	GND	M12		

Table 12: FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
4	IO_L91N_4/VREF_4	AL16	
4	IO_L91P_4	AL17	
4	IO_L92N_4	AJ17	
4	IO_L92P_4	AJ16	
4	IO_L93N_4	AM15	
4	IO_L93P_4	AM14	
4	IO_L94N_4/VREF_4	AM16	
4	IO_L94P_4	AM17	
4	IO_L95N_4/GCLK3S	AF17	
4	IO_L95P_4/GCLK2P	AG17	
4	IO_L96N_4/GCLK1S	AK16	
4	IO_L96P_4/GCLK0P	AK17	
5	IO_L96N_5/GCLK7S	AK18	
5	IO_L96P_5/GCLK6P	AK19	
5	IO_L95N_5/GCLK5S	AG18	
5	IO_L95P_5/GCLK4P	AF18	
5	IO_L94N_5	AL18	
5	IO_L94P_5/VREF_5	AL19	
5	IO_L93N_5	AJ19	
5	IO_L93P_5	AJ18	
5	IO_L92N_5	AH19	
5	IO_L92P_5	AH18	
5	IO_L91N_5	AM19	
5	IO_L91P_5/VREF_5	AM20	
5	IO_L84N_5	AL21	NC
5	IO_L84P_5	AL20	NC
5	IO_L83N_5	AM22	NC
5	IO_L83P_5	AM21	NC
5	IO_L82N_5	AN18	NC
5	IO_L82P_5	AP18	NC
5	IO_L81N_5/VREF_5	AP20	NC
5	IO_L81P_5	AN19	NC
5	IO_L80N_5	AE18	NC
5	IO_L80P_5	AE19	NC
5	IO_L79N_5	AP22	NC

Table 12: FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
NA	GND	B34	
NA	GND	B33	
NA	GND	B20	
NA	GND	B15	
NA	GND	B2	
NA	GND	B1	
NA	GND	A33	
NA	GND	A32	
NA	GND	A27	
NA	GND	A8	
NA	GND	A3	
NA	GND	A2	

Notes:

1. See Table 4 for an explanation of the signals available on this pin.

FF1152 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)

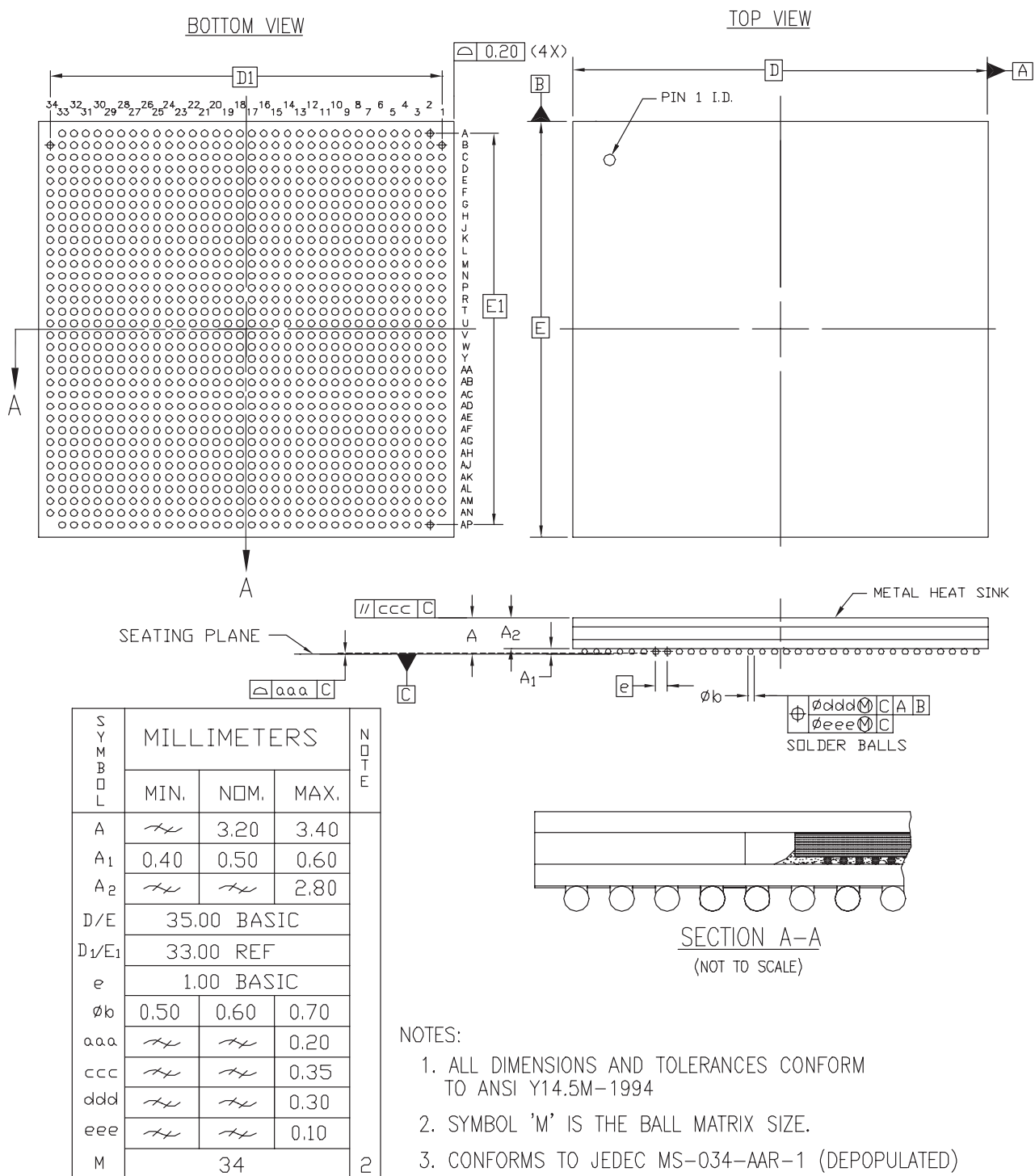


Figure 8: FF1152 Flip-Chip Fine-Pitch BGA Package Specifications

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
1	IO_L09N_1/VREF_1	G9	NC	
1	IO_L09P_1	G10	NC	
1	IO_L08N_1	K13	NC	
1	IO_L08P_1	K12	NC	
1	IO_L07N_1	A4	NC	
1	IO_L07P_1	A5	NC	
1	IO_L06N_1	F8		
1	IO_L06P_1	E8		
1	IO_L05N_1	J11		
1	IO_L05P_1	K11		
1	IO_L04N_1	C5		
1	IO_L04P_1/VREF_1	C6		
1	IO_L03N_1/VRP_1	D6		
1	IO_L03P_1/VRN_1	D7		
1	IO_L02N_1	H10		
1	IO_L02P_1	J10		
1	IO_L01N_1	C4		
1	IO_L01P_1	B4		
2	IO_L01N_2	E3		
2	IO_L01P_2	D2		
2	IO_L02N_2/VRP_2	L13		
2	IO_L02P_2/VRN_2	M13		
2	IO_L03N_2	F4		
2	IO_L03P_2/VREF_2	E4		
2	IO_L04N_2	E1		
2	IO_L04P_2	D1		
2	IO_L05N_2	L12		
2	IO_L05P_2	M11		
2	IO_L06N_2	G6		
2	IO_L06P_2	F5		
2	IO_L07N_2	F2	NC	
2	IO_L07P_2	E2	NC	
2	IO_L08N_2	M12	NC	
2	IO_L08P_2	N12	NC	
2	IO_L09N_2	H6	NC	

Table 14: BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000

Bank	Pin Description	Pin Number	No Connect in XC2V2000
2	IO_L23N_2	E2	
2	IO_L23P_2	F2	
2	IO_L24N_2	H4	
2	IO_L24P_2	J4	
2	IO_L25N_2	K8	NC
2	IO_L25P_2	L8	NC
2	IO_L27N_2	J7	NC
2	IO_L27P_2/VREF_2	K7	NC
2	IO_L43N_2	F1	
2	IO_L43P_2	G1	
2	IO_L44N_2	L9	
2	IO_L44P_2	M9	
2	IO_L45N_2	G2	
2	IO_L45P_2/VREF_2	J2	
2	IO_L46N_2	H3	
2	IO_L46P_2	J3	
2	IO_L47N_2	J6	
2	IO_L47P_2	L6	
2	IO_L48N_2	J5	
2	IO_L48P_2	K5	
2	IO_L49N_2	H1	
2	IO_L49P_2	J1	
2	IO_L50N_2	N10	
2	IO_L50P_2	P10	
2	IO_L51N_2	L7	
2	IO_L51P_2/VREF_2	M7	
2	IO_L52N_2	K3	
2	IO_L52P_2	L3	
2	IO_L53N_2	M8	
2	IO_L53P_2	N8	
2	IO_L54N_2	L5	
2	IO_L54P_2	M5	
2	IO_L67N_2	K2	
2	IO_L67P_2	L2	
2	IO_L68N_2	M6	
2	IO_L68P_2	N6	
2	IO_L69N_2	L4	
2	IO_L69P_2/VREF_2	M4	

Table 14: BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000

Bank	Pin Description	Pin Number	No Connect in XC2V2000
NA	GND	AG27	
NA	GND	AH4	
NA	GND	AH10	
NA	GND	AH16	
NA	GND	AH22	
NA	GND	AH28	
NA	GND	AJ1	
NA	GND	AJ3	
NA	GND	AJ29	
NA	GND	AJ31	
NA	GND	AK1	
NA	GND	AK2	
NA	GND	AK8	
NA	GND	AK24	
NA	GND	AK30	
NA	GND	AK31	
NA	GND	AL2	
NA	GND	AL3	
NA	GND	AL16	
NA	GND	AL29	
NA	GND	AL30	

Notes:

1. See Table 4 for an explanation of the signals available on this pin.