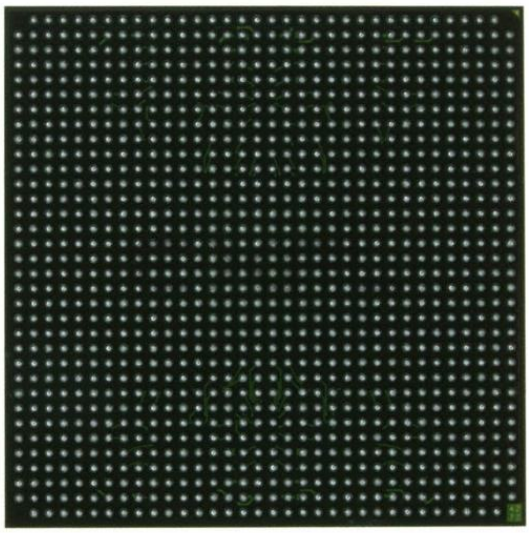

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	5760
Number of Logic Elements/Cells	-
Total RAM Bits	2211840
Number of I/O	824
Number of Gates	4000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v4000-4ff1152i

Architecture

Virtex-II Array Overview

Virtex-II devices are user-programmable gate arrays with various configurable elements. The Virtex-II architecture is optimized for high-density and high-performance logic designs. As shown in Figure 1, the programmable device is comprised of input/output blocks (IOBs) and internal configurable logic blocks (CLBs).

Programmable I/O blocks provide the interface between package pins and the internal configurable logic. Most popular and leading-edge I/O standards are supported by the programmable IOBs.

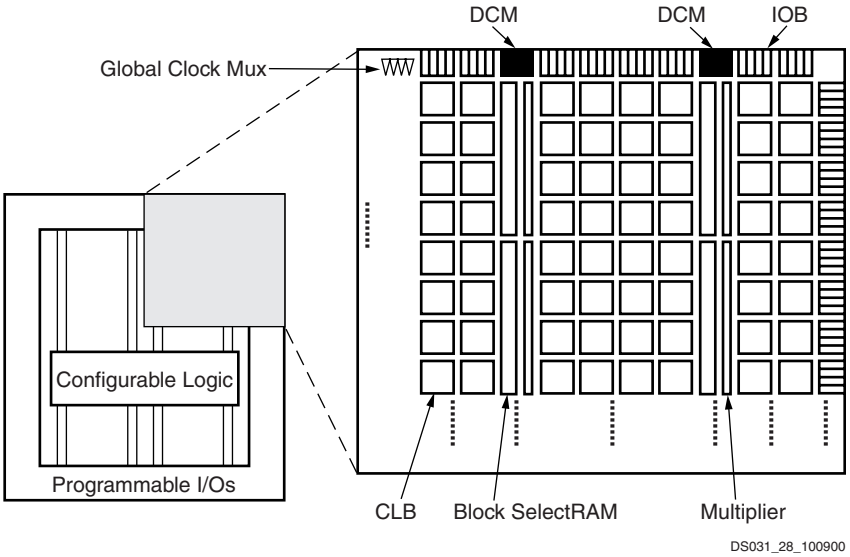


Figure 1: **Virtex-II Architecture Overview**

The internal configurable logic includes four major elements organized in a regular array.

- Configurable Logic Blocks (CLBs) provide functional elements for combinatorial and synchronous logic, including basic storage elements. BUFTs (3-state buffers) associated with each CLB element drive dedicated segmentable horizontal routing resources.
- Block SelectRAM memory modules provide large 18 Kbit storage elements of dual-port RAM.
- Multiplier blocks are 18-bit x 18-bit dedicated multipliers.
- DCM (Digital Clock Manager) blocks provide self-calibrating, fully digital solutions for clock distribution delay compensation, clock multiplication and division, coarse- and fine-grained clock phase shifting.

A new generation of programmable routing resources called Active Interconnect Technology interconnects all of these elements. The general routing matrix (GRM) is an array of routing switches. Each programmable element is tied to a switch matrix, allowing multiple connections to the general routing matrix. The overall programmable interconnection is hierarchical and designed to support high-speed designs.

All programmable elements, including the routing resources, are controlled by values stored in static memory cells. These values are loaded in the memory cells during configuration and can be reloaded to change the functions of the programmable elements.

Virtex-II Features

This section briefly describes Virtex-II features.

Input/Output Blocks (IOBs)

IOBs are programmable and can be categorized as follows:

- Input block with an optional single-data-rate or double-data-rate (DDR) register
- Output block with an optional single-data-rate or DDR register, and an optional 3-state buffer, to be driven directly or through a single or DDR register
- Bidirectional block (any combination of input and output configurations)

These registers are either edge-triggered D-type flip-flops or level-sensitive latches.

IOBs support the following single-ended I/O standards:

- LVTTL, LVCMOS (3.3V, 2.5V, 1.8V, and 1.5V)
- PCI-X compatible (133 MHz and 66 MHz) at 3.3V
- PCI compliant (66 MHz and 33 MHz) at 3.3V
- CardBus compliant (33 MHz) at 3.3V
- GTL and GTLP

Table 5: **Summary of Voltage Supply Requirements for All Input and Output Standards**

I/O Standard	V_{CCO}		V_{REF}	Termination Type	
	Output	Input	Input	Output	Input
LVDS_33	3.3	N/R	N/R[1]	N/R	N/R
LVDSEXT_33			N/R	N/R	N/R
LVPECL_33			N/R	N/R	N/R
SSTL3_I			1.5	N/R	N/R
SSTL3_II			1.5	N/R	N/R
AGP			1.32	N/R	N/R
LVTTL		3.3	N/R	N/R	N/R
LVCMOS33			N/R	N/R	N/R
LVDCI_33			N/R	Series	N/R
LVDCI_DV2_33			N/R	Series	N/R
PCI33_3			N/R	N/R	N/R
PCI66_3			N/R	N/R	N/R
PCIX			N/R	N/R	N/R
SSTL3_I_DCI			1.5	N/R	Split
SSTL3_II_DCI			1.5	Split	Split
LVDS_25	2.5	N/R	N/R	N/R	N/R
LVDSEXT_25			N/R	N/R	N/R
LDT_25			N/R	N/R	N/R
ULVDS_25			N/R	N/R	N/R
BLVDS_25			N/R	N/R	N/R
SSTL2_I			1.25	N/R	N/R
SSTL2_II			1.25	N/R	N/R
LVCMOS25		2.5	N/R	N/R	N/R
LVDCI_25			N/R	Series	N/R
LVDCI_DV2_25			N/R	Series	N/R
LVDS_25_DCI			N/R	N/R	Split
LVDSEXT_25_DCI			N/R	N/R	Split
SSTL2_I_DCI			1.25	N/R	Split
SSTL2_II_DCI			1.25	Split	Split

Table 5: **Summary of Voltage Supply Requirements for All Input and Output Standards *(Continued)***

I/O Standard	V_{CCO}		V_{REF}	Termination Type	
	Output	Input	Input	Output	Input
HSTL_III_18	1.8	N/R	1.1	N/R	N/R
HSTL_IV_18			1.1	N/R	N/R
HSTL_I_18			0.9	N/R	N/R
HSTL_II_18			0.9	N/R	N/R
SSTL18_I			0.9	N/R	N/R
SSTL18_II			0.9	N/R	N/R
LVCMOS18		1.8	N/R	N/R	N/R
LVDCI_18			N/R	Series	N/R
LVDCI_DV2_18			N/R	Series	N/R
HSTL_III_DCI_18			1.1	N/R	Single
HSTL_IV_DCI_18			1.1	Single	Single
HSTL_I_DCI_18			0.9	N/R	Split
HSTL_II_DCI_18			0.9	Split	Split
SSTL18_I_DCI			0.9	N/R	Split
SSTL18_II_DCI			0.9	Split	Split
HSTL_III	1.5	N/R	0.9	N/R	N/R
HSTL_IV			0.9	N/R	N/R
HSTL_I			0.75	N/R	N/R
HSTL_II			0.75	N/R	N/R
LVCMOS15		1.5	N/R	N/R	N/R
LVDCI_15			N/R	Series	N/R
LVDCI_DV2_15			N/R	Series	N/R
GTLP_DCI			1	Single	Single
HSTL_III_DCI			0.9	N/R	Single
HSTL_IV_DCI			0.9	Single	Single
HSTL_I_DCI			0.75	N/R	Split
HSTL_II_DCI			0.75	Split	Split
GTL_DCI	1.2	1.2	0.8	Single	Single
GTLP	N/R	N/R	1	N/R	N/R
GTL			0.8	N/R	N/R

Notes:
1. N/R = no requirement.

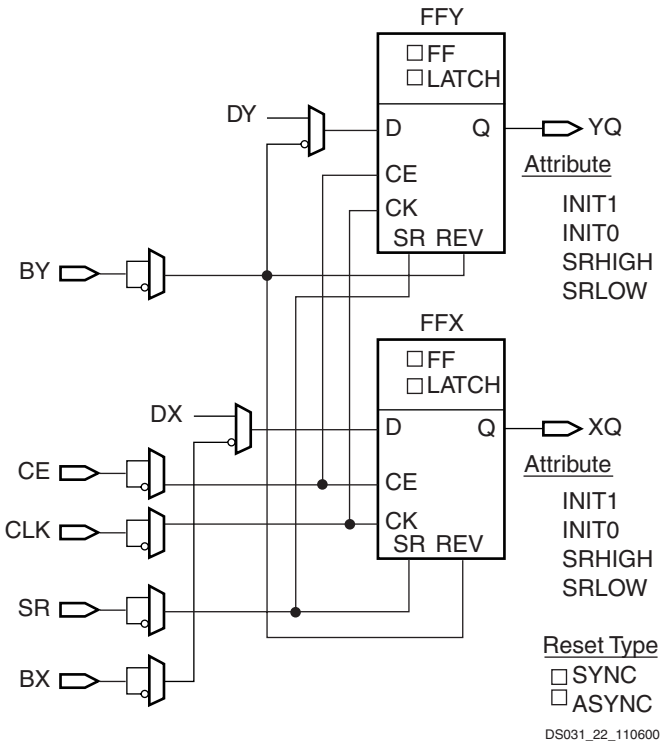


Figure 17: **Register / Latch Configuration in a Slice**

The set and reset functionality of a register or a latch can be configured as follows:

- No set or reset
- Synchronous set
- Synchronous reset
- Synchronous set and reset
- Asynchronous set (preset)
- Asynchronous reset (clear)
- Asynchronous set and reset (preset and clear)

The synchronous reset has precedence over a set, and an asynchronous clear has precedence over a preset.

Distributed SelectRAM Memory

Each function generator (LUT) can implement a 16 x 1-bit synchronous RAM resource called a distributed SelectRAM element. The SelectRAM elements are configurable within a CLB to implement the following:

- Single-Port 16 x 8 bit RAM
- Single-Port 32 x 4 bit RAM
- Single-Port 64 x 2 bit RAM
- Single-Port 128 x 1 bit RAM
- Dual-Port 16 x 4 bit RAM
- Dual-Port 32 x 2 bit RAM
- Dual-Port 64 x 1 bit RAM

Distributed SelectRAM memory modules are synchronous (write) resources. The combinatorial read access time is extremely fast, while the synchronous write simplifies high-speed designs. A synchronous read can be implemented with a storage element in the same slice. The distributed SelectRAM memory and the storage element share the same clock input. A Write Enable (WE) input is active High, and is driven by the SR input.

Table 9 shows the number of LUTs (2 per slice) occupied by each distributed SelectRAM configuration.

Table 9: **Distributed SelectRAM Configurations**

RAM	Number of LUTs
16 x 1S	1
16 x 1D	2
32 x 1S	2
32 x 1D	4
64 x 1S	4
64 x 1D	8
128 x 1S	8

Notes:
1. S = single-port configuration; D = dual-port configuration

For single-port configurations, distributed SelectRAM memory has one address port for synchronous writes and asynchronous reads.

For dual-port configurations, distributed SelectRAM memory has one port for synchronous writes and asynchronous reads and another port for asynchronous reads. The function generator (LUT) has separated read address inputs (A1, A2, A3, A4) and write address inputs (WG1/WF1, WG2/WF2, WG3/WF3, WG4/WF4).

In single-port mode, read and write addresses share the same address bus. In dual-port mode, one function generator (R/W port) is connected with shared read and write addresses. The second function generator has the A inputs (read) connected to the second read-only port address and the W inputs (write) shared with the first read/write port address.

Sum of Products

Each Virtex-II slice has a dedicated OR gate named ORCY, ORing together outputs from the slices carryout and the ORCY from an adjacent slice. The ORCY gate with the dedicated Sum of Products (SOP) chain are designed for implementing large, flexible SOP chains. One input of each ORCY is connected through the fast SOP chain to the output of the previous ORCY in the same slice row. The second input is connected to the output of the top MUXCY in the same slice, as shown in Figure 25.

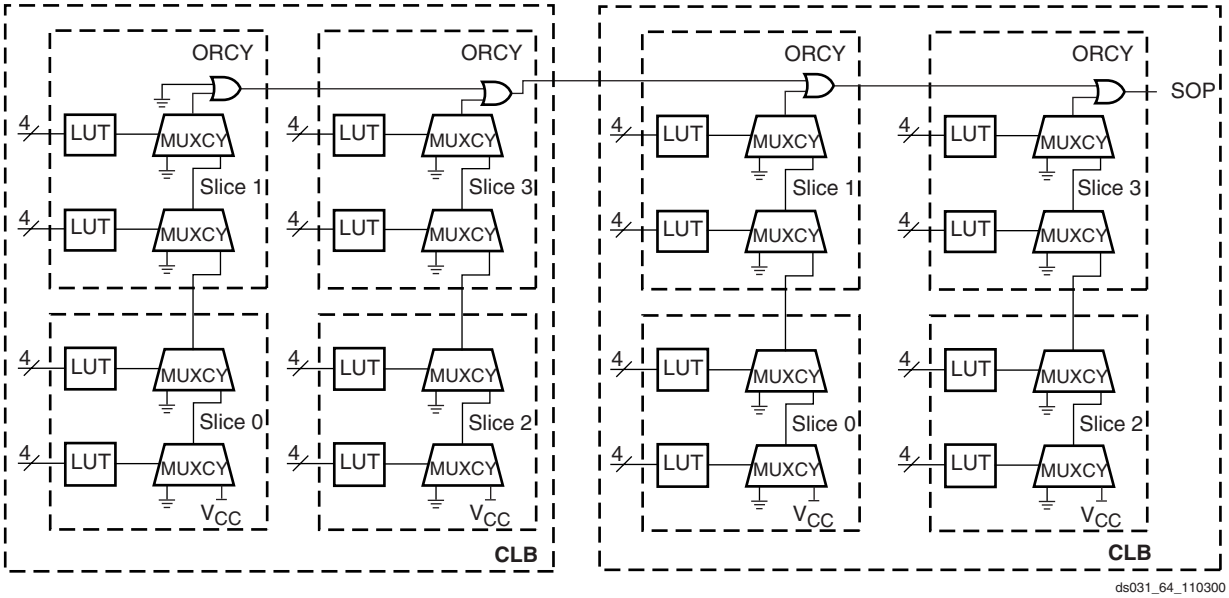


Figure 25: **Horizontal Cascade Chain**

LUTs and MUXCYs can implement large AND gates or other combinatorial logic functions. Figure 26 illustrates LUT and MUXCY resources configured as a 16-input AND gate.

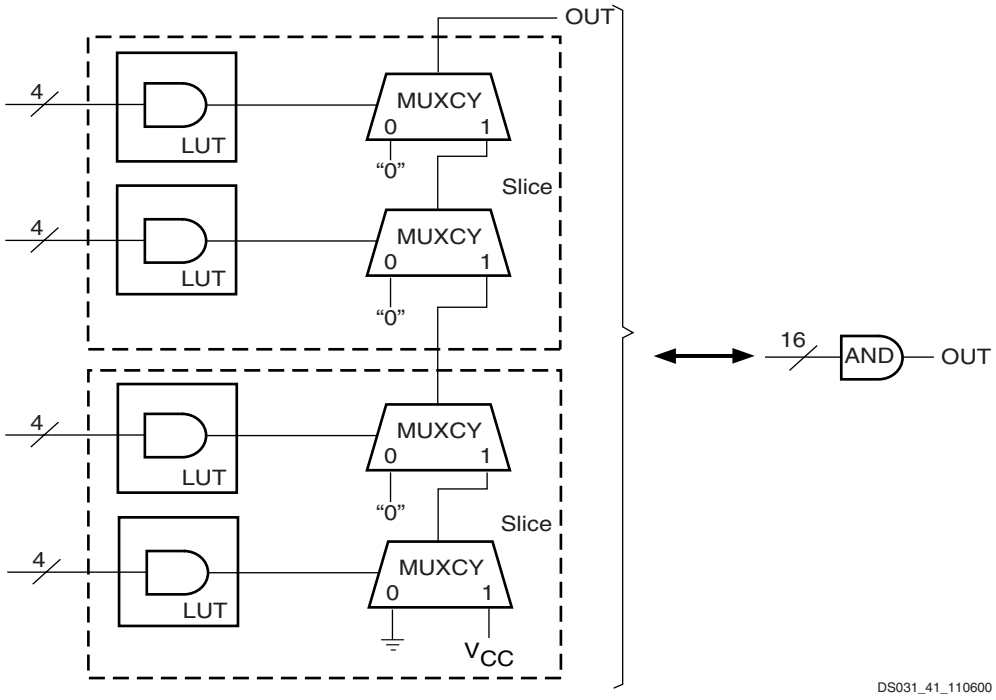


Figure 26: **Wide-Input AND Gate (16 Inputs)**

Table 14: **IOB Input Switching Characteristics *(Continued)***

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
Propagation Delays						
Pad to output IQ via transparent latch, no delay	T_{IOPLI}	All	0.83	0.91	1.05	ns, Max
Pad to output IQ via transparent latch, with delay	T_{IOPLID}	XC2V40	3.23	3.55	4.09	ns, Max
		XC2V80	3.23	3.55	4.09	ns, Max
		XC2V250	3.23	3.55	4.09	ns, Max
		XC2V500	3.23	3.55	4.09	ns, Max
		XC2V1000	3.23	3.55	4.09	ns, Max
		XC2V1500	3.23	3.55	4.09	ns, Max
		XC2V2000	3.23	3.55	4.09	ns, Max
		XC2V3000	3.32	3.65	4.20	ns, Max
		XC2V4000	3.32	3.65	4.20	ns, Max
		XC2V6000	3.60	3.95	4.55	ns, Max
		XC2V8000		3.95	4.55	ns, Max
Clock CLK to output IQ	T_{IOCKIQ}	All		0.67	0.77	ns, Max
Setup and Hold Times With Respect to Clock at IOB Input Register						
Pad, no delay	T_{IOPICK}/T_{IOICKP}	All	0.84/–0.36	0.92/–0.39	1.06/–0.45	ns, Min
Pad, with delay	$T_{IOPICKD}/T_{IOICKPD}$	XC2V40	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V80	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V250	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V500	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V1000	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V1500	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V2000	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V3000	3.33/–2.10	3.67/–2.31	4.22/–2.66	ns, Min
		XC2V4000	3.33/–2.10	3.67/–2.31	4.22/–2.66	ns, Min
		XC2V6000	3.61/–2.29	3.97/–2.52	4.56/–2.90	ns, Min
		XC2V8000		3.97/–2.52	4.56/–2.90	ns, Min
ICE input	$T_{IOICECK}/T_{IOCKICE}$	All		0.21/ 0.04	0.24/ 0.04	ns, Min
SR input (IFF, synchronous)	$T_{IOSRCKI}$	All	0.27	0.30	0.34	ns, Min
Set/Reset Delays						
SR input to IQ (asynchronous)	T_{IOSRIQ}	All	1.11	1.22	1.40	ns, Max
GSR to output IQ	T_{GSRQ}	All	5.44	5.98	6.88	ns, Max

Notes:
1. Input timing for LVTTL is measured at 1.4 V. For other I/O standards, see Table 18.

IOB Output Switching Characteristics Standard Adjustments

Table 17 gives all standard-specific adjustments for output delays terminating at pads, based on standard capacitive load, C_{REF}. Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

Table 17: **IOB Output Switching Characteristics Standard Adjustments**

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-6	-5	-4	
LVTTL (Low-Voltage Transistor-Transistor Logic), Slow, 2 mA	LVTTL_S2	T_{OLVTTL_S2}	9.42	9.71	10.68	ns
LVTTL, Slow, 4 mA	LVTTL_S4	T_{OLVTTL_S4}	5.77	5.95	6.55	ns
LVTTL, Slow, 6 mA	LVTTL_S6	T_{OLVTTL_S6}	4.11	4.24	4.66	ns
LVTTL, Slow, 8 mA	LVTTL_S8	T_{OLVTTL_S8}	2.87	2.96	3.26	ns
LVTTL, Slow, 12 mA	LVTTL_S12	T_{OLVTTL_S12}	2.32	2.39	2.63	ns
LVTTL, Slow, 16 mA	LVTTL_S16	T_{OLVTTL_S16}	1.70	1.75	1.93	ns
LVTTL, Slow, 24 mA	LVTTL_S24	T_{OLVTTL_S24}	1.26	1.30	1.43	ns
LVTTL, Fast, 2 mA	LVTTL_F2	T_{OLVTTL_F2}	6.52	6.72	7.39	ns
LVTTL, Fast, 4 mA	LVTTL_F4	T_{OLVTTL_F4}	2.80	2.88	3.17	ns
LVTTL, Fast, 6 mA	LVTTL_F6	T_{OLVTTL_F6}	1.57	1.62	1.78	ns
LVTTL, Fast, 8 mA	LVTTL_F8	T_{OLVTTL_F8}	0.46	0.48	0.52	ns
LVTTL, Fast, 12 mA	LVTTL_F12	T_{OLVTTL_F12}	0.00	0.00	0.00	ns
LVTTL, Fast, 16 mA	LVTTL_F16	T_{OLVTTL_F16}	–0.13	–0.14	–0.15	ns
LVTTL, Fast, 24 mA	LVTTL_F24	T_{OLVTTL_F24}	–0.22	–0.23	–0.26	ns
LVCMOS (Low-Voltage CMOS), 3.3V, Slow, 2 mA	LVCMOS33_S2	$T_{OLVCMOS33\_S2}$	7.67	7.91	8.70	ns
LVCMOS, 3.3V, Slow, 4 mA	LVCMOS33_S4	$T_{OLVCMOS33\_S4}$	4.37	4.50	4.95	ns
LVCMOS, 3.3V, Slow, 6 mA	LVCMOS33_S6	$T_{OLVCMOS33\_S6}$	3.34	3.44	3.78	ns
LVCMOS, 3.3V, Slow, 8 mA	LVCMOS33_S8	$T_{OLVCMOS33\_S8}$	2.29	2.36	2.60	ns
LVCMOS, 3.3V, Slow, 12 mA	LVCMOS33_S12	$T_{OLVCMOS33\_S12}$	1.91	1.97	2.16	ns
LVCMOS, 3.3V, Slow, 16 mA	LVCMOS33_S16	$T_{OLVCMOS33\_S16}$	1.24	1.27	1.40	ns
LVCMOS, 3.3V, Slow, 24 mA	LVCMOS33_S24	$T_{OLVCMOS33\_S24}$	1.18	1.22	1.34	ns
LVCMOS, 3.3V, Fast, 2 mA	LVCMOS33_F2	$T_{OLVCMOS33\_F2}$	5.82	6.00	6.60	ns
LVCMOS, 3.3V, Fast, 4 mA	LVCMOS33_F4	$T_{OLVCMOS33\_F4}$	2.48	2.55	2.81	ns
LVCMOS, 3.3V, Fast, 6 mA	LVCMOS33_F6	$T_{OLVCMOS33\_F6}$	1.28	1.31	1.45	ns
LVCMOS, 3.3V, Fast, 8 mA	LVCMOS33_F8	$T_{OLVCMOS33\_F8}$	0.48	0.49	0.54	ns
LVCMOS, 3.3V, Fast, 12 mA	LVCMOS33_F12	$T_{OLVCMOS33\_F12}$	0.27	0.28	0.31	ns
LVCMOS, 3.3V, Fast, 16 mA	LVCMOS33_F16	$T_{OLVCMOS33\_F16}$	–0.14	–0.14	–0.15	ns
LVCMOS, 3.3V, Fast, 24 mA	LVCMOS33_F24	$T_{OLVCMOS33\_F24}$	–0.21	–0.21	–0.23	ns
LVCMOS, 2.5V, Slow, 2 mA	LVCMOS25_S2	$T_{OLVCMOS25\_S2}$	9.11	9.39	10.33	ns
LVCMOS, 2.5V, Slow, 4 mA	LVCMOS25_S4	$T_{OLVCMOS25\_S4}$	5.00	5.16	5.67	ns
LVCMOS, 2.5V, Slow, 6 mA	LVCMOS25_S6	$T_{OLVCMOS25\_S6}$	4.53	4.67	5.13	ns
LVCMOS, 2.5V, Slow, 8 mA	LVCMOS25_S8	$T_{OLVCMOS25\_S8}$	3.86	3.98	4.38	ns
LVCMOS, 2.5V, Slow, 12 mA	LVCMOS25_S12	$T_{OLVCMOS25\_S12}$	2.84	2.93	3.22	ns
LVCMOS, 2.5V, Slow, 16 mA	LVCMOS25_S16	$T_{OLVCMOS25\_S16}$	2.36	2.43	2.67	ns
LVCMOS, 2.5V, Slow, 24 mA	LVCMOS25_S24	$T_{OLVCMOS25\_S24}$	2.00	2.06	2.27	ns
LVCMOS, 2.5V, Fast, 2 mA	LVCMOS25_F2	$T_{OLVCMOS25\_F2}$	4.06	4.18	4.60	ns
LVCMOS, 2.5V, Fast, 4 mA	LVCMOS25_F4	$T_{OLVCMOS25\_F4}$	1.15	1.18	1.30	ns
LVCMOS, 2.5V, Fast, 6 mA	LVCMOS25_F6	$T_{OLVCMOS25\_F6}$	0.72	0.74	0.81	ns
LVCMOS, 2.5V, Fast, 8 mA	LVCMOS25_F8	$T_{OLVCMOS25\_F8}$	0.33	0.34	0.37	ns
LVCMOS, 2.5V, Fast, 12 mA	LVCMOS25_F12	$T_{OLVCMOS25\_F12}$	0.02	0.02	0.03	ns

Table 17: **IOB Output Switching Characteristics Standard Adjustments *(Continued)***

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-6	-5	-4	
HSTL, Class II, 1.8V	HSTL_II_18	$T_{OHSTL\_II\_18}$	–0.17	–0.18	–0.20	ns
HSTL, Class III, 1.8V	HSTL_III_18	$T_{OHSTL\_III\_18}$	–0.16	–0.16	–0.18	ns
HSTL, Class IV, 1.8V	HSTL_IV_18	$T_{OHSTL\_IV\_18}$	–0.39	–0.40	–0.44	ns
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	$T_{OSSTL18\_I}$	0.20	0.20	0.22	ns
SSTL, Class II, 1.8V	SSTL18_II	$T_{OSSTL18\_II}$	–0.05	–0.05	–0.06	ns
SSTL, Class I, 2.5V	SSTL2_I	T_{OSSTL2_I}	0.21	0.22	0.24	ns
SSTL, Class II, 2.5V	SSTL2_II	T_{OSSTL2_II}	–0.15	–0.16	–0.18	ns
SSTL, Class I, 3.3V	SSTL3_I	T_{OSSTL3_I}	0.29	0.30	0.33	ns
SSTL, Class II, 3.3V	SSTL3_II	T_{OSSTL3_II}	–0.05	–0.05	–0.05	ns
AGP-2X/AGP (Accelerated Graphics Port)	AGP	T_{OAGP}	–0.27	–0.28	–0.31	ns
LVDCI (Low-Voltage Digitally Controlled Impedance), 3.3V	LVDCI_33	T_{OLVDCI_33}	0.74	0.77	0.84	ns
LVDCI, 2.5V	LVDCI_25	T_{OLVDCI_25}	0.78	0.80	0.88	ns
LVDCI, 1.8V	LVDCI_18	T_{OLVDCI_18}	0.84	0.87	0.95	ns
LVDCI, 1.5V	LVDCI_15	T_{OLVDCI_15}	1.82	1.88	2.06	ns
LVDCI, 3.3V, Half-Impedance	LVDCI_DV2_33	$T_{OLVDCI\_DV2\_33}$	0.12	0.12	0.13	ns
LVDCI, 2.5V, Half-Impedance	LVDCI_DV2_25	$T_{OLVDCI\_DV2\_25}$	0.03	0.03	0.03	ns
LVDCI, 1.8V, Half-Impedance	LVDCI_DV2_18	$T_{OLVDCI\_DV2\_18}$	0.42	0.43	0.48	ns
LVDCI, 1.5V, Half-Impedance	LVDCI_DV2_15	$T_{OLVDCI\_DV2\_15}$	1.20	1.23	1.36	ns
HSLVDCI (High-Speed Low-Voltage DCI), 1.5V	HSLVDCI_15	$T_{OHSLVDCI\_15}$	1.82	1.88	2.06	ns
HSLVDCI, 1.8V	HSLVDCI_18	$T_{OHSLVDCI\_18}$	1.05	1.08	1.24	ns
HSLVDCI, 2.5V	HSLVDCI_25	$T_{OHSLVDCI\_25}$	0.78	0.80	0.88	ns
HSLVDCI, 3.3V	HSLVDCI_33	$T_{OHSLVDCI\_33}$	0.74	0.77	0.84	ns
GTL (Gunning Transceiver Logic) with DCI	GTL_DCI	T_{OGTL_DCI}	–0.31	–0.32	–0.35	ns
GTL Plus with DCI	GTLP_DCI	T_{OGTLP_DCI}	–0.15	–0.16	–0.17	ns
HSTL (High-Speed Transceiver Logic), Class I, with DCI	HSTL_I_DCI	$T_{OHSTL\_I\_DCI}$	0.23	0.23	0.26	ns
HSTL, Class II, with DCI	HSTL_II_DCI	$T_{OHSTL\_II\_DCI}$	0.06	0.06	0.07	ns
HSTL, Class III, with DCI	HSTL_III_DCI	$T_{OHSTL\_III\_DCI}$	–0.17	–0.18	–0.20	ns
HSTL, Class IV, with DCI	HSTL_IV_DCI	$T_{OHSTL\_IV\_DCI}$	–0.46	–0.47	–0.52	ns
HSTL, Class I, 1.8V, with DCI	HSTL_I_DCI_18	$T_{OHSTL\_I\_DCI\_18}$	0.05	0.05	0.06	ns
HSTL, Class II, 1.8V, with DCI	HSTL_II_DCI_18	$T_{OHSTL\_II\_DCI\_18}$	–0.03	–0.03	–0.03	ns
HSTL, Class III, 1.8V, with DCI	HSTL_III_DCI_18	$T_{OHSTL\_III\_DCI\_18}$	–0.14	–0.14	–0.16	ns
HSTL, Class IV, 1.8V, with DCI	HSTL_IV_DCI_18	$T_{OHSTL\_IV\_DCI\_18}$	–0.41	–0.42	–0.47	ns
SSTL (Stub Series Terminated Logic), Class I, 1.8V, with DCI	SSTL18_I_DCI	$T_{OSSTL18\_I\_DCI}$	0.36	0.37	0.40	ns
SSTL, Class II, 1.8V, with DCI	SSTL18_II_DCI	$T_{OSSTL18\_II\_DCI}$	0.06	0.06	0.07	ns
SSTL, Class I, 2.5V, with DCI	SSTL2_I_DCI	$T_{OSSTL2\_I\_DCI}$	0.12	0.13	0.14	ns
SSTL, Class II, 2.5V, with DCI	SSTL2_II_DCI	$T_{OSSTL2\_II\_DCI}$	–0.10	–0.10	–0.11	ns
SSTL, Class I, 3.3V, with DCI	SSTL3_I_DCI	$T_{OSSTL3\_I\_DCI}$	0.15	0.16	0.17	ns
SSTL, Class II, 3.3V, with DCI	SSTL3_II_DCI	$T_{OSSTL3\_II\_DCI}$	0.08	0.08	0.09	ns

Source-Synchronous Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-II source-synchronous transmitter and receiver data-valid windows.

Table 45: **Duty Cycle Distortion and Clock-Tree Skew**

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
Duty Cycle Distortion(1)	T_{DCD_CLK0}	All	140	140	140	ps
	T_{DCD_CLK180}	All	50	50	50	ps
Clock Tree Skew(2)	T_{CKSKEW}	XC2V40	50	50	60	ps
		XC2V80	50	50	60	ps
		XC2V250	50	50	60	ps
		XC2V500	50	50	60	ps
		XC2V1000	80	80	90	ps
		XC2V1500	80	80	90	ps
		XC2V2000	100	100	110	ps
		XC2V3000	100	100	110	ps
		XC2V4000	400	400	450	ps
		XC2V6000	500	500	550	ps
		XC2V8000		600	650	ps

Notes:

1. These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
   T_{DCD_CLK0} applies to cases where local (IOB) inversion is used to provide the negative-edge clock to the DDR element in the I/O.
   T_{DCD_CLK180} applies to cases where the CLK180 output of the DCM is used to provide the negative-edge clock to the DDR element in the I/O.
2. This value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

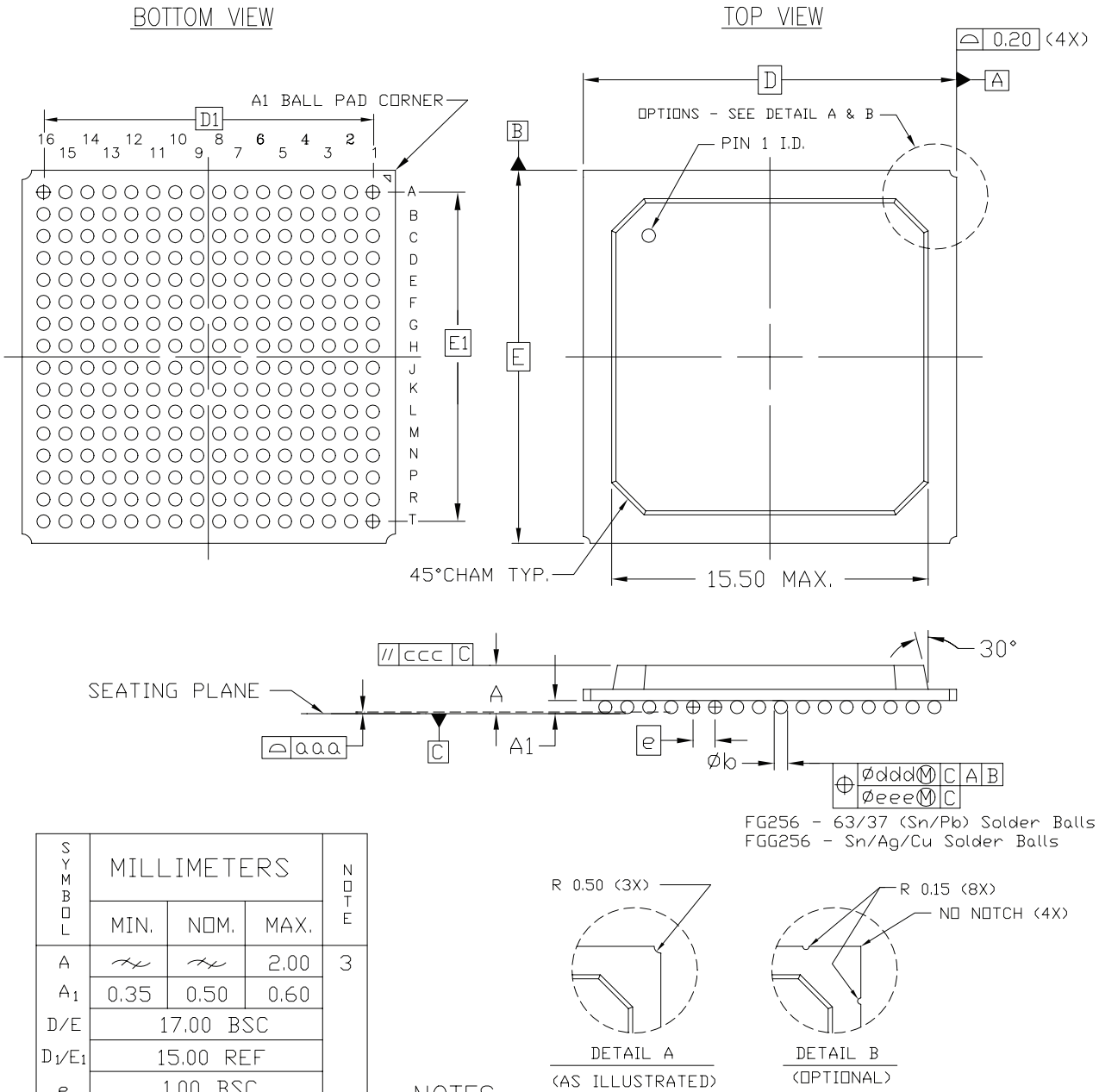
Table 46: **Package Skew**

Description	Symbol	Device/Package	Value	Units
Package Skew(1)	$T_{PKGSKEW}$	XC2V1000 / FF896	130	ps
		XC2V3000 / FF1152	115	ps
		XC2V3000 / BF957	130	ps
		XC2V4000 / FF1152	130	ps
		XC2V4000 / FF1517	200	ps
		XC2V4000 / BF957	140	ps
		XC2V6000 / FF1152	90	ps
		XC2V6000 / FF1517	105	ps
		XC2V6000 / BF957	105	ps

Notes:

1. These values represent the worst-case skew between any two balls of the package: shortest flight time to longest flight time from Pad to Ball (7.1ps per mm).
2. Package trace length information is available for these device/package combinations. This information can be used to deskew the package.

FG256/FGG256 Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A			2.00	3
A_1	0.35	0.50	0.60	
D/E	17.00 BSC			
D_1/E_1	15.00 REF			
e	1.00 BSC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.35	
ddd			0.30	
eee			0.10	
M	16			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994.
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. NOMINAL DIMENSION IS TYPICALLY 1.60-1.73mm
4. CONFORMS TO JEDEC MS-034-AAF-1

256-BALL FINE PITCH BGA (FG256/FGG256)

Figure 2: **FG256/FGG256 Fine-Pitch BGA Package Specifications**

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
4	IO_L02N_4/D0/DIN(1)	V18		
4	IO_L02P_4/D1	V17		
4	IO_L03N_4/D2/ALT_VRP_4	W18		
4	IO_L03P_4/D3/ALT_VRN_4	Y18		
4	IO_L04N_4/VREF_4	AA18		
4	IO_L04P_4	AB18		
4	IO_L05N_4/VRP_4	W17		
4	IO_L05P_4/VRN_4	Y17		
4	IO_L06N_4	AA17		
4	IO_L06P_4	AB17		
4	IO_L19N_4	V16	NC	NC
4	IO_L19P_4	V15	NC	NC
4	IO_L21N_4	W16	NC	NC
4	IO_L21P_4/VREF_4	Y16	NC	NC
4	IO_L22N_4	AA16	NC	NC
4	IO_L22P_4	AB16	NC	NC
4	IO_L24N_4	W15	NC	NC
4	IO_L24P_4	Y15	NC	NC
4	IO_L49N_4	AA15	NC	
4	IO_L49P_4	AB15	NC	
4	IO_L51N_4	U14	NC	
4	IO_L51P_4/VREF_4	V14	NC	
4	IO_L52N_4	W14	NC	
4	IO_L52P_4	Y14	NC	
4	IO_L54N_4	AA14	NC	
4	IO_L54P_4	AB14	NC	
4	IO_L91N_4/VREF_4	U13		
4	IO_L91P_4	V13		
4	IO_L92N_4	W13		
4	IO_L92P_4	Y13		
4	IO_L93N_4	AA13		
4	IO_L93P_4	AB13		
4	IO_L94N_4/VREF_4	U12		
4	IO_L94P_4	V12		

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
2	IO_L45N_2	H23		
2	IO_L45P_2/VREF_2	H24		
2	IO_L46N_2	J21		
2	IO_L46P_2	J20		
2	IO_L48N_2	H25		
2	IO_L48P_2	H26		
2	IO_L49N_2	J22		
2	IO_L49P_2	J23		
2	IO_L51N_2	K21		
2	IO_L51P_2/VREF_2	K22		
2	IO_L52N_2	K20		
2	IO_L52P_2	L20		
2	IO_L54N_2	J24		
2	IO_L54P_2	J25		
2	IO_L67N_2	K23		
2	IO_L67P_2	K24		
2	IO_L69N_2	J26		
2	IO_L69P_2/VREF_2	K26		
2	IO_L70N_2	L22		
2	IO_L70P_2	L21		
2	IO_L72N_2	L25		
2	IO_L72P_2	L26		
2	IO_L73N_2	L19	NC	
2	IO_L73P_2	M19	NC	
2	IO_L75N_2	L23	NC	
2	IO_L75P_2/VREF_2	L24	NC	
2	IO_L76N_2	M22	NC	
2	IO_L76P_2	M21	NC	
2	IO_L78N_2	M23	NC	
2	IO_L78P_2	M24	NC	
2	IO_L91N_2	M25		
2	IO_L91P_2	M26		
2	IO_L93N_2	M20		
2	IO_L93P_2/VREF_2	N20		
2	IO_L94N_2	N22		
2	IO_L94P_2	N21		
2	IO_L96N_2	N24		

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
3	IO_L46P_3	Y26		
3	IO_L45N_3/VREF_3	U20		
3	IO_L45P_3	V20		
3	IO_L43N_3	W25		
3	IO_L43P_3	W24		
3	IO_L25N_3	V21	NC	NC
3	IO_L25P_3	W21	NC	NC
3	IO_L24N_3	AA26		
3	IO_L24P_3	AA25		
3	IO_L22N_3	Y24		
3	IO_L22P_3	Y23		
3	IO_L21N_3/VREF_3	W22		
3	IO_L21P_3	W23		
3	IO_L19N_3	AB26		
3	IO_L19P_3	AB25		
3	IO_L06N_3	AC26		
3	IO_L06P_3	AC25		
3	IO_L04N_3	AD26		
3	IO_L04P_3	AD25		
3	IO_L03N_3/VREF_3	AA24		
3	IO_L03P_3	AA23		
3	IO_L02N_3/VRP_3	AB24		
3	IO_L02P_3/VRN_3	AB23		
3	IO_L01N_3	Y22		
3	IO_L01P_3	AA22		
4	IO_L01N_4/BUSY/DOUT(1)	AD21		
4	IO_L01P_4/INIT_B	AC21		
4	IO_L02N_4/D0/DIN(1)	Y20		
4	IO_L02P_4/D1	Y19		
4	IO_L03N_4/D2/ALT_VRP_4	AA20		
4	IO_L03P_4/D3/ALT_VRN_4	AB20		
4	IO_L04N_4/VREF_4	AC22		
4	IO_L04P_4	AE21		
4	IO_L05N_4/VRP_4	AE26		
4	IO_L05P_4/VRN_4	AF25		
4	IO_L06N_4	W20		

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
7	IO_L78N_7	M2	NC	
7	IO_L76P_7	M5	NC	
7	IO_L76N_7	M6	NC	
7	IO_L75P_7/VREF_7	M3	NC	
7	IO_L75N_7	M4	NC	
7	IO_L73P_7	M7	NC	
7	IO_L73N_7	M8	NC	
7	IO_L72P_7	L1		
7	IO_L72N_7	L2		
7	IO_L70P_7	L5		
7	IO_L70N_7	L6		
7	IO_L69P_7/VREF_7	L3		
7	IO_L69N_7	L4		
7	IO_L67P_7	K1		
7	IO_L67N_7	J1		
7	IO_L54P_7	K3		
7	IO_L54N_7	K4		
7	IO_L52P_7	K5		
7	IO_L52N_7	K6		
7	IO_L51P_7/VREF_7	L8		
7	IO_L51N_7	L7		
7	IO_L49P_7	J2		
7	IO_L49N_7	H1		
7	IO_L48P_7	J3		
7	IO_L48N_7	J4		
7	IO_L46P_7	J5		
7	IO_L46N_7	J6		
7	IO_L45P_7/VREF_7	H5		
7	IO_L45N_7	H4		
7	IO_L43P_7	K7		
7	IO_L43N_7	J7		
7	IO_L25P_7	H2	NC	NC
7	IO_L25N_7	H3	NC	NC
7	IO_L24P_7	G1		
7	IO_L24N_7	F1		
7	IO_L22P_7	G3		
7	IO_L22N_7	G4		

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
NA	VCCINT	H19		
NA	VCCINT	H8		
NA	GND	AF26		
NA	GND	AF1		
NA	GND	AE25		
NA	GND	AE14		
NA	GND	AE13		
NA	GND	AE2		
NA	GND	AD24		
NA	GND	AD3		
NA	GND	AC23		
NA	GND	AC4		
NA	GND	AB22		
NA	GND	AB5		
NA	GND	AA21		
NA	GND	AA6		
NA	GND	U17		
NA	GND	U16		
NA	GND	U15		
NA	GND	U14		
NA	GND	U13		
NA	GND	U12		
NA	GND	U11		
NA	GND	U10		
NA	GND	T17		
NA	GND	T16		
NA	GND	T15		
NA	GND	T14		
NA	GND	T13		
NA	GND	T12		
NA	GND	T11		
NA	GND	T10		
NA	GND	R17		
NA	GND	R16		
NA	GND	R15		
NA	GND	R14		
NA	GND	R13		

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
3	IO_L53P_3	AD2	
3	IO_L52N_3	AC8	
3	IO_L52P_3	AB8	
3	IO_L51N_3/VREF_3	AB10	
3	IO_L51P_3	AC10	
3	IO_L50N_3	AD5	
3	IO_L50P_3	AE5	
3	IO_L49N_3	AE4	
3	IO_L49P_3	AF4	
3	IO_L48N_3	AB9	
3	IO_L48P_3	AC9	
3	IO_L47N_3	AE2	
3	IO_L47P_3	AF1	
3	IO_L46N_3	AD6	
3	IO_L46P_3	AE6	
3	IO_L45N_3/VREF_3	AD9	
3	IO_L45P_3	AE9	
3	IO_L44N_3	AF2	
3	IO_L44P_3	AG2	
3	IO_L43N_3	AF3	
3	IO_L43P_3	AG3	
3	IO_L30N_3	AD7	
3	IO_L30P_3	AE7	
3	IO_L29N_3	AF5	
3	IO_L29P_3	AG5	
3	IO_L28N_3	AE8	
3	IO_L28P_3	AD8	
3	IO_L27N_3/VREF_3	AF8	
3	IO_L27P_3	AF9	
3	IO_L26N_3	AH1	
3	IO_L26P_3	AJ1	
3	IO_L25N_3	AG4	
3	IO_L25P_3	AH5	
3	IO_L24N_3	AF6	
3	IO_L24P_3	AG6	
3	IO_L23N_3	AH3	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
5	IO_L79P_5	AP21	NC
5	IO_L78N_5	AK22	
5	IO_L78P_5	AK21	
5	IO_L77N_5	AD18	
5	IO_L77P_5	AD19	
5	IO_L76N_5	AN22	
5	IO_L76P_5	AN21	
5	IO_L75N_5/VREF_5	AJ20	
5	IO_L75P_5	AH20	
5	IO_L74N_5	AG19	
5	IO_L74P_5	AG20	
5	IO_L73N_5	AP24	
5	IO_L73P_5	AP23	
5	IO_L72N_5	AL23	
5	IO_L72P_5	AL22	
5	IO_L71N_5	AF20	
5	IO_L71P_5	AF21	
5	IO_L70N_5	AM24	
5	IO_L70P_5	AM23	
5	IO_L69N_5/VREF_5	AJ21	
5	IO_L69P_5	AJ22	
5	IO_L68N_5	AJ24	
5	IO_L68P_5	AJ23	
5	IO_L67N_5	AN24	
5	IO_L67P_5	AN23	
5	IO_L60N_5	AN26	NC
5	IO_L60P_5	AN25	NC
5	IO_L54N_5	AL25	
5	IO_L54P_5	AL24	
5	IO_L53N_5	AE20	
5	IO_L53P_5	AE21	
5	IO_L52N_5	AN27	
5	IO_L52P_5	AP26	
5	IO_L51N_5/VREF_5	AP29	
5	IO_L51P_5	AP28	
5	IO_L50N_5	AG21	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
6	IO_L71P_6	AD34	
6	IO_L71N_6	AC34	
6	IO_L72P_6	AC31	
6	IO_L72N_6	AD31	
6	IO_L73P_6	Y27	
6	IO_L73N_6	W27	
6	IO_L74P_6	AB29	
6	IO_L74N_6	AA29	
6	IO_L75P_6	AB31	
6	IO_L75N_6/VREF_6	AA31	
6	IO_L76P_6	Y28	
6	IO_L76N_6	Y29	
6	IO_L77P_6	AB33	
6	IO_L77N_6	AA33	
6	IO_L78P_6	AA30	
6	IO_L78N_6	AB30	
6	IO_L79P_6	W24	NC
6	IO_L79N_6	V24	NC
6	IO_L80P_6	AB34	NC
6	IO_L80N_6	AA34	NC
6	IO_L81P_6	W33	NC
6	IO_L81N_6/VREF_6	Y34	NC
6	IO_L82P_6	W25	NC
6	IO_L82N_6	V25	NC
6	IO_L83P_6	Y32	NC
6	IO_L83N_6	AA32	NC
6	IO_L84P_6	W29	NC
6	IO_L84N_6	V29	NC
6	IO_L91P_6	W28	
6	IO_L91N_6	V28	
6	IO_L92P_6	V33	
6	IO_L92N_6	V34	
6	IO_L93P_6	Y31	
6	IO_L93N_6/VREF_6	W31	
6	IO_L94P_6	V26	
6	IO_L94N_6	V27	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
4	IO_L68P_4	AL17		
4	IO_L69N_4	AT16		
4	IO_L69P_4/VREF_4	AT15		
4	IO_L70N_4	AU14		
4	IO_L70P_4	AU13		
4	IO_L71N_4	AH18		
4	IO_L71P_4	AH19		
4	IO_L72N_4	AN17		
4	IO_L72P_4	AN16		
4	IO_L73N_4	AW15		
4	IO_L73P_4	AW14		
4	IO_L74N_4	AJ18		
4	IO_L74P_4	AJ19		
4	IO_L75N_4	AP17		
4	IO_L75P_4/VREF_4	AP16		
4	IO_L76N_4	AV15		
4	IO_L76P_4	AU15		
4	IO_L77N_4	AK18		
4	IO_L77P_4	AK19		
4	IO_L78N_4	AR18		
4	IO_L78P_4	AR17		
4	IO_L79N_4	AU17		
4	IO_L79P_4	AU16		
4	IO_L80N_4	AL18		
4	IO_L80P_4	AL19		
4	IO_L81N_4	AN19		
4	IO_L81P_4/VREF_4	AN18		
4	IO_L82N_4	AV17		
4	IO_L82P_4	AV16		
4	IO_L83N_4	AM18		
4	IO_L83P_4	AM19		
4	IO_L84N_4	AP19		
4	IO_L84P_4	AP18		
4	IO_L85N_4	AW17	NC	NC
4	IO_L85P_4	AW16	NC	NC
4	IO_L91N_4/VREF_4	AV19		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
4	IO_L91P_4	AV18		
4	IO_L92N_4	AH20		
4	IO_L92P_4	AJ20		
4	IO_L93N_4	AR19		
4	IO_L93P_4	AT18		
4	IO_L94N_4/VREF_4	AW19		
4	IO_L94P_4	AW18		
4	IO_L95N_4/GCLK3S	AL20		
4	IO_L95P_4/GCLK2P	AM20		
4	IO_L96N_4/GCLK1S	AU19		
4	IO_L96P_4/GCLK0P	AT19		
5	IO_L96N_5/GCLK7S	AP21		
5	IO_L96P_5/GCLK6P	AP20		
5	IO_L95N_5/GCLK5S	AN21		
5	IO_L95P_5/GCLK4P	AN22		
5	IO_L94N_5	AU21		
5	IO_L94P_5/VREF_5	AU20		
5	IO_L93N_5	AR21		
5	IO_L93P_5	AR20		
5	IO_L92N_5	AM21		
5	IO_L92P_5	AM22		
5	IO_L91N_5	AW22		
5	IO_L91P_5/VREF_5	AW21		
5	IO_L85N_5	AV22	NC	NC
5	IO_L85P_5	AV21	NC	NC
5	IO_L84N_5	AT22		
5	IO_L84P_5	AT21		
5	IO_L83N_5	AL21		
5	IO_L83P_5	AL22		
5	IO_L82N_5	AW24		
5	IO_L82P_5	AW23		
5	IO_L81N_5/VREF_5	AR23		
5	IO_L81P_5	AR22		
5	IO_L80N_5	AK21		
5	IO_L80P_5	AK22		

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
5	VCCO_5	AJ18	
5	VCCO_5	AJ25	
6	VCCO_6	U20	
6	VCCO_6	U21	
6	VCCO_6	V20	
6	VCCO_6	V21	
6	VCCO_6	V24	
6	VCCO_6	V29	
6	VCCO_6	W20	
6	VCCO_6	W21	
6	VCCO_6	Y21	
6	VCCO_6	AB26	
6	VCCO_6	AE29	
7	VCCO_7	G29	
7	VCCO_7	K26	
7	VCCO_7	M21	
7	VCCO_7	N20	
7	VCCO_7	N21	
7	VCCO_7	P20	
7	VCCO_7	P21	
7	VCCO_7	P24	
7	VCCO_7	P29	
7	VCCO_7	R20	
7	VCCO_7	R21	
NA	CCLK	AJ4	
NA	PROG_B	D27	
NA	DONE	AG6	
NA	M0	AH27	
NA	M1	AJ28	
NA	M2	AG26	
NA	HSWAP_EN	E26	
NA	TCK	K11	
NA	TDI	C28	
NA	TDO	C4	
NA	TMS	J10	
NA	PWRDWN_B	AH5	
NA	DXN	F25	