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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	5760
Number of Logic Elements/Cells	-
Total RAM Bits	2211840
Number of I/O	912
Number of Gates	4000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FCBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v4000-4ff1517i

Table 13: **Virtex-II Logic Resources Available in All CLBs**

Device	CLB Array: Row x Column	Number of Slices	Number of LUTs	Max Distributed SelectRAM or Shift Register (bits)	Number of Flip-Flops	Number of Carry-Chains(1)	Number of SOP Chains(1)
XC2V40	8 x 8	256	512	8,192	512	16	16
XC2V80	16 x 8	512	1,024	16,384	1,024	16	32
XC2V250	24 x 16	1,536	3,072	49,152	3,072	32	48
XC2V500	32 x 24	3,072	6,144	98,304	6,144	48	64
XC2V1000	40 x 32	5,120	10,240	163,840	10,240	64	80
XC2V1500	48 x 40	7,680	15,360	245,760	15,360	80	96
XC2V2000	56 x 48	10,752	21,504	344,064	21,504	96	112
XC2V3000	64 x 56	14,336	28,672	458,752	28,672	112	128
XC2V4000	80 x 72	23,040	46,080	737,280	46,080	144	160
XC2V6000	96 x 88	33,792	67,584	1,081,344	67,584	176	192
XC2V8000	112 x 104	46,592	93,184	1,490,944	93,184	208	224

Notes:
1. The carry-chains and SOP chains can be split or cascaded.

18 Kbit Block SelectRAM Resources

Introduction

Virtex-II devices incorporate large amounts of 18 Kbit block SelectRAM. These complement the distributed SelectRAM resources that provide shallow RAM structures implemented in CLBs. Each Virtex-II block SelectRAM is an 18 Kbit true dual-port RAM with two independently clocked and independently controlled synchronous ports that access a common storage area. Both ports are functionally identical. CLK, EN, WE, and SSR polarities are defined through configuration.

Each port has the following types of inputs: Clock and Clock Enable, Write Enable, Set/Reset, and Address, as well as separate Data/parity data inputs (for write) and Data/parity data outputs (for read).

Operation is synchronous; the block SelectRAM behaves like a register. Control, address and data inputs must (and need only) be valid during the set-up time window prior to a rising (or falling, a configuration option) clock edge. Data outputs change as a result of the same clock edge.

Configuration

The Virtex-II block SelectRAM supports various configurations, including single- and dual-port RAM and various data/address aspect ratios. Supported memory configurations for single- and dual-port modes are shown in Table 14.

Table 14: **Dual- and Single-Port Configurations**

16K x 1 bit	2K x 9 bits
8K x 2 bits	1K x 18 bits
4K x 4 bits	512 x 36 bits

Single-Port Configuration

As a single-port RAM, the block SelectRAM has access to the 18 Kbit memory locations in any of the 2K x 9-bit, 1K x 18-bit, or 512 x 36-bit configurations and to 16 Kbit memory locations in any of the 16K x 1-bit, 8K x 2-bit, or 4K x 4-bit configurations. The advantage of the 9-bit, 18-bit and 36-bit widths is the ability to store a parity bit for each eight bits. Parity bits must be generated or checked externally in user logic. In such cases, the width is viewed as 8 + 1, 16 + 2, or 32 + 4. These extra parity bits are stored and behave exactly as the other bits, including the timing parameters. Video applications can use the 9-bit ratio of Virtex-II block SelectRAM memory to advantage.

Each block SelectRAM cell is a fully synchronous memory as illustrated in Figure 29. Input data bus and output data bus widths are identical.

Virtex-II Electrical Characteristics

Virtex-II™ devices are provided in -6, -5, and -4 speed grades, with -6 having the highest performance.

Virtex-II DC and AC characteristics are specified for both commercial and industrial grades. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -4 speed grade industrial device are the same as for a -4 speed grade commercial device). However, only selected speed grades and/or devices might be available in the industrial range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications. Contact Xilinx for design considerations requiring more detailed information.

All specifications are subject to change without notice.

Virtex-II DC Characteristics

Table 1: **Absolute Maximum Ratings**

Symbol	Description(1)			Units
V_{CCINT}	Internal supply voltage relative to GND		–0.5 to 1.65	V
V_{CCAUX}	Auxiliary supply voltage relative to GND		–0.5 to 4.0	V
V_{CCO}	Output drivers supply voltage relative to GND		–0.5 to 4.0	V
V_{BATT}	Key memory battery backup supply		–0.5 to 4.0	V
V_{REF}	Input reference voltage		–0.5 to V_{CCO} + 0.5	V
V_{IN}(3)	Input voltage relative to GND (user and dedicated I/Os)		–0.5 to V_{CCO} + 0.5	V
V_{TS}	Voltage applied to 3-state output (user and dedicated I/Os)		–0.5 to 4.0	V
T_{STG}	Storage temperature (ambient)		–65 to +150	°C
T_{SOL}	Maximum soldering temperature(2)	All regular FF/BF flip-chip and FG/BG/CS wire-bond packages	+220	°C
		Pb-free FGG456, FGG676, BGG575, and BGG728 wire-bond packages	+250	°C
		Pb-free FGG256 and CSG144 wire-bond packages	+260	°C
T_J	Maximum junction temperature(2)		+125	°C

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. For soldering guidelines and thermal considerations, see the **Device Packaging and Thermal Characteristics Guide** information on the Xilinx website.
3. Inputs configured as PCI are fully PCI compliant. This statement takes precedence over any specification that would imply that the device is not PCI compliant.

Table 17: **IOB Output Switching Characteristics Standard Adjustments *(Continued)***

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-6	-5	-4	
HSTL, Class II, 1.8V	HSTL_II_18	$T_{OHSTL\_II\_18}$	–0.17	–0.18	–0.20	ns
HSTL, Class III, 1.8V	HSTL_III_18	$T_{OHSTL\_III\_18}$	–0.16	–0.16	–0.18	ns
HSTL, Class IV, 1.8V	HSTL_IV_18	$T_{OHSTL\_IV\_18}$	–0.39	–0.40	–0.44	ns
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	$T_{OSSTL18\_I}$	0.20	0.20	0.22	ns
SSTL, Class II, 1.8V	SSTL18_II	$T_{OSSTL18\_II}$	–0.05	–0.05	–0.06	ns
SSTL, Class I, 2.5V	SSTL2_I	T_{OSSTL2_I}	0.21	0.22	0.24	ns
SSTL, Class II, 2.5V	SSTL2_II	T_{OSSTL2_II}	–0.15	–0.16	–0.18	ns
SSTL, Class I, 3.3V	SSTL3_I	T_{OSSTL3_I}	0.29	0.30	0.33	ns
SSTL, Class II, 3.3V	SSTL3_II	T_{OSSTL3_II}	–0.05	–0.05	–0.05	ns
AGP-2X/AGP (Accelerated Graphics Port)	AGP	T_{OAGP}	–0.27	–0.28	–0.31	ns
LVDCI (Low-Voltage Digitally Controlled Impedance), 3.3V	LVDCI_33	T_{OLVDCI_33}	0.74	0.77	0.84	ns
LVDCI, 2.5V	LVDCI_25	T_{OLVDCI_25}	0.78	0.80	0.88	ns
LVDCI, 1.8V	LVDCI_18	T_{OLVDCI_18}	0.84	0.87	0.95	ns
LVDCI, 1.5V	LVDCI_15	T_{OLVDCI_15}	1.82	1.88	2.06	ns
LVDCI, 3.3V, Half-Impedance	LVDCI_DV2_33	$T_{OLVDCI\_DV2\_33}$	0.12	0.12	0.13	ns
LVDCI, 2.5V, Half-Impedance	LVDCI_DV2_25	$T_{OLVDCI\_DV2\_25}$	0.03	0.03	0.03	ns
LVDCI, 1.8V, Half-Impedance	LVDCI_DV2_18	$T_{OLVDCI\_DV2\_18}$	0.42	0.43	0.48	ns
LVDCI, 1.5V, Half-Impedance	LVDCI_DV2_15	$T_{OLVDCI\_DV2\_15}$	1.20	1.23	1.36	ns
HSLVDCI (High-Speed Low-Voltage DCI), 1.5V	HSLVDCI_15	$T_{OHSLVDCI\_15}$	1.82	1.88	2.06	ns
HSLVDCI, 1.8V	HSLVDCI_18	$T_{OHSLVDCI\_18}$	1.05	1.08	1.24	ns
HSLVDCI, 2.5V	HSLVDCI_25	$T_{OHSLVDCI\_25}$	0.78	0.80	0.88	ns
HSLVDCI, 3.3V	HSLVDCI_33	$T_{OHSLVDCI\_33}$	0.74	0.77	0.84	ns
GTL (Gunning Transceiver Logic) with DCI	GTL_DCI	T_{OGTL_DCI}	–0.31	–0.32	–0.35	ns
GTL Plus with DCI	GTLP_DCI	T_{OGTLP_DCI}	–0.15	–0.16	–0.17	ns
HSTL (High-Speed Transceiver Logic), Class I, with DCI	HSTL_I_DCI	$T_{OHSTL\_I\_DCI}$	0.23	0.23	0.26	ns
HSTL, Class II, with DCI	HSTL_II_DCI	$T_{OHSTL\_II\_DCI}$	0.06	0.06	0.07	ns
HSTL, Class III, with DCI	HSTL_III_DCI	$T_{OHSTL\_III\_DCI}$	–0.17	–0.18	–0.20	ns
HSTL, Class IV, with DCI	HSTL_IV_DCI	$T_{OHSTL\_IV\_DCI}$	–0.46	–0.47	–0.52	ns
HSTL, Class I, 1.8V, with DCI	HSTL_I_DCI_18	$T_{OHSTL\_I\_DCI\_18}$	0.05	0.05	0.06	ns
HSTL, Class II, 1.8V, with DCI	HSTL_II_DCI_18	$T_{OHSTL\_II\_DCI\_18}$	–0.03	–0.03	–0.03	ns
HSTL, Class III, 1.8V, with DCI	HSTL_III_DCI_18	$T_{OHSTL\_III\_DCI\_18}$	–0.14	–0.14	–0.16	ns
HSTL, Class IV, 1.8V, with DCI	HSTL_IV_DCI_18	$T_{OHSTL\_IV\_DCI\_18}$	–0.41	–0.42	–0.47	ns
SSTL (Stub Series Terminated Logic), Class I, 1.8V, with DCI	SSTL18_I_DCI	$T_{OSSTL18\_I\_DCI}$	0.36	0.37	0.40	ns
SSTL, Class II, 1.8V, with DCI	SSTL18_II_DCI	$T_{OSSTL18\_II\_DCI}$	0.06	0.06	0.07	ns
SSTL, Class I, 2.5V, with DCI	SSTL2_I_DCI	$T_{OSSTL2\_I\_DCI}$	0.12	0.13	0.14	ns
SSTL, Class II, 2.5V, with DCI	SSTL2_II_DCI	$T_{OSSTL2\_II\_DCI}$	–0.10	–0.10	–0.11	ns
SSTL, Class I, 3.3V, with DCI	SSTL3_I_DCI	$T_{OSSTL3\_I\_DCI}$	0.15	0.16	0.17	ns
SSTL, Class II, 3.3V, with DCI	SSTL3_II_DCI	$T_{OSSTL3\_II\_DCI}$	0.08	0.08	0.09	ns

Virtex-II Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *With* DCM

Table 34: **Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *With* DCM**

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
LVTTL Global Clock Input to Output delay using Output flip-flop, 12 mA, Fast Slew Rate, *with* DCM. For data *output* with different standards, adjust the delays with the values shown in IOB Output Switching Characteristics Standard Adjustments, page 14.						
Global Clock and OFF with DCM	$T_{ICKOFDCM}$	XC2V40	1.10	1.28	1.48	ns
		XC2V80	1.10	1.28	1.48	ns
		XC2V250	1.10	1.28	1.48	ns
		XC2V500	1.10	1.28	1.48	ns
		XC2V1000	1.10	1.28	1.48	ns
		XC2V1500	1.10	1.28	1.48	ns
		XC2V2000	1.10	1.28	1.48	ns
		XC2V3000	1.19	1.38	1.59	ns
		XC2V4000	1.19	1.38	1.59	ns
		XC2V6000	1.64	1.88	2.17	ns
		XC2V8000		1.88	2.17	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with test setup shown in Figure 1. For other I/O standards, see Table 19.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *Without* DCM

Table 35: **Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *Without* DCM**

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
LVTTL Global Clock Input to Output Delay using Output flip-flop, 12 mA, Fast Slew Rate, *without* DCM. For data *output* with different standards, adjust the delays with the values shown in IOB Output Switching Characteristics Standard Adjustments, page 14.						
Global Clock and OFF without DCM	T_{ICKOF}	XC2V40	3.46	3.58	3.69	ns
		XC2V80	3.62	3.58	3.69	ns
		XC2V250	3.79	3.88	4.47	ns
		XC2V500	3.85	3.88	4.47	ns
		XC2V1000	4.02	4.28	4.62	ns
		XC2V1500	4.16	4.28	4.62	ns
		XC2V2000	4.30	4.43	5.10	ns
		XC2V3000	4.49	4.64	5.34	ns
		XC2V4000	4.82	4.99	5.74	ns
		XC2V6000	5.19	5.38	5.93	ns
		XC2V8000		6.09	7.00	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with test setup shown in Figure 1. For other I/O standards, see Table 19.

Virtex-II Platform FPGAs: Pinout Information

DS031-4 (v3.5) November 5, 2007

Product Specification

This document provides Virtex-II™ Device/Package Combinations, Maximum I/Os Available, and Virtex-II Pin Definitions, followed by pinout tables for the following packages:

- CS144/CSG144 Chip-Scale BGA Package
- FG256/FGG256 Fine-Pitch BGA Package
- FG456/FGG456 Fine-Pitch BGA Package
- FG676/FGG676 Fine-Pitch BGA Package
- BG575/BGG575 Standard BGA Package
- BG728/BGG728 Standard BGA Package
- FF896 Flip-Chip Fine-Pitch BGA Package
- FF1152 Flip-Chip Fine-Pitch BGA Package
- FF1517 Flip-Chip Fine-Pitch BGA Package
- BF957 Flip-Chip BGA Package

For device pinout diagrams and layout guidelines, refer to the ***Virtex-II Platform FPGA User Guide***. ASCII package pinout files are also available for download from the Xilinx website (**www.xilinx.com**).

Virtex-II Device/Package Combinations and Maximum I/Os Available

Wire-bond and flip-chip packages are available. Table 1 and Table 2 show the maximum number of user I/Os possible in wire-bond and flip-chip packages, respectively.

Table 3 shows the number of user I/Os available for all device/package combinations.

- CS denotes wire-bond chip-scale ball grid array (BGA) (0.80 mm pitch).
- CSG denotes Pb-free wire-bond chip-scale ball grid array (BGA) (0.80 mm pitch).
- FG denotes wire-bond fine-pitch BGA (1.00 mm pitch).
- FGG denotes Pb-free wire-bond fine-pitch BGA (1.00 mm pitch).
- BG denotes standard BGA (1.27 mm pitch).
- BGG denotes Pb-free standard BGA (1.27 mm pitch).
- FF denotes flip-chip fine-pitch BGA (1.00 mm pitch).
- BF denotes flip-chip BGA (1.27 mm pitch).

The number of I/Os per package include all user I/Os except the 15 control pins (CCLK, DONE, M0, M1, M2, PROG_B, PWRDWN_B, TCK, TDI, TDO, TMS, HSWAP_EN, DXN, DXP, AND RSVD).

Table 1: **Wire-Bond Packages Information**

Package[1]	CS144/ CSG144	FG256/ FGG256	FG456/ FGG456	FG676/ FGG676	BG575/ BGG575	BG728/ BGG728
Pitch (mm)	0.80	1.00	1.00	1.00	1.27	1.27
Size (mm)	12 x 12	17 x 17	23 x 23	27 x 27	31 x 31	35 x 35
I/Os	92	172	324	484	408	516

Notes:
1. Wire-bond packages include FGG*nnn* Pb-free versions. See Virtex-II Ordering Examples (Module 1).

Table 2: **Flip-Chip Packages Information**

Package	FF896	FF1152	FF1517	BF957
Pitch (mm)	1.00	1.00	1.00	1.27
Size (mm)	31 x 31	35 x 35	40 x 40	40 x 40
I/Os	624	824	1,108	684

Table 4: **Virtex-II Pin Definitions *(Continued)***

Pin Name	Direction	Description
PROG_B	Input	Active Low asynchronous reset to configuration logic. This pin has a permanent weak pull-up resistor.
DONE	Input/Output	DONE is a bidirectional signal with an optional internal pull-up resistor. As an output, this pin indicates completion of the configuration process. As an input, a Low level on DONE can be configured to delay the start-up sequence.
M2, M1, M0	Input	Configuration mode selection.
HSWAP_EN	Input	Enable I/O pull-ups during configuration.
TCK	Input	Boundary Scan Clock.
TDI	Input	Boundary Scan Data Input.
TDO	Output	Boundary Scan Data Output.
TMS	Input	Boundary Scan Mode Select.
PWRDWN_B	Input *(unsupported)*	Active Low power-down pin (unsupported). *Driving this pin Low can adversely affect device operation and configuration.* PWRDWN_B is internally pulled High, which is its default state. It does not require an external pull-up.
Other Pins		
DXN, DXP	N/A	Temperature-sensing diode pins (Anode: DXP, Cathode: DXN).
V_{BATT}	Input	Decryptor key memory backup supply. Connect V_{BATT} to V_{CCAUX} or GND if battery is not used.
RSVD	N/A	Reserved pin - do not connect.
V_{CCO}	Input	Power-supply pins for the output drivers (per bank).
V_{CCAUX}	Input	Power-supply pins for auxiliary circuits.
V_{CCINT}	Input	Power-supply pins for the internal core logic.
GND	Input	Ground.

Notes:
1. All dedicated pins (JTAG and configuration) are powered by V_{CCAUX} (independent of the bank V_{CCO} voltage).

Table 5: **CS144/CSG144 — XC2V40, XC2V80, and XC2V250**

Bank	Pin Description	Pin Number	No Connect in the XC2V40
6	IO_L01P_6	L3	
6	IO_L01N_6	L2	
6	IO_L02P_6/VRN_6	L1	
6	IO_L02N_6/VRP_6	K3	
6	IO_L03P_6	K2	
6	IO_L03N_6/VREF_6	K1	
6	IO_L94P_6	J2	
6	IO_L94N_6	H4	
6	IO_L96P_6	H3	
6	IO_L96N_6	H1	
7	IO_L96P_7	G4	
7	IO_L96N_7	G3	
7	IO_L94P_7	G1	
7	IO_L94N_7	F1	
7	IO_L93P_7/VREF_7	F2	NC
7	IO_L93N_7	F4	NC
7	IO_L03P_7/VREF_7	E2	
7	IO_L03N_7	E3	
7	IO_L02P_7/VRN_7	E4	
7	IO_L02N_7/VRP_7	D1	
7	IO_L01P_7	D2	
7	IO_L01N_7	D3	
0	VCCO_0	B5	
0	VCCO_0	C3	
1	VCCO_1	A11	
1	VCCO_1	A9	
2	VCCO_2	F10	
2	VCCO_2	C12	
3	VCCO_3	L12	
3	VCCO_3	J12	
4	VCCO_4	M9	
4	VCCO_4	L11	
5	VCCO_5	N3	
5	VCCO_5	N5	
6	VCCO_6	J3	
6	VCCO_6	M1	
7	VCCO_7	D4	
7	VCCO_7	F3	

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
1	IO_L70N_1	B15	NC	
1	IO_L70P_1	C15	NC	
1	IO_L69N_1/VREF_1	E15	NC	
1	IO_L69P_1	F15	NC	
1	IO_L67N_1	G15	NC	
1	IO_L67P_1	H15	NC	
1	IO_L54N_1	B16		
1	IO_L54P_1	C16		
1	IO_L52N_1	D16		
1	IO_L52P_1	E16		
1	IO_L51N_1/VREF_1	F16		
1	IO_L51P_1	G16		
1	IO_L49N_1	A17		
1	IO_L49P_1	A19		
1	IO_L24N_1	B17		
1	IO_L24P_1	B18		
1	IO_L22N_1	C17		
1	IO_L22P_1	D17		
1	IO_L21N_1/VREF_1	F17		
1	IO_L21P_1	E17		
1	IO_L19N_1	A20		
1	IO_L19P_1	A21		
1	IO_L06N_1	B19		
1	IO_L06P_1	B20		
1	IO_L05N_1	C18		
1	IO_L05P_1	D18		
1	IO_L04N_1	C20		
1	IO_L04P_1/VREF_1	D20		
1	IO_L03N_1/VRP_1	D19		
1	IO_L03P_1/VRN_1	E19		
1	IO_L02N_1	E18		
1	IO_L02P_1	F18		
1	IO_L01N_1	H16		
1	IO_L01P_1	G17		
2	IO_L01N_2	D22		

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
4	IO_L94P_4	AE14
4	IO_L95N_4/GCLK3S	AF15
4	IO_L95P_4/GCLK2P	AG15
4	IO_L96N_4/GCLK1S	Y14
4	IO_L96P_4/GCLK0P	AA14
5	IO_L96N_5/GCLK7S	AC14
5	IO_L96P_5/GCLK6P	AB14
5	IO_L95N_5/GCLK5S	AG13
5	IO_L95P_5/GCLK4P	AF13
5	IO_L94N_5	AE13
5	IO_L94P_5/VREF_5	AD13
5	IO_L93N_5	AC13
5	IO_L93P_5	AB13
5	IO_L92N_5	AA13
5	IO_L92P_5	Y13
5	IO_L91N_5	W13
5	IO_L91P_5/VREF_5	W12
5	IO_L78N_5	AG12
5	IO_L78P_5	AF12
5	IO_L76N_5	AD12
5	IO_L76P_5	AC12
5	IO_L75N_5/VREF_5	AB12
5	IO_L75P_5	AB11
5	IO_L73N_5	Y12
5	IO_L73P_5	Y11
5	IO_L72N_5	AG11
5	IO_L72P_5	AF11
5	IO_L70N_5	AE11
5	IO_L70P_5	AD11
5	IO_L69N_5/VREF_5	AA10
5	IO_L69P_5	AA11
5	IO_L67N_5	AG10
5	IO_L67P_5	AF10
5	IO_L54N_5	AE10
5	IO_L54P_5	AD10

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
NA	VCCAUX	P26
NA	VCCAUX	P2
NA	VCCAUX	C26
NA	VCCAUX	C2
NA	VCCAUX	B14
NA	VCCINT	V18
NA	VCCINT	V14
NA	VCCINT	V10
NA	VCCINT	U17
NA	VCCINT	U16
NA	VCCINT	U15
NA	VCCINT	U14
NA	VCCINT	U13
NA	VCCINT	U12
NA	VCCINT	U11
NA	VCCINT	T17
NA	VCCINT	T11
NA	VCCINT	R17
NA	VCCINT	R11
NA	VCCINT	P18
NA	VCCINT	P17
NA	VCCINT	P11
NA	VCCINT	P10
NA	VCCINT	N17
NA	VCCINT	N11
NA	VCCINT	M17
NA	VCCINT	M11
NA	VCCINT	L17
NA	VCCINT	L16
NA	VCCINT	L15
NA	VCCINT	L14
NA	VCCINT	L13
NA	VCCINT	L12
NA	VCCINT	L11
NA	VCCINT	K18
NA	VCCINT	K14

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
7	IO_L95N_7	R24		
7	IO_L94P_7	R29		
7	IO_L94N_7	T29		
7	IO_L93P_7/VREF_7	R27		
7	IO_L93N_7	P27		
7	IO_L92P_7	R23		
7	IO_L92N_7	P23		
7	IO_L91P_7	N30		
7	IO_L91N_7	P30		
7	IO_L78P_7	P26	NC	NC
7	IO_L78N_7	R26	NC	NC
7	IO_L77P_7	R22	NC	NC
7	IO_L77N_7	P22	NC	NC
7	IO_L76P_7	N29	NC	NC
7	IO_L76N_7	P29	NC	NC
7	IO_L75P_7/VREF_7	N27	NC	NC
7	IO_L75N_7	N26	NC	NC
7	IO_L74P_7	P25	NC	NC
7	IO_L74N_7	N25	NC	NC
7	IO_L73P_7	L30	NC	NC
7	IO_L73N_7	M30	NC	NC
7	IO_L72P_7	L28	NC	
7	IO_L72N_7	M28	NC	
7	IO_L71P_7	N24	NC	
7	IO_L71N_7	M24	NC	
7	IO_L70P_7	L29	NC	
7	IO_L70N_7	M29	NC	
7	IO_L69P_7/VREF_7	M27	NC	
7	IO_L69N_7	L27	NC	
7	IO_L68P_7	N23	NC	
7	IO_L68N_7	M23	NC	
7	IO_L67P_7	J30	NC	
7	IO_L67N_7	K30	NC	
7	IO_L54P_7	K26		
7	IO_L54N_7	L26		
7	IO_L53P_7	M25		
7	IO_L53N_7	L25		

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
0	IO_L77N_0	J20	
0	IO_L77P_0	K19	
0	IO_L78N_0	D20	
0	IO_L78P_0	D21	
0	IO_L79N_0	A21	NC
0	IO_L79P_0	A22	NC
0	IO_L80N_0	L19	NC
0	IO_L80P_0	L18	NC
0	IO_L81N_0	B19	NC
0	IO_L81P_0/VREF_0	A20	NC
0	IO_L82N_0	A18	NC
0	IO_L82P_0	B18	NC
0	IO_L83N_0	H19	NC
0	IO_L83P_0	H18	NC
0	IO_L84N_0	C20	NC
0	IO_L84P_0	C21	NC
0	IO_L91N_0/VREF_0	D19	
0	IO_L91P_0	D18	
0	IO_L92N_0	G18	
0	IO_L92P_0	G19	
0	IO_L93N_0	F18	
0	IO_L93P_0	F19	
0	IO_L94N_0/VREF_0	C19	
0	IO_L94P_0	C18	
0	IO_L95N_0/GCLK7P	K18	
0	IO_L95P_0/GCLK6S	J18	
0	IO_L96N_0/GCLK5P	E19	
0	IO_L96P_0/GCLK4S	E18	
1	IO_L96N_1/GCLK3P	E17	
1	IO_L96P_1/GCLK2S	E16	
1	IO_L95N_1/GCLK1P	H17	
1	IO_L95P_1/GCLK0S	H16	
1	IO_L94N_1	D17	
1	IO_L94P_1/VREF_1	D16	
1	IO_L93N_1	F16	

FF1517 Flip-Chip Fine-Pitch BGA Package

As shown in Table 13, XC2V4000, XC2V6000, and XC2V8000 Virtex-II devices are available in the FF1517 flip-chip fine-pitch BGA package. Pins in each of these devices are the same, except for the pin differences in the XC2V4000 and XC2V6000 devices shown in the No Connect columns. Following this table are the FF1517 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
0	IO_L01N_0	B36		
0	IO_L01P_0	C36		
0	IO_L02N_0	J30		
0	IO_L02P_0	J29		
0	IO_L03N_0/VRP_0	D33		
0	IO_L03P_0/VRN_0	D34		
0	IO_L04N_0/VREF_0	C34		
0	IO_L04P_0	C35		
0	IO_L05N_0	H30		
0	IO_L05P_0	G30		
0	IO_L06N_0	D32		
0	IO_L06P_0	E33		
0	IO_L07N_0	A35	NC	
0	IO_L07P_0	A36	NC	
0	IO_L08N_0	K28	NC	
0	IO_L08P_0	J28	NC	
0	IO_L09N_0	E32	NC	
0	IO_L09P_0/VREF_0	F32	NC	
0	IO_L10N_0	B34	NC	
0	IO_L10P_0	B35	NC	
0	IO_L11N_0	H29	NC	
0	IO_L11P_0	H28	NC	
0	IO_L12N_0	F31	NC	
0	IO_L12P_0	G31	NC	
0	IO_L19N_0	C32		
0	IO_L19P_0	C33		
0	IO_L20N_0	M26		
0	IO_L20P_0	M25		
0	IO_L21N_0	E30		
0	IO_L21P_0/VREF_0	E31		
0	IO_L22N_0	A33		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
0	IO_L22P_0	A34		
0	IO_L23N_0	K27		
0	IO_L23P_0	K26		
0	IO_L24N_0	F29		
0	IO_L24P_0	F30		
0	IO_L25N_0	B32		
0	IO_L25P_0	B33		
0	IO_L26N_0	L26		
0	IO_L26P_0	L25		
0	IO_L27N_0	G28		
0	IO_L27P_0/VREF_0	G29		
0	IO_L28N_0	C30		
0	IO_L28P_0	C31		
0	IO_L29N_0	J27		
0	IO_L29P_0	J26		
0	IO_L30N_0	D30		
0	IO_L30P_0	D31		
0	IO_L31N_0	A31	NC	
0	IO_L31P_0	A32	NC	
0	IO_L32N_0	H27	NC	
0	IO_L32P_0	H26	NC	
0	IO_L33N_0	F27	NC	
0	IO_L33P_0/VREF_0	F28	NC	
0	IO_L34N_0	B30	NC	
0	IO_L34P_0	B31	NC	
0	IO_L35N_0	M24	NC	
0	IO_L35P_0	M23	NC	
0	IO_L36N_0	D28	NC	
0	IO_L36P_0	D29	NC	
0	IO_L49N_0	C28		
0	IO_L49P_0	C29		
0	IO_L50N_0	K25		
0	IO_L50P_0	L24		
0	IO_L51N_0	E27		
0	IO_L51P_0/VREF_0	E28		
0	IO_L52N_0	A29		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
3	IO_L10N_3	AK7	NC	
3	IO_L10P_3	AL7	NC	
3	IO_L09N_3/VREF_3	AK11	NC	
3	IO_L09P_3	AJ10	NC	
3	IO_L08N_3	AR1	NC	
3	IO_L08P_3	AT1	NC	
3	IO_L07N_3	AM5	NC	
3	IO_L07P_3	AN5	NC	
3	IO_L06N_3	AM7		
3	IO_L06P_3	AL8		
3	IO_L05N_3	AP3		
3	IO_L05P_3	AP4		
3	IO_L04N_3	AM6		
3	IO_L04P_3	AN6		
3	IO_L03N_3/VREF_3	AJ13		
3	IO_L03P_3	AH13		
3	IO_L02N_3/VRP_3	AR3		
3	IO_L02P_3/VRN_3	AT2		
3	IO_L01N_3	AP5		
3	IO_L01P_3	AR4		
4	IO_L01N_4/BUSY/DOUT(1)	AV4		
4	IO_L01P_4/INIT_B	AU4		
4	IO_L02N_4/D0/DIN(1)	AM9		
4	IO_L02P_4/D1	AM10		
4	IO_L03N_4/D2/ALT_VRP_4	AT6		
4	IO_L03P_4/D3/ALT_VRN_4	AR6		
4	IO_L04N_4/VREF_4	AU6		
4	IO_L04P_4	AU5		
4	IO_L05N_4/VRP_4	AL10		
4	IO_L05P_4/VRN_4	AL11		
4	IO_L06N_4	AR8		
4	IO_L06P_4	AR7		
4	IO_L07N_4	AW5	NC	
4	IO_L07P_4	AW4	NC	
4	IO_L08N_4	AK12	NC	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	GND	Y17		
NA	GND	Y16		
NA	GND	Y10		
NA	GND	Y7		
NA	GND	Y4		
NA	GND	Y1		
NA	GND	W24		
NA	GND	W23		
NA	GND	W22		
NA	GND	W21		
NA	GND	W20		
NA	GND	W19		
NA	GND	W18		
NA	GND	W17		
NA	GND	W16		
NA	GND	V24		
NA	GND	V23		
NA	GND	V22		
NA	GND	V21		
NA	GND	V20		
NA	GND	V19		
NA	GND	V18		
NA	GND	V17		
NA	GND	V16		
NA	GND	U36		
NA	GND	U32		
NA	GND	U24		
NA	GND	U23		
NA	GND	U22		
NA	GND	U21		
NA	GND	U20		
NA	GND	U19		
NA	GND	U18		
NA	GND	U17		
NA	GND	U16		
NA	GND	U8		

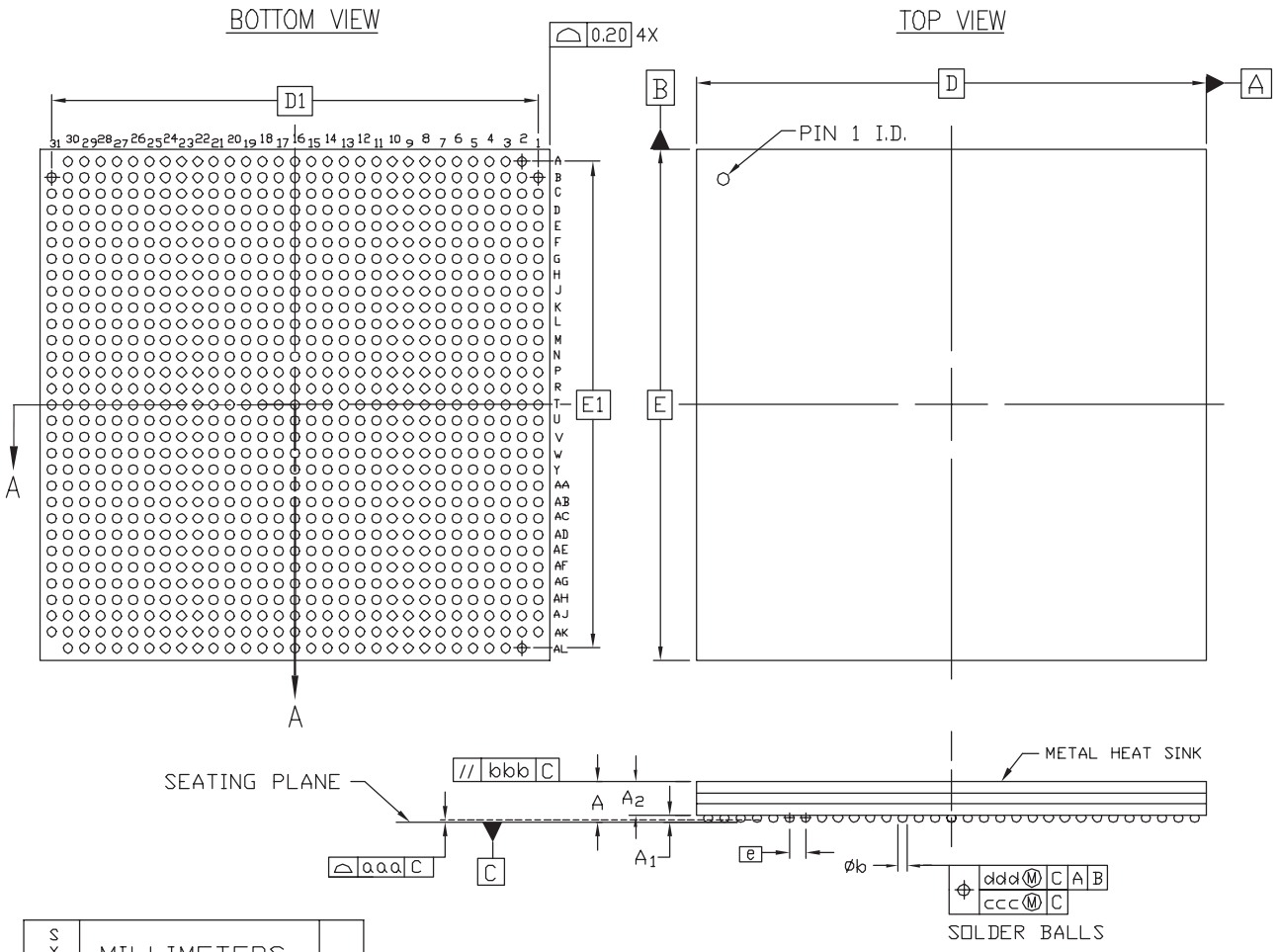
Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
0	IO_L49N_0	C23	
0	IO_L49P_0	C22	
0	IO_L50N_0	E22	
0	IO_L50P_0	E21	
0	IO_L51N_0	F21	
0	IO_L51P_0/VREF_0	F20	
0	IO_L52N_0	A24	
0	IO_L52P_0	A23	
0	IO_L53N_0	E20	
0	IO_L53P_0	E19	
0	IO_L54N_0	B22	
0	IO_L54P_0	B21	
0	IO_L67N_0	D21	
0	IO_L67P_0	D20	
0	IO_L68N_0	J20	
0	IO_L68P_0	J19	
0	IO_L69N_0	F19	
0	IO_L69P_0/VREF_0	F18	
0	IO_L70N_0	A22	
0	IO_L70P_0	A21	
0	IO_L71N_0	H19	
0	IO_L71P_0	H17	
0	IO_L72N_0	C21	
0	IO_L72P_0	C20	
0	IO_L73N_0	B20	
0	IO_L73P_0	B19	
0	IO_L74N_0	G18	
0	IO_L74P_0	G17	
0	IO_L75N_0	E18	
0	IO_L75P_0/VREF_0	D17	
0	IO_L76N_0	A20	
0	IO_L76P_0	A19	
0	IO_L77N_0	D19	
0	IO_L77P_0	D18	
0	IO_L78N_0	C19	
0	IO_L78P_0	C17	
0	IO_L91N_0/VREF_0	K18	
0	IO_L91P_0	J18	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
3	IO_L03P_3	AD7	
3	IO_L02N_3/VRP_3	AE6	
3	IO_L02P_3/VRN_3	AF5	
3	IO_L01N_3	AH2	
3	IO_L01P_3	AH3	
4	IO_L01N_4/BUSY/DOUT(1)	AD9	
4	IO_L01P_4/INIT_B	AD10	
4	IO_L02N_4/D0/DIN(1)	AF7	
4	IO_L02P_4/D1	AG7	
4	IO_L03N_4/D2/ALT_VRP_4	AK3	
4	IO_L03P_4/D3/ALT_VRN_4	AJ5	
4	IO_L04N_4/VREF_4	AE8	
4	IO_L04P_4	AF8	
4	IO_L05N_4/VRP_4	AK4	
4	IO_L05P_4/VRN_4	AK5	
4	IO_L06N_4	AH6	
4	IO_L06P_4	AH7	
4	IO_L19N_4	AC10	
4	IO_L19P_4	AC11	
4	IO_L20N_4	AE9	
4	IO_L20P_4	AE10	
4	IO_L21N_4	AL4	
4	IO_L21P_4/VREF_4	AL5	
4	IO_L22N_4	AB12	
4	IO_L22P_4	AB13	
4	IO_L23N_4	AJ6	
4	IO_L23P_4	AJ8	
4	IO_L24N_4	AK6	
4	IO_L24P_4	AK7	
4	IO_L25N_4	AG8	NC
4	IO_L25P_4	AG9	NC
4	IO_L26N_4	AF9	NC
4	IO_L26P_4	AF11	NC
4	IO_L27N_4	AH8	NC
4	IO_L27P_4/VREF_4	AH9	NC
4	IO_L28N_4	AD11	NC
4	IO_L28P_4	AD12	NC

BF957 Flip-Chip BGA Package Specifications (1.27mm pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	---	3.25	3.50	
A_1	0.50	0.60	0.70	
A_2	---	---	2.80	
A_3	0.20	---	---	
D/E	40.00 BSC			
D_1/E_1	38.10 REF.			
e	1.27 BSC			
øb	0.60	0.75	0.90	
aaa	---	---	0.20	
bbb	---	---	0.25	
ccc	---	---	0.15	
ddd	---	---	0.30	
M	31			

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–BAU–1 (DEPOPULATED)

Figure 10: **BF957 Flip-Chip BGA Package Specifications**