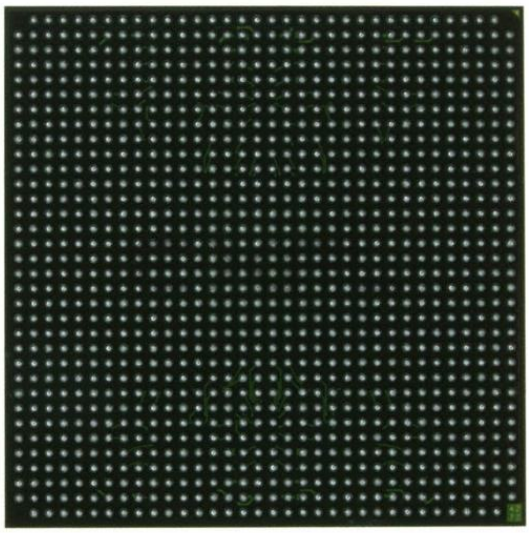

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	5760
Number of Logic Elements/Cells	-
Total RAM Bits	2211840
Number of I/O	824
Number of Gates	4000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v4000-4ffg1152c

Table 6: **Virtex-II Device/Package Combinations and Maximum Number of Available I/Os (Advance Information)**

Package(1,2)	Available I/Os										
	XC2V 40	XC2V 80	XC2V 250	XC2V 500	XC2V 1000	XC2V 1500	XC2V 2000	XC2V 3000	XC2V 4000	XC2V 6000	XC2V 8000
CS144/CSG144	88	92	92	-	-	-	-	-	-	-	-
FG256/FGG256	88	120	172	172	172	-	-	-	-	-	-
FG456/FGG456	-	-	200	264	324	-	-	-	-	-	-
FG676/FGG676	-	-	-	-	-	392	456	484	-	-	-
FF896	-	-	-	-	432	528	624	-	-	-	-
FF1152	-	-	-	-	-	-	-	720	824	824	824
FF1517	-	-	-	-	-	-	-	-	912	1,104	1,108
BG575/BGG575	-	-	-	-	328	392	408	-	-	-	-
BG728/BGG728	-	-	-	-	-	-	-	516	-	-	-
BF957	-	-	-	-	-	-	624	684	684	684	-

Notes:
1. All devices in a particular package are pinout (footprint) compatible. In addition, the FG456/FGG456 and FG676/FGG676 packages are compatible, as are the FF896 and FF1152 packages.
2. Wire-bond packages CS144, FG256, FG456, FG676, BG575, and BG728 are also available in Pb-free versions CSG144, FGG256, FGG456, FGG676, BGG575, and BGG728. See Virtex-II Ordering Examples for details on how to order.

Virtex-II Ordering Examples

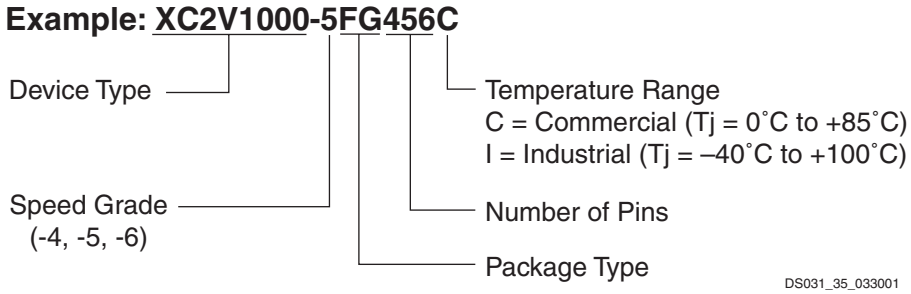

Figure 2: **Virtex-II Ordering Example. Regular Package**

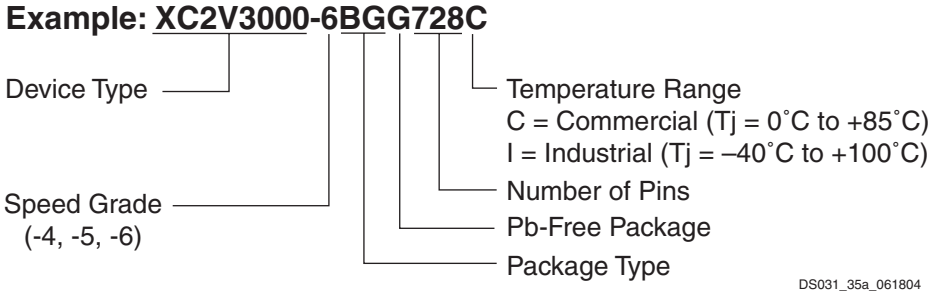

Figure 3: **Virtex-II Ordering Example. Pb-Free Package**

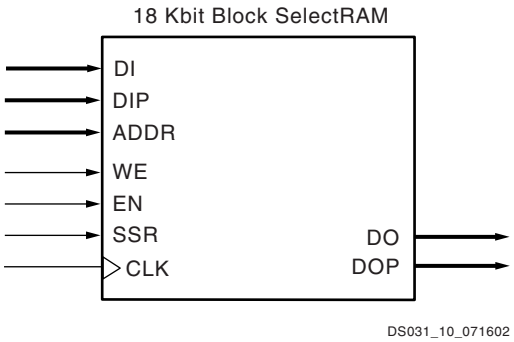

Figure 29: **18 Kbit Block SelectRAM Memory in Single-Port Mode**

Dual-Port Configuration

As a dual-port RAM, each port of block SelectRAM has access to a common 18 Kbit memory resource. These are fully synchronous ports with independent control signals for each port. The data widths of the two ports can be configured independently, providing built-in bus-width conversion.

Table 15 illustrates the different configurations available on ports A and B.

If both ports are configured in either 2K x 9-bit, 1K x 18-bit, or 512 x 36-bit configurations, the 18 Kbit block is accessible from port A or B. If both ports are configured in either 16K x 1-bit, 8K x 2-bit. or 4K x 4-bit configurations, the 16 K-bit block is accessible from Port A or Port B. All other configurations result in one port having access to an 18 Kbit memory block and the other port having access to a 16 K-bit subset of the memory block equal to 16 Kbits.

Table 15: **Dual-Port Mode Configurations**

Port A	16K x 1	16K x 1	16K x 1	16K x 1	16K x 1	16K x 1
Port B	16K x 1	8K x 2	4K x 4	2K x 9	1K x 18	512 x 36
Port A	8K x 2	8K x 2	8K x 2	8K x 2	8K x 2	
Port B	8K x 2	4K x 4	2K x 9	1K x 18	512 x 36	
Port A	4K x 4	4K x 4	4K x 4	4K x 4		
Port B	4K x 4	2K x 9	1K x 18	512 x 36		
Port A	2K x 9	2K x 9	2K x 9			
Port B	2K x 9	1K x 18	512 x 36			
Port A	1K x 18	1K x 18				
Port B	1K x 18	512 x 36				
Port A	512 x 36					
Port B	512 x 36					

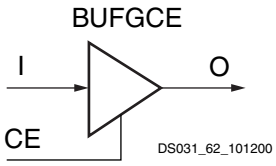

Figure 42: **Virtex-II BUFGCE Function**

If the CE input is inactive (Low) prior to the incoming rising clock edge, the following clock pulse does not pass through the clock buffer, and the output stays Low. Any level change of CE during the incoming clock High time has no effect. CE must not change during a short setup window just prior to the rising clock edge on the BUFGCE input I. Violating this setup time requirement can result in an undefined runt pulse output.

BUFGMUX

BUFGMUX can switch between two unrelated, even asynchronous clocks. Basically, a Low on S selects the I0 input, a High on S selects the I1 input. Switching from one clock to the other is done in such a way that the output High and Low time is never shorter than the shortest High or Low time of either input clock. As long as the presently selected clock is High, any level change of S has no effect .

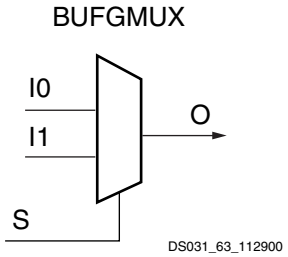

Figure 43: **Virtex-II BUFGMUX Function**

If the presently selected clock is Low while S changes, or if it goes Low after S has changed, the output is kept Low until the other ("to-be-selected") clock has made a transition from High to Low. At that instant, the new clock starts driving the output.

The two clock inputs can be asynchronous with regard to each other, and the S input can change at any time, except for a short setup time prior to the rising edge of the presently selected clock (I0 or I1). Violating this setup time requirement can result in an undefined runt pulse output.

All Virtex-II devices have 16 global clock multiplexer buffers.

Figure 44 shows a switchover from I0 to I1.

- The current clock is CLK0.
- S is activated High.
- If CLK0 is currently High, the multiplexer waits for CLK0 to go Low.
- Once CLK0 is Low, the multiplexer output stays Low until CLK1 transitions High to Low.
- When CLK1 transitions from High to Low, the output switches to CLK1.
- No glitches or short pulses can appear on the output.

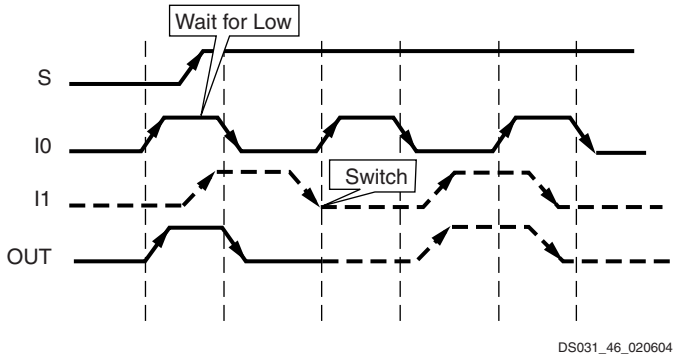

Figure 44: **Clock Multiplexer Waveform Diagram**

Local Clocking

In addition to global clocks, there are local clock resources in the Virtex-II devices. There are more than 72 local clocks in the Virtex-II family. These resources can be used for many different applications, including but not limited to memory interfaces. For example, even using only the left and right I/O banks, Virtex-II FPGAs can support up to 50 local clocks for DDR SDRAM. These interfaces can operate beyond 200 MHz on Virtex-II devices.

Digital Clock Manager (DCM)

The Virtex-II DCM offers a wide range of powerful clock management features.

- **Clock De-skew**: The DCM generates new system clocks (either internally or externally to the FPGA), which are phase-aligned to the input clock, thus eliminating clock distribution delays.
- **Frequency Synthesis**: The DCM generates a wide range of output clock frequencies, performing very flexible clock multiplication and division.
- **Phase Shifting**: The DCM provides both coarse phase shifting and fine-grained phase shifting with dynamic phase shift control.

The DCM utilizes fully digital delay lines allowing robust high-precision control of clock phase and frequency. It also utilizes fully digital feedback systems, operating dynamically to compensate for temperature and voltage variations during operation.

Up to four of the nine DCM clock outputs can drive inputs to global clock buffers or global clock multiplexer buffers simultaneously (see Figure 45). All DCM clock outputs can simultaneously drive general routing resources, including routes to output buffers.

Virtex-II FPGA device. Timing is similar to the Slave Serial-MAP mode except that CCLK is supplied by the Virtex-II FPGA.

Boundary-Scan (JTAG, IEEE 1532) Mode

In Boundary-Scan mode, dedicated pins are used for configuring the Virtex-II device. The configuration is done entirely through the IEEE 1149.1 Test Access Port (TAP). Virtex-II device configuration using Boundary-Scan is compatible with the IEEE 1149.1-1993 standard and the new IEEE 1532 standard for In-System Configurable (ISC) devices. The IEEE 1532 standard is backward compliant with the IEEE 1149.1-1993 TAP and state machine. The IEEE Standard 1532 for In-System Configurable (ISC) devices is intended to be programmed, reprogrammed, or tested on the board via a physical and logical protocol.

Configuration through the Boundary-Scan port is always available, independent of the mode selection. Selecting the Boundary-Scan mode simply turns off the other modes.

Table 25: **Virtex-II Configuration Mode Pin Settings**

Configuration Mode(1)	M2	M1	M0	CCLK Direction	Data Width	Serial D_{OUT}(2)
Master Serial	0	0	0	Out	1	Yes
Slave Serial	1	1	1	In	1	Yes
Master SelectMAP	0	1	1	Out	8	No
Slave SelectMAP	1	1	0	In	8	No
Boundary-Scan	1	0	1	N/A	1	No

Notes:
1. The HSWAP_EN pin controls the pull-ups. Setting M2, M1, and M0 selects the configuration mode, while the HSWAP_EN pin controls whether or not the pull-ups are used.
2. Daisy chaining is possible only in modes where Serial D_{OUT} is used. For example, in SelectMAP modes, the first device does NOT support daisy chaining of downstream devices.

Table 26 lists the total number of bits required to configure each device.

Table 26: **Virtex-II Bitstream Lengths**

Device	# of Configuration Bits
XC2V40	338,976
XC2V80	598,816
XC2V250	1,593,632
XC2V500	2,560,544
XC2V1000	4,082,592
XC2V1500	5,170,208
XC2V2000	6,812,960
XC2V3000	10,494,368
XC2V4000	15,659,936
XC2V6000	21,849,504
XC2V8000	26,194,208

Configuration Sequence

The configuration of Virtex-II devices is a three-phase process after Power On Reset or POR. POR occurs when V_{CCINT} is greater than 1.2V, V_{CCAUX} is greater than 2.5V, and V_{CCO} (bank 4) is greater than 1.5V. Once the POR voltages have been reached, the three-phase process begins.

First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process.

Configuration is automatically initiated on power-up unless it is delayed by the user. The INIT_B pin can be held Low using an open-drain driver. An open-drain is required since INIT_B is a bidirectional open-drain pin that is held Low by a Virtex-II FPGA device while the configuration memory is being cleared. Extending the time that the pin is Low causes the configuration sequencer to wait. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

The configuration process can also be initiated by asserting the PROG_B pin. The end of the memory-clearing phase is signaled by the INIT_B pin going High, and the completion of the entire process is signaled by the DONE pin going High. The Global Set/Reset (GSR) signal is pulsed after the last frame of configuration data is written but before the start-up sequence. The GSR signal resets all flip-flops on the device.

The default start-up sequence is that one CCLK cycle after DONE goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary. One CCLK cycle later, the Global Write Enable (GWE) signal is released. This permits the internal storage ele-

Notice of Disclaimer

Virtex-II Data Sheet

The Virtex-II Data Sheet contains the following modules:

- Virtex-II Platform FPGAs: Introduction and Overview (Module 1)
- Virtex-II Platform FPGAs: Functional Description (Module 2)
- Virtex-II Platform FPGAs: DC and Switching Characteristics (Module 3)
- Virtex-II Platform FPGAs: Pinout Information (Module 4)

Table 5: **Minimum Power On Current Required for Virtex-II Devices**

	Device (mA)							
	XC2V40, XC2V80, XC2V250, XC2V500	XC2V1000	XC2V1500	XC2V2000	XC2V3000	XC2V4000	XC2V6000	XC2V8000
$I_{CCINTMIN}$	200	250	350	400	500	650	800	1100
$I_{CCAUXMIN}$	100	100	100	100	100	100	100	100
I_{CCOMIN}	50	50	100	100	100	100	100	100

Notes:
1. Values specified for power on current parameters are Commercial Grade. For Industrial Grade values, multiply Commercial Grade values by 1.25.
2. I_{CCOMIN} values listed here apply to the entire device (all banks).

General Power Supply Requirements

Proper decoupling of all FPGA power supplies is sessential. Consult Xilinx Application Note **XAPP623** for detailed information on power distribution system design.

V_{CCAUX} powers critical resources in the FPGA. Thus, V_{CCAUX} is especially susceptible to power supply noise.

Changes in V_{CCAUX} voltage outside of 200 mV peak to peak should take place at a rate no faster than 10 mV per millisecond. Techniques to help reduce jitter and period distortion are provided in Xilinx Answer Record 13756, available at **www.support.xilinx.com**.

V_{CCAUX} can share a power plane with 3.3V V_{CCO}, but only if V_{CCO} does not have excessive noise. Using simultaneously switching output (SSO) limits are essential for keeping power supply noise to a minimum. Refer to **XAPP689**, "Managing Ground Bounce in Large FPGAs," to determine the number of simultaneously switching outputs allowed per bank at the package level.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 6: **DC Input and Output Levels**

Input/Output	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
Standard	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTL(1)	– 0.5	0.8	2.0	3.6	0.4	2.4	24	– 24
LVCMOS33	– 0.5	0.8	2.0	3.6	0.4	V_{CCO} – 0.4	24	– 24
LVCMOS25	– 0.5	0.7	1.7	2.7	0.4	V_{CCO} – 0.4	24	– 24
LVCMOS18	– 0.5	35% V_{CCO}	65% V_{CCO}	1.95	0.4	V_{CCO} – 0.4	16	– 16
LVCMOS15	– 0.5	35% V_{CCO}	65% V_{CCO}	1.7	0.4	V_{CCO} – 0.4	16	– 16
PCI33_3	– 0.5	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
PCI66_3	– 0.5	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
PCI–X	– 0.5	Note 2	Note 2	Note 2	Note 2	Note 2	Note 2	Note 2
GTLP	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.5	0.6	n/a	36	n/a
GTL	– 0.5	V_{REF} – 0.05	V_{REF} + 0.05	V_{CCO} + 0.5	0.4	n/a	40	n/a
HSTL I	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.5	0.4	V_{CCO} – 0.4	8	– 8
HSTL II	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.5	0.4	V_{CCO} – 0.4	16	– 16
HSTL III	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.5	0.4	V_{CCO} – 0.4	24	– 8
HSTL IV	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.5	0.4	V_{CCO} – 0.4	48	– 8

FG256/FGG256 Fine-Pitch BGA Package

As shown in Table 6, XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000 Virtex-II devices are available in the FG256/FGG256 fine-pitch BGA package. The pins in the XC2V250, XC2V500, and XC2V1000 devices are same. The No Connect columns show pin differences for the XC2V40 and XC2V80 devices. Following this table are the FG256/FGG256 Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 6: **FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
0	IO_L01N_0	C4		
0	IO_L01P_0	B4		
0	IO_L02N_0	D5		
0	IO_L02P_0	C5		
0	IO_L03N_0/VRP_0	B5		
0	IO_L03P_0/VRN_0	A5		
0	IO_L04N_0/VREF_0	D6	NC	NC
0	IO_L04P_0	C6	NC	NC
0	IO_L05N_0	B6	NC	NC
0	IO_L05P_0	A6	NC	NC
0	IO_L92N_0	E6	NC	NC
0	IO_L92P_0	E7	NC	NC
0	IO_L93N_0	D7	NC	NC
0	IO_L93P_0	C7	NC	NC
0	IO_L94N_0/VREF_0	B7		
0	IO_L94P_0	A7		
0	IO_L95N_0/GCLK7P	D8		
0	IO_L95P_0/GCLK6S	C8		
0	IO_L96N_0/GCLK5P	B8		
0	IO_L96P_0/GCLK4S	A8		
1	IO_L96N_1/GCLK3P	A9		
1	IO_L96P_1/GCLK2S	B9		
1	IO_L95N_1/GCLK1P	C9		
1	IO_L95P_1/GCLK0S	D9		
1	IO_L94N_1	A10		
1	IO_L94P_1/VREF_1	B10		
1	IO_L93N_1	C10	NC	NC
1	IO_L93P_1	D10	NC	NC
1	IO_L92N_1	E10	NC	NC

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
2	IO_L45N_2	H19		
2	IO_L45P_2/VREF_2	H20		
2	IO_L46N_2	H21		
2	IO_L46P_2	H22		
2	IO_L48N_2	J17		
2	IO_L48P_2	J18		
2	IO_L49N_2	J19	NC	
2	IO_L49P_2	J20	NC	
2	IO_L51N_2	J21	NC	
2	IO_L51P_2/VREF_2	J22	NC	
2	IO_L52N_2	K17	NC	
2	IO_L52P_2	K18	NC	
2	IO_L54N_2	K19	NC	
2	IO_L54P_2	K20	NC	
2	IO_L91N_2	K21		
2	IO_L91P_2	K22		
2	IO_L93N_2	L17		
2	IO_L93P_2/VREF_2	L18		
2	IO_L94N_2	L19		
2	IO_L94P_2	L20		
2	IO_L96N_2	L21		
2	IO_L96P_2	L22		
3	IO_L96N_3	M21		
3	IO_L96P_3	M20		
3	IO_L94N_3	M19		
3	IO_L94P_3	M18		
3	IO_L93N_3/VREF_3	M17		
3	IO_L93P_3	N17		
3	IO_L91N_3	N22		
3	IO_L91P_3	N21		
3	IO_L54N_3	N20	NC	
3	IO_L54P_3	N19	NC	
3	IO_L52N_3	N18	NC	

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
7	IO_L51N_7	J2	NC	
7	IO_L49P_7	J3	NC	
7	IO_L49N_7	J4	NC	
7	IO_L48P_7	H1		
7	IO_L48N_7	H2		
7	IO_L46P_7	H3		
7	IO_L46N_7	H4		
7	IO_L45P_7/VREF_7	J6		
7	IO_L45N_7	H5		
7	IO_L43P_7	G1		
7	IO_L43N_7	G2		
7	IO_L24P_7	G3	NC	NC
7	IO_L24N_7	G4	NC	NC
7	IO_L22P_7	F1	NC	NC
7	IO_L22N_7	F2	NC	NC
7	IO_L21P_7/VREF_7	F3	NC	NC
7	IO_L21N_7	F4	NC	NC
7	IO_L19P_7	G5	NC	NC
7	IO_L19N_7	F5	NC	NC
7	IO_L06P_7	E1		
7	IO_L06N_7	E2		
7	IO_L04P_7	E3		
7	IO_L04N_7	E4		
7	IO_L03P_7/VREF_7	D1		
7	IO_L03N_7	D2		
7	IO_L02P_7/VRN_7	C1		
7	IO_L02N_7/VRP_7	C2		
7	IO_L01P_7	E5		
7	IO_L01N_7	E6		
0	VCCO_0	G11		
0	VCCO_0	G10		
0	VCCO_0	G9		
0	VCCO_0	F8		

FG676/FGG676 Fine-Pitch BGA Package

As shown in Table 8, XC2V1500, XC2V2000, and XC2V3000 Virtex-II devices are available in the FG676/FGG676 fine-pitch BGA package. Pins in the XC2V1500, XC2V2000, and XC2V3000 devices are the same, except for the pin differences in the XC2V1500 and XC2V2000 devices shown in the No Connect columns. Following this table are the FG676/FGG676 Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
0	IO_L01N_0	D6		
0	IO_L01P_0	C6		
0	IO_L02N_0	B1		
0	IO_L02P_0	A2		
0	IO_L03N_0/VRP_0	D7		
0	IO_L03P_0/VRN_0	C7		
0	IO_L04N_0/VREF_0	B3		
0	IO_L04P_0	A3		
0	IO_L05N_0	G6		
0	IO_L05P_0	G7		
0	IO_L06N_0	E6		
0	IO_L06P_0	E7		
0	IO_L19N_0	B4		
0	IO_L19P_0	A4		
0	IO_L21N_0	B5		
0	IO_L21P_0/VREF_0	A5		
0	IO_L22N_0	B6		
0	IO_L22P_0	A6		
0	IO_L24N_0	A7		
0	IO_L24P_0	A8		
0	IO_L25N_0	E8	NC	NC
0	IO_L25P_0	D8	NC	NC
0	IO_L27N_0	G8	NC	NC
0	IO_L27P_0/VREF_0	F8	NC	NC
0	IO_L49N_0	C8		
0	IO_L49P_0	B8		
0	IO_L51N_0	D9		
0	IO_L51P_0/VREF_0	E9		
0	IO_L52N_0	F9		
0	IO_L52P_0	G9		
0	IO_L54N_0	B9		
0	IO_L54P_0	A9		
0	IO_L67N_0	C9		

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
2	IO_L45N_2	H23		
2	IO_L45P_2/VREF_2	H24		
2	IO_L46N_2	J21		
2	IO_L46P_2	J20		
2	IO_L48N_2	H25		
2	IO_L48P_2	H26		
2	IO_L49N_2	J22		
2	IO_L49P_2	J23		
2	IO_L51N_2	K21		
2	IO_L51P_2/VREF_2	K22		
2	IO_L52N_2	K20		
2	IO_L52P_2	L20		
2	IO_L54N_2	J24		
2	IO_L54P_2	J25		
2	IO_L67N_2	K23		
2	IO_L67P_2	K24		
2	IO_L69N_2	J26		
2	IO_L69P_2/VREF_2	K26		
2	IO_L70N_2	L22		
2	IO_L70P_2	L21		
2	IO_L72N_2	L25		
2	IO_L72P_2	L26		
2	IO_L73N_2	L19	NC	
2	IO_L73P_2	M19	NC	
2	IO_L75N_2	L23	NC	
2	IO_L75P_2/VREF_2	L24	NC	
2	IO_L76N_2	M22	NC	
2	IO_L76P_2	M21	NC	
2	IO_L78N_2	M23	NC	
2	IO_L78P_2	M24	NC	
2	IO_L91N_2	M25		
2	IO_L91P_2	M26		
2	IO_L93N_2	M20		
2	IO_L93P_2/VREF_2	N20		
2	IO_L94N_2	N22		
2	IO_L94P_2	N21		
2	IO_L96N_2	N24		

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
4	IO_L02P_4/D1	AB20		
4	IO_L03N_4/D2/ALT_VRP_4	Y19		
4	IO_L03P_4/D3/ALT_VRN_4	AA19		
4	IO_L04N_4/VREF_4	W18		
4	IO_L04P_4	Y18		
4	IO_L05N_4/VRP_4	U16		
4	IO_L05P_4/VRN_4	V17		
4	IO_L06N_4	AD20		
4	IO_L06P_4	AD19		
4	IO_L19N_4	AC20		
4	IO_L19P_4	AC19		
4	IO_L21N_4	AA18		
4	IO_L21P_4/VREF_4	AB18		
4	IO_L22N_4	AC18		
4	IO_L22P_4	AC17		
4	IO_L24N_4	AA17		
4	IO_L24P_4	AB17		
4	IO_L49N_4	Y17		
4	IO_L49P_4	W17		
4	IO_L51N_4	V16		
4	IO_L51P_4/VREF_4	W16		
4	IO_L52N_4	AD17		
4	IO_L52P_4	AD16		
4	IO_L54N_4	AB16		
4	IO_L54P_4	AC16		
4	IO_L67N_4	Y16	NC	
4	IO_L67P_4	AA16	NC	
4	IO_L69N_4	W15	NC	
4	IO_L69P_4/VREF_4	Y15	NC	
4	IO_L70N_4	U15	NC	
4	IO_L70P_4	V15	NC	
4	IO_L72N_4	AD15	NC	
4	IO_L72P_4	AD14	NC	
4	IO_L73N_4	AB15	NC	NC
4	IO_L73P_4	AC15	NC	NC
4	IO_L91N_4/VREF_4	AA14		

BG728/BGG728 Standard BGA Package

As shown in Table 10, XC2V3000 Virtex-II devices are available in the BG728/BGG728 BGA package. Following this table are the BG728/BGG728 Standard BGA Package Specifications (1.27mm pitch).

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
0	IO_L01N_0	B3
0	IO_L01P_0	A3
0	IO_L02N_0	B4
0	IO_L02P_0	A4
0	IO_L03N_0/VRP_0	C5
0	IO_L03P_0/VRN_0	C6
0	IO_L04N_0/VREF_0	B5
0	IO_L04P_0	A5
0	IO_L05N_0	E6
0	IO_L05P_0	D6
0	IO_L06N_0	B6
0	IO_L06P_0	A6
0	IO_L19N_0	E7
0	IO_L19P_0	D8
0	IO_L21N_0	F8
0	IO_L21P_0/VREF_0	E8
0	IO_L22N_0	C7
0	IO_L22P_0	C8
0	IO_L24N_0	B7
0	IO_L24P_0	A7
0	IO_L25N_0	H9
0	IO_L25P_0	J9
0	IO_L27N_0	F9
0	IO_L27P_0/VREF_0	G9
0	IO_L28N_0	E9
0	IO_L28P_0	D9
0	IO_L30N_0	C9
0	IO_L30P_0	B9
0	IO_L49N_0	A8
0	IO_L49P_0	A9
0	IO_L51N_0	G10
0	IO_L51P_0/VREF_0	H10
0	IO_L52N_0	F10

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
5	IO_L23N_5	AD20		
5	IO_L23P_5	AD21		
5	IO_L22N_5	AK25		
5	IO_L22P_5	AK24		
5	IO_L21N_5/VREF_5	AH24		
5	IO_L21P_5	AH25		
5	IO_L20N_5	AE21		
5	IO_L20P_5	AD22		
5	IO_L19N_5	AJ25		
5	IO_L19P_5	AJ24		
5	IO_L06N_5	AG25		
5	IO_L06P_5	AG24		
5	IO_L05N_5/VRP_5	AC20		
5	IO_L05P_5/VRN_5	AC21		
5	IO_L04N_5	AK26		
5	IO_L04P_5/VREF_5	AK27		
5	IO_L03N_5/D4/ALT_VRP_5	AH26		
5	IO_L03P_5/D5/ALT_VRN_5	AJ27		
5	IO_L02N_5/D6	AE22		
5	IO_L02P_5/D7	AE23		
5	IO_L01N_5/RDWR_B	AJ28		
5	IO_L01P_5/CS_B	AK29		
6	IO_L01P_6	AC22		
6	IO_L01N_6	AB23		
6	IO_L02P_6/VRN_6	AG28		
6	IO_L02N_6/VRP_6	AF28		
6	IO_L03P_6	AJ30		
6	IO_L03N_6/VREF_6	AH30		
6	IO_L04P_6	AD23		
6	IO_L04N_6	AC23		
6	IO_L05P_6	AF27		
6	IO_L05N_6	AE27		
6	IO_L06P_6	AG29		
6	IO_L06N_6	AH29		
6	IO_L19P_6	AE24		
6	IO_L19N_6	AD24		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
NA	GND	T13		
NA	GND	T12		
NA	GND	R19		
NA	GND	R18		
NA	GND	R17		
NA	GND	R16		
NA	GND	R15		
NA	GND	R14		
NA	GND	R13		
NA	GND	R12		
NA	GND	P24		
NA	GND	P19		
NA	GND	P18		
NA	GND	P17		
NA	GND	P16		
NA	GND	P15		
NA	GND	P14		
NA	GND	P13		
NA	GND	P12		
NA	GND	P7		
NA	GND	N19		
NA	GND	N18		
NA	GND	N17		
NA	GND	N16		
NA	GND	N15		
NA	GND	N14		
NA	GND	N13		
NA	GND	N12		
NA	GND	M26		
NA	GND	M19		
NA	GND	M18		
NA	GND	M17		
NA	GND	M16		
NA	GND	M15		
NA	GND	M14		
NA	GND	M13		
NA	GND	M12		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
3	IO_L34N_3	AH6	NC	
3	IO_L34P_3	AJ6	NC	
3	IO_L33N_3/VREF_3	AJ8	NC	
3	IO_L33P_3	AH8	NC	
3	IO_L32N_3	AL1	NC	
3	IO_L32P_3	AM1	NC	
3	IO_L31N_3	AH7	NC	
3	IO_L31P_3	AJ7	NC	
3	IO_L30N_3	AH10		
3	IO_L30P_3	AG10		
3	IO_L29N_3	AK3		
3	IO_L29P_3	AL3		
3	IO_L28N_3	AK4		
3	IO_L28P_3	AL4		
3	IO_L27N_3/VREF_3	AJ9		
3	IO_L27P_3	AH9		
3	IO_L26N_3	AM2		
3	IO_L26P_3	AN2		
3	IO_L25N_3	AK5		
3	IO_L25P_3	AL5		
3	IO_L24N_3	AK9		
3	IO_L24P_3	AK8		
3	IO_L23N_3	AN1		
3	IO_L23P_3	AP1		
3	IO_L22N_3	AK6		
3	IO_L22P_3	AL6		
3	IO_L21N_3/VREF_3	AH12		
3	IO_L21P_3	AG12		
3	IO_L20N_3	AM3		
3	IO_L20P_3	AN3		
3	IO_L19N_3	AM4		
3	IO_L19P_3	AN4		
3	IO_L12N_3	AJ12	NC	
3	IO_L12P_3	AH11	NC	
3	IO_L11N_3	AP2	NC	
3	IO_L11P_3	AR2	NC	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	VCCINT	AE18		
NA	VCCINT	AE17		
NA	VCCINT	AE16		
NA	VCCINT	AE15		
NA	VCCINT	AD25		
NA	VCCINT	AD24		
NA	VCCINT	AD16		
NA	VCCINT	AD15		
NA	VCCINT	AC25		
NA	VCCINT	AC15		
NA	VCCINT	AB25		
NA	VCCINT	AB15		
NA	VCCINT	AA25		
NA	VCCINT	AA15		
NA	VCCINT	Y27		
NA	VCCINT	Y26		
NA	VCCINT	Y25		
NA	VCCINT	Y15		
NA	VCCINT	Y14		
NA	VCCINT	Y13		
NA	VCCINT	W25		
NA	VCCINT	W15		
NA	VCCINT	V25		
NA	VCCINT	V15		
NA	VCCINT	U25		
NA	VCCINT	U15		
NA	VCCINT	T25		
NA	VCCINT	T24		
NA	VCCINT	T16		
NA	VCCINT	T15		
NA	VCCINT	R25		
NA	VCCINT	R24		
NA	VCCINT	R23		
NA	VCCINT	R22		
NA	VCCINT	R21		
NA	VCCINT	R20		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	VCCINT	R19		
NA	VCCINT	R18		
NA	VCCINT	R17		
NA	VCCINT	R16		
NA	VCCINT	R15		
NA	VCCINT	P26		
NA	VCCINT	P20		
NA	VCCINT	P14		
NA	VCCINT	N27		
NA	VCCINT	N20		
NA	VCCINT	N13		
NA	GND	AW38		
NA	GND	AW37		
NA	GND	AW20		
NA	GND	AW3		
NA	GND	AW2		
NA	GND	AV39		
NA	GND	AV38		
NA	GND	AV37		
NA	GND	AV29		
NA	GND	AV11		
NA	GND	AV3		
NA	GND	AV2		
NA	GND	AV1		
NA	GND	AU39		
NA	GND	AU38		
NA	GND	AU37		
NA	GND	AU3		
NA	GND	AU2		
NA	GND	AU1		
NA	GND	AT36		
NA	GND	AT23		
NA	GND	AT20		
NA	GND	AT17		
NA	GND	AT4		
NA	GND	AR35		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	GND	Y17		
NA	GND	Y16		
NA	GND	Y10		
NA	GND	Y7		
NA	GND	Y4		
NA	GND	Y1		
NA	GND	W24		
NA	GND	W23		
NA	GND	W22		
NA	GND	W21		
NA	GND	W20		
NA	GND	W19		
NA	GND	W18		
NA	GND	W17		
NA	GND	W16		
NA	GND	V24		
NA	GND	V23		
NA	GND	V22		
NA	GND	V21		
NA	GND	V20		
NA	GND	V19		
NA	GND	V18		
NA	GND	V17		
NA	GND	V16		
NA	GND	U36		
NA	GND	U32		
NA	GND	U24		
NA	GND	U23		
NA	GND	U22		
NA	GND	U21		
NA	GND	U20		
NA	GND	U19		
NA	GND	U18		
NA	GND	U17		
NA	GND	U16		
NA	GND	U8		

Notice of Disclaimer

Virtex-II Data Sheet

The Virtex-II Data Sheet contains the following modules: