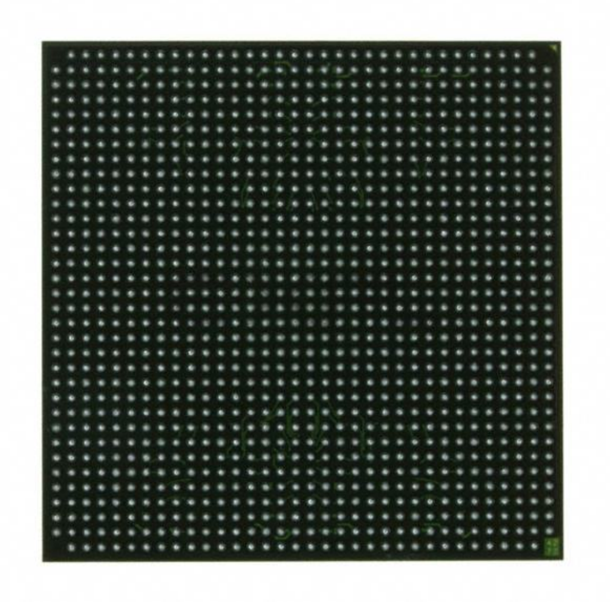

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	5760
Number of Logic Elements/Cells	-
Total RAM Bits	2211840
Number of I/O	824
Number of Gates	4000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v4000-4ffg1152i

Virtex-II Platform FPGAs: Introduction and Overview

DS031-1 (v3.5) November 5, 2007 **Product Specification**

Summary of Virtex-II™ Features

- Industry First Platform FPGA Solution
- IP-Immersion Architecture
  - Densities from 40K to 8M system gates
  - 420 MHz internal clock speed (Advance Data)
  - 840+ Mb/s I/O (Advance Data)
- SelectRAM™ Memory Hierarchy
  - 3 Mb of dual-port RAM in 18 Kbit block SelectRAM resources
  - Up to 1.5 Mb of distributed SelectRAM resources
- High-Performance Interfaces to External Memory
  - DRAM interfaces
    - SDR / DDR SDRAM
    - Network FCRAM
    - Reduced Latency DRAM
  - SRAM interfaces
    - SDR / DDR SRAM
    - QDR™ SRAM
  - CAM interfaces
- Arithmetic Functions
  - Dedicated 18-bit x 18-bit multiplier blocks
  - Fast look-ahead carry logic chains
- Flexible Logic Resources
  - Up to 93,184 internal registers / latches with Clock Enable
  - Up to 93,184 look-up tables (LUTs) or cascadable 16-bit shift registers
  - Wide multiplexers and wide-input function support
  - Horizontal cascade chain and sum-of-products support
  - Internal 3-state bussing
- High-Performance Clock Management Circuitry
  - Up to 12 DCM (Digital Clock Manager) modules
    - Precise clock de-skew
    - Flexible frequency synthesis
    - High-resolution phase shifting
  - 16 global clock multiplexer buffers
- Active Interconnect Technology
  - Fourth generation segmented routing structure
  - Predictable, fast routing delay, independent of fanout
- SelectIO™-Ultra Technology
  - Up to 1,108 user I/Os
  - 19 single-ended and six differential standards
  - Programmable sink current (2 mA to 24 mA) per I/O
  - Digitally Controlled Impedance (DCI) I/O: on-chip termination resistors for single-ended I/O standards
  - PCI-X compatible (133 MHz and 66 MHz) at 3.3V
  - PCI compliant (66 MHz and 33 MHz) at 3.3V
  - CardBus compliant (33 MHz) at 3.3V
  - Differential Signaling
    - 840 Mb/s Low-Voltage Differential Signaling I/O (LVDS) with current mode drivers
    - Bus LVDS I/O
    - Lightning Data Transport (LDT) I/O with current driver buffers
    - Low-Voltage Positive Emitter-Coupled Logic (LVPECL) I/O
    - Built-in DDR input and output registers
  - Proprietary high-performance SelectLink Technology
    - High-bandwidth data path
    - Double Data Rate (DDR) link
    - Web-based HDL generation methodology
- Supported by Xilinx Foundation™ and Alliance Series™ Development Systems
  - Integrated VHDL and Verilog design flows
  - Compilation of 10M system gates designs
  - Internet Team Design (ITD) tool
- SRAM-Based In-System Configuration
  - Fast SelectMAP configuration
  - Triple Data Encryption Standard (DES) security option (Bitstream Encryption)
  - IEEE 1532 support
  - Partial reconfiguration
  - Unlimited reprogrammability
  - Readback capability
- 0.15 μm 8-Layer Metal Process with 0.12 μm High-Speed Transistors
- 1.5V (V_{CCINT}) Core Power Supply, Dedicated 3.3V V_{CCAUX} Auxiliary and V_{CCO} I/O Power Supplies
- IEEE 1149.1 Compatible Boundary-Scan Logic Support
- Flip-Chip and Wire-Bond Ball Grid Array (BGA) Packages in Three Standard Fine Pitches (0.80 mm, 1.00 mm, and 1.27 mm)
- Wire-Bond BGA Devices Available in Pb-Free Packaging (www.xilinx.com/pbfree)
- 100% Factory Tested

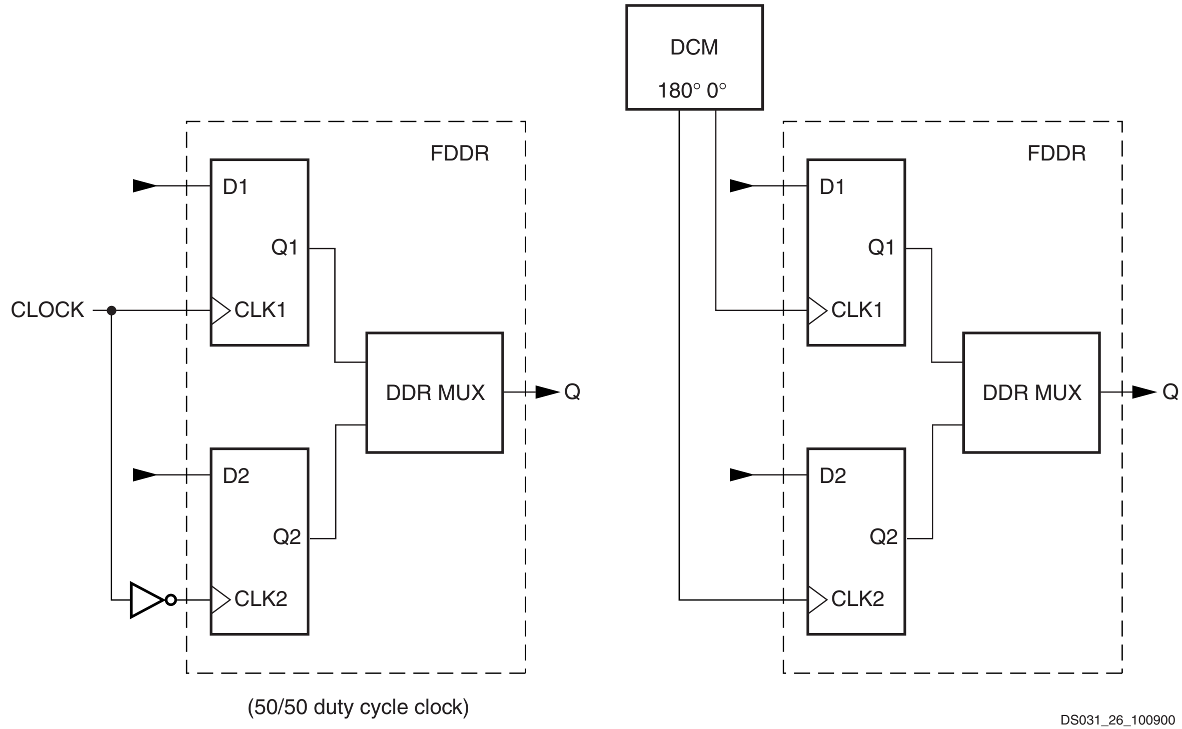

Figure 3: **Double Data Rate Registers**

The DDR mechanism shown in Figure 3 can be used to mirror a copy of the clock on the output. This is useful for propagating a clock along the data that has an identical delay. It is also useful for multiple clock generation, where there is a unique clock driver for every clock load. Virtex-II devices can produce many copies of a clock with very little skew.

Each group of two registers has a clock enable signal (ICE for the input registers, OCE for the output registers, and TCE for the 3-state registers). The clock enable signals are active High by default. If left unconnected, the clock enable for that storage element defaults to the active state.

Each IOB block has common synchronous or asynchronous set and reset (SR and REV signals).

SR forces the storage element into the state specified by the SRHIGH or SRLOW attribute. SRHIGH forces a logic “1”. SRLOW forces a logic “0”. When SR is used, a second input (REV) forces the storage element into the opposite state. The reset condition predominates over the set condition. The initial state after configuration or global initialization state is defined by a separate INIT0 and INIT1 attribute. By default, the SRLOW attribute forces INIT0, and the SRHIGH attribute forces INIT1.

For each storage element, the SRHIGH, SRLOW, INIT0, and INIT1 attributes are independent. Synchronous or asynchronous set / reset is consistent in an IOB block.

All the control signals have independent polarity. Any inverter placed on a control input is automatically absorbed.

Each register or latch (independent of all other registers or latches) (see Figure 4) can be configured as follows:

- No set or reset
- Synchronous set
- Synchronous reset
- Synchronous set and reset
- Asynchronous set (preset)
- Asynchronous reset (clear)
- Asynchronous set and reset (preset and clear)

The synchronous reset overrides a set, and an asynchronous clear overrides a preset.

Table 5: **Summary of Voltage Supply Requirements for All Input and Output Standards**

I/O Standard	V_{CCO}		V_{REF}	Termination Type	
	Output	**Input**	**Input**	**Output**	**Input**
LVDS_33	3.3	N/R	N/R[1]	N/R	N/R
LVDSEXT_33			N/R	N/R	N/R
LVPECL_33			N/R	N/R	N/R
SSTL3_I			1.5	N/R	N/R
SSTL3_II			1.5	N/R	N/R
AGP			1.32	N/R	N/R
LVTTL		3.3	N/R	N/R	N/R
LVCMOS33			N/R	N/R	N/R
LVDCI_33			N/R	Series	N/R
LVDCI_DV2_33			N/R	Series	N/R
PCI33_3			N/R	N/R	N/R
PCI66_3			N/R	N/R	N/R
PCIX			N/R	N/R	N/R
SSTL3_I_DCI			1.5	N/R	Split
SSTL3_II_DCI			1.5	Split	Split
LVDS_25	2.5	N/R	N/R	N/R	N/R
LVDSEXT_25			N/R	N/R	N/R
LDT_25			N/R	N/R	N/R
ULVDS_25			N/R	N/R	N/R
BLVDS_25			N/R	N/R	N/R
SSTL2_I			1.25	N/R	N/R
SSTL2_II			1.25	N/R	N/R
LVCMOS25		2.5	N/R	N/R	N/R
LVDCI_25			N/R	Series	N/R
LVDCI_DV2_25			N/R	Series	N/R
LVDS_25_DCI			N/R	N/R	Split
LVDSEXT_25_DCI			N/R	N/R	Split
SSTL2_I_DCI			1.25	N/R	Split
SSTL2_II_DCI			1.25	Split	Split
HSTL_III_18	1.8	N/R	1.1	N/R	N/R
HSTL_IV_18			1.1	N/R	N/R
HSTL_I_18			0.9	N/R	N/R
HSTL_II_18			0.9	N/R	N/R
SSTL18_I			0.9	N/R	N/R
SSTL18_II			0.9	N/R	N/R
LVCMOS18		1.8	N/R	N/R	N/R
LVDCI_18			N/R	Series	N/R
LVDCI_DV2_18			N/R	Series	N/R
HSTL_III_DCI_18			1.1	N/R	Single
HSTL_IV_DCI_18			1.1	Single	Single
HSTL_I_DCI_18			0.9	N/R	Split
HSTL_II_DCI_18			0.9	Split	Split
SSTL18_I_DCI			0.9	N/R	Split
SSTL18_II_DCI			0.9	Split	Split
HSTL_III	1.5	N/R	0.9	N/R	N/R
HSTL_IV			0.9	N/R	N/R
HSTL_I			0.75	N/R	N/R
HSTL_II			0.75	N/R	N/R
LVCMOS15		1.5	N/R	N/R	N/R
LVDCI_15			N/R	Series	N/R
LVDCI_DV2_15			N/R	Series	N/R
GTLP_DCI			1	Single	Single
HSTL_III_DCI			0.9	N/R	Single
HSTL_IV_DCI			0.9	Single	Single
HSTL_I_DCI			0.75	N/R	Split
HSTL_II_DCI			0.75	Split	Split
GTL_DCI	1.2	1.2	0.8	Single	Single
GTLP	N/R	N/R	1	N/R	N/R
GTL			0.8	N/R	N/R

Notes:
1. N/R = no requirement.

Sum of Products

Each Virtex-II slice has a dedicated OR gate named ORCY, ORing together outputs from the slices carryout and the ORCY from an adjacent slice. The ORCY gate with the dedicated Sum of Products (SOP) chain are designed for implementing large, flexible SOP chains. One input of each ORCY is connected through the fast SOP chain to the output of the previous ORCY in the same slice row. The second input is connected to the output of the top MUXCY in the same slice, as shown in Figure 25.

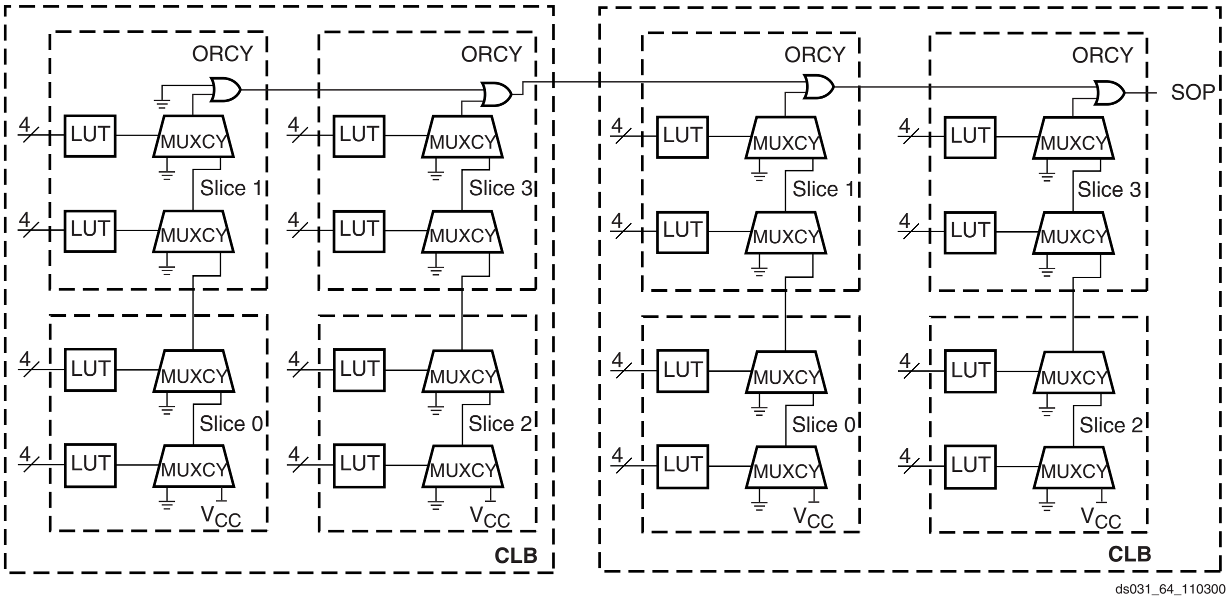

Figure 25: **Horizontal Cascade Chain**

LUTs and MUXCYs can implement large AND gates or other combinatorial logic functions. Figure 26 illustrates LUT and MUXCY resources configured as a 16-input AND gate.

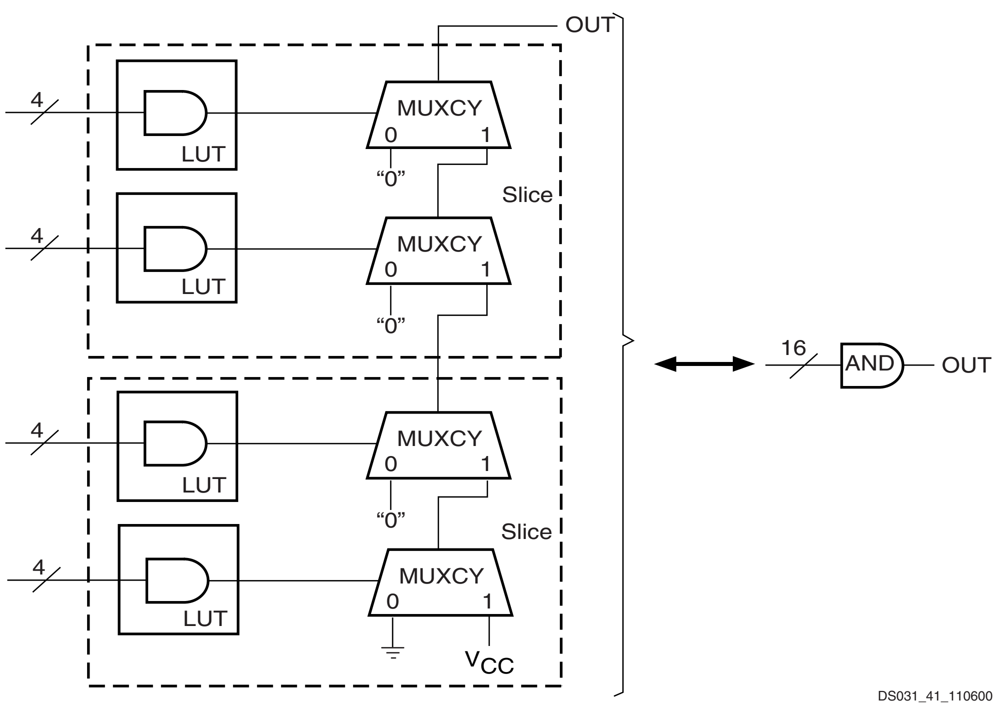

Figure 26: **Wide-Input AND Gate (16 Inputs)**

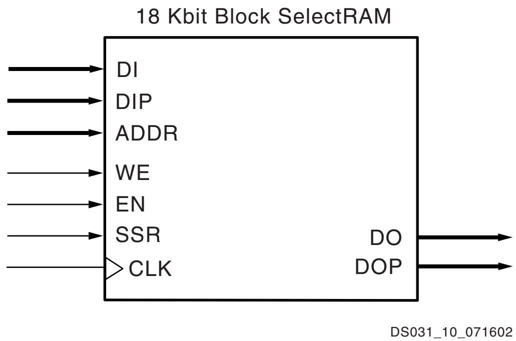

Figure 29: **18 Kbit Block SelectRAM Memory in Single-Port Mode**

Dual-Port Configuration

As a dual-port RAM, each port of block SelectRAM has access to a common 18 Kbit memory resource. These are fully synchronous ports with independent control signals for each port. The data widths of the two ports can be configured independently, providing built-in bus-width conversion.

Table 15 illustrates the different configurations available on ports A and B.

If both ports are configured in either 2K x 9-bit, 1K x 18-bit, or 512 x 36-bit configurations, the 18 Kbit block is accessible from port A or B. If both ports are configured in either 16K x 1-bit, 8K x 2-bit. or 4K x 4-bit configurations, the 16 K-bit block is accessible from Port A or Port B. All other configurations result in one port having access to an 18 Kbit memory block and the other port having access to a 16 K-bit subset of the memory block equal to 16 Kbits.

Table 15: **Dual-Port Mode Configurations**

Port A	16K x 1	16K x 1	16K x 1	16K x 1	16K x 1	16K x 1
Port B	16K x 1	8K x 2	4K x 4	2K x 9	1K x 18	512 x 36
Port A	8K x 2	8K x 2	8K x 2	8K x 2	8K x 2	
Port B	8K x 2	4K x 4	2K x 9	1K x 18	512 x 36	
Port A	4K x 4	4K x 4	4K x 4	4K x 4		
Port B	4K x 4	2K x 9	1K x 18	512 x 36		
Port A	2K x 9	2K x 9	2K x 9			
Port B	2K x 9	1K x 18	512 x 36			
Port A	1K x 18	1K x 18				
Port B	1K x 18	512 x 36				
Port A	512 x 36					
Port B	512 x 36					

Table 4: **Quiescent Supply Current**

Symbol	Description	Device	Min	Typical	Max	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC2V40		3	125	mA
		XC2V80		5	125	
		XC2V250		8	150	
		XC2V500		10	200	
		XC2V1000		12	250	
		XC2V1500		15	350	
		XC2V2000		20	400	
		XC2V3000		27	500	
		XC2V4000		35	650	
		XC2V6000		45	800	
		XC2V8000		60	1100	
I_{CCOQ}	Quiescent V_{CCO} supply current(1,2)	XC2V40		1	2	mA
		XC2V80		1	2	
		XC2V250		1	2	
		XC2V500		1	2	
		XC2V1000		1	2	
		XC2V1500		2	4	
		XC2V2000		2	4	
		XC2V3000		2	4	
		XC2V4000		2	4	
		XC2V6000		2	4	
		XC2V8000		2	4	
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current(1,2)	XC2V40		5	25	mA
		XC2V80		5	25	
		XC2V250		5	25	
		XC2V500		5	25	
		XC2V1000		5	25	
		XC2V1500		7.5	50	
		XC2V2000		7.5	50	
		XC2V3000		10	75	
		XC2V4000		10	75	
		XC2V6000		12.5	100	
		XC2V8000		12.5	100	

Notes:
1. With no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
2. If DCI or differential signaling is used, more accurate values can be obtained by using the Power Estimator or XPOWER™.
3. Data are retained even if V_{CCO} drops to 0 V.
4. Values specified for quiescent supply current parameters are Commercial Grade. For Industrial Grade values, multiply Commercial Grade values by 1.25.

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device operation. The actual current consumed depends on the power-on ramp rate of the power supply.

The V_{CCINT}, V_{CCAUX}, and V_{CCO} power supplies shall each ramp on, monotonically, no faster than 200 µs and no slower than 50 ms. Ramp on is defined as: 0 V_{DC} to minimum supply voltages.

Table 5 shows the minimum current required by Virtex-II devices for proper power on and configuration.

Power supplies can be turned on in any sequence.(1)

If any V_{CCO} bank powers up before V_{CCAUX}, then each bank draws up to 300 mA, worst case, until the V_{CCAUX} powers up.(2) This does not harm the device. If the current is limited to the minimum value above, or larger, the device powers on properly after all three supplies have passed through their power-on reset threshold voltages.

Once initialized and configured, use the power calculator to estimate current drain on these supplies.

Notes:
1. If the V_{CCINT} ramp rate is longer than 10 ms, then V_{CCINT} must be applied before V_{CCO} and V_{CCAUX}. The device will not be damaged if this requirement is violated, but configuration will probably fail.
2. The 300 mA is transient current (peak); it eventually disappears even if V_{CCAUX} does not power up.

Output Clock Jitter

Table 40: **Output Clock Jitter**

Description	Symbol	Constraints	Speed Grade			Units
			-6	-5	-4	
Clock Synthesis Period Jitter						
CLK0	CLKOUT_PER_JITT_0		±100	±100	±100	ps
CLK90	CLKOUT_PER_JITT_90		±150	±150	±150	ps
CLK180	CLKOUT_PER_JITT_180		±150	±150	±150	ps
CLK270	CLKOUT_PER_JITT_270		±150	±150	±150	ps
CLK2X, CLK2X180	CLKOUT_PER_JITT_2X		±200	±200	±200	ps
CLKDV (integer division)	CLKOUT_PER_JITT_DV1		±150	±150	±150	ps
CLKDV (non-integer division)	CLKOUT_PER_JITT_DV2		±300	±300	±300	ps
CLKFX, CLKFX180	CLKOUT_PER_JITT_FX		Note 1	Note 1	Note 1	ps

Notes:
1. Values for this parameter are available at www.xilinx.com.

Output Clock Phase Alignment

Table 41: **Output Clock Phase Alignment**

Description	Symbol	Constraints	Speed Grade			Units
			-6	-5	-4	
Phase Offset Between CLKIN and CLKFB						
CLKIN/CLKFB	CLKIN_CLKFB_PHASE		±50	±50	±50	ps
Phase Offset Between Any DCM Outputs						
All CLK outputs	CLKOUT_PHASE		±140	±140	±140	ps
Duty Cycle Precision						
DLL outputs(1)	CLKOUT_DUTY_CYCLE_DLL(2)		±150	±150	±150	ps
CLKFX outputs	CLKOUT_DUTY_CYCLE_FX		±100	±100	±100	ps

Notes:
1. "DLL outputs" is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. CLKOUT_DUTY_CYCLE_DLL applies to the 1X clock outputs (CLK0, CLK90, CLK180, and CLK270) only if DUTY_CYCLE_CORRECTION = TRUE.
3. Specification also applies to PSCLK.

Source-Synchronous Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-II source-synchronous transmitter and receiver data-valid windows.

Table 45: **Duty Cycle Distortion and Clock-Tree Skew**

Description	Symbol	Device	Speed Grade -6	Speed Grade -5	Speed Grade -4	Units
Duty Cycle Distortion(1)	T_{DCD_CLK0}	All	140	140	140	ps
	T_{DCD_CLK180}	All	50	50	50	ps
Clock Tree Skew(2)	T_{CKSKEW}	XC2V40	50	50	60	ps
		XC2V80	50	50	60	ps
		XC2V250	50	50	60	ps
		XC2V500	50	50	60	ps
		XC2V1000	80	80	90	ps
		XC2V1500	80	80	90	ps
		XC2V2000	100	100	110	ps
		XC2V3000	100	100	110	ps
		XC2V4000	400	400	450	ps
		XC2V6000	500	500	550	ps
		XC2V8000		600	650	ps

Notes:

1. These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
   T_{DCD_CLK0} applies to cases where local (IOB) inversion is used to provide the negative-edge clock to the DDR element in the I/O.
   T_{DCD_CLK180} applies to cases where the CLK180 output of the DCM is used to provide the negative-edge clock to the DDR element in the I/O.
2. This value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

Table 46: **Package Skew**

Description	Symbol	Device/Package	Value	Units
Package Skew(1)	$T_{PKGSKEW}$	XC2V1000 / FF896	130	ps
		XC2V3000 / FF1152	115	ps
		XC2V3000 / BF957	130	ps
		XC2V4000 / FF1152	130	ps
		XC2V4000 / FF1517	200	ps
		XC2V4000 / BF957	140	ps
		XC2V6000 / FF1152	90	ps
		XC2V6000 / FF1517	105	ps
		XC2V6000 / BF957	105	ps

Notes:

1. These values represent the worst-case skew between any two balls of the package: shortest flight time to longest flight time from Pad to Ball (7.1ps per mm).
2. Package trace length information is available for these device/package combinations. This information can be used to deskew the package.

Table 6: **FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
5	IO_L01P_5/CS_B	T3		
6	IO_L01P_6	P1		
6	IO_L01N_6	N1		
6	IO_L02P_6/VRN_6	N3		
6	IO_L02N_6/VRP_6	N2		
6	IO_L03P_6	M4		
6	IO_L03N_6/VREF_6	M3		
6	IO_L04P_6	M2	NC	
6	IO_L04N_6	M1	NC	
6	IO_L06P_6	L4	NC	
6	IO_L06N_6	L3	NC	
6	IO_L43P_6	L2	NC	NC
6	IO_L43N_6	L1	NC	NC
6	IO_L45P_6	L5	NC	NC
6	IO_L45N_6/VREF_6	K5	NC	NC
6	IO_L91P_6	K4	NC	
6	IO_L91N_6	K3	NC	
6	IO_L93P_6	K2	NC	
6	IO_L93N_6/VREF_6	K1	NC	
6	IO_L94P_6	J4		
6	IO_L94N_6	J3		
6	IO_L96P_6	J2		
6	IO_L96N_6	J1		
7	IO_L96P_7	H1		
7	IO_L96N_7	H2		
7	IO_L94P_7	H3		
7	IO_L94N_7	H4		
7	IO_L93P_7/VREF_7	G1	NC	
7	IO_L93N_7	G2	NC	
7	IO_L91P_7	G3	NC	
7	IO_L91N_7	G4	NC	
7	IO_L45P_7/VREF_7	G5	NC	NC

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
4	IO_L06P_4	Y21		
4	IO_L19N_4	AE24		
4	IO_L19P_4	AF24		
4	IO_L21N_4	AE23		
4	IO_L21P_4/VREF_4	AF23		
4	IO_L22N_4	AE22		
4	IO_L22P_4	AF22		
4	IO_L24N_4	AF21		
4	IO_L24P_4	AF20		
4	IO_L25N_4	AA19	NC	NC
4	IO_L25P_4	AB19	NC	NC
4	IO_L27N_4	AD20	NC	NC
4	IO_L27P_4/VREF_4	AC20	NC	NC
4	IO_L28N_4	AC19	NC	NC
4	IO_L28P_4	AD19	NC	NC
4	IO_L49N_4	AE19		
4	IO_L49P_4	AF19		
4	IO_L51N_4	AA18		
4	IO_L51P_4/VREF_4	AB18		
4	IO_L52N_4	Y18		
4	IO_L52P_4	Y17		
4	IO_L54N_4	AC18		
4	IO_L54P_4	AD18		
4	IO_L67N_4	AE18		
4	IO_L67P_4	AF18		
4	IO_L69N_4	AA17		
4	IO_L69P_4/VREF_4	AB17		
4	IO_L70N_4	AC17		
4	IO_L70P_4	AD17		
4	IO_L72N_4	AF17		
4	IO_L72P_4	AF16		
4	IO_L73N_4	AB16	NC	
4	IO_L73P_4	AC16	NC	
4	IO_L75N_4	AA16	NC	
4	IO_L75P_4/VREF_4	Y16	NC	
4	IO_L76N_4	AD16	NC	
4	IO_L76P_4	AE16	NC	

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
1	IO_L01N_1	B4		
1	IO_L01P_1	A4		
2	IO_L01N_2	C1		
2	IO_L01P_2	B1		
2	IO_L02N_2/VRP_2	H9		
2	IO_L02P_2/VRN_2	H8		
2	IO_L03N_2	D3		
2	IO_L03P_2/VREF_2	E3		
2	IO_L04N_2	D2		
2	IO_L04P_2	C2		
2	IO_L05N_2	G7		
2	IO_L05P_2	H7		
2	IO_L06N_2	F4		
2	IO_L06P_2	E4		
2	IO_L19N_2	E1		
2	IO_L19P_2	D1		
2	IO_L20N_2	G6		
2	IO_L20P_2	H6		
2	IO_L21N_2	F5		
2	IO_L21P_2/VREF_2	G5		
2	IO_L22N_2	G2		
2	IO_L22P_2	F2		
2	IO_L23N_2	J8		
2	IO_L23P_2	J7		
2	IO_L24N_2	G3		
2	IO_L24P_2	F3		
2	IO_L43N_2	G1		
2	IO_L43P_2	F1		
2	IO_L44N_2	K8		
2	IO_L44P_2	L8		
2	IO_L45N_2	G4		
2	IO_L45P_2/VREF_2	H4		
2	IO_L46N_2	J2		
2	IO_L46P_2	H2		
2	IO_L47N_2	J6		
2	IO_L47P_2	K6		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
2	IO_L48N_2	J5		
2	IO_L48P_2	H5		
2	IO_L49N_2	J3		
2	IO_L49P_2	H3		
2	IO_L50N_2	K7		
2	IO_L50P_2	L7		
2	IO_L51N_2	J4		
2	IO_L51P_2/VREF_2	K4		
2	IO_L52N_2	K1		
2	IO_L52P_2	J1		
2	IO_L53N_2	L6		
2	IO_L53P_2	M6		
2	IO_L54N_2	L5		
2	IO_L54P_2	K5		
2	IO_L67N_2	L2	NC	
2	IO_L67P_2	K2	NC	
2	IO_L68N_2	M8	NC	
2	IO_L68P_2	N8	NC	
2	IO_L69N_2	L4	NC	
2	IO_L69P_2/VREF_2	M4	NC	
2	IO_L70N_2	M1	NC	
2	IO_L70P_2	L1	NC	
2	IO_L71N_2	M7	NC	
2	IO_L71P_2	N7	NC	
2	IO_L72N_2	M3	NC	
2	IO_L72P_2	L3	NC	
2	IO_L73N_2	N2	NC	NC
2	IO_L73P_2	M2	NC	NC
2	IO_L74N_2	N6	NC	NC
2	IO_L74P_2	P6	NC	NC
2	IO_L75N_2	N5	NC	NC
2	IO_L75P_2/VREF_2	N4	NC	NC
2	IO_L76N_2	P1	NC	NC
2	IO_L76P_2	N1	NC	NC
2	IO_L77N_2	P9	NC	NC
2	IO_L77P_2	R9	NC	NC
2	IO_L78N_2	R5	NC	NC

device shown in the No Connect column. Following this table are the FF1152 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
0	IO_L01N_0	D29	
0	IO_L01P_0	C29	
0	IO_L02N_0	H26	
0	IO_L02P_0	G26	
0	IO_L03N_0/VRP_0	E28	
0	IO_L03P_0/VRN_0	E27	
0	IO_L04N_0/VREF_0	F25	
0	IO_L04P_0	F26	
0	IO_L05N_0	H25	
0	IO_L05P_0	H24	
0	IO_L06N_0	E26	
0	IO_L06P_0	F27	
0	IO_L19N_0	B32	
0	IO_L19P_0	C33	
0	IO_L20N_0	J24	
0	IO_L20P_0	J23	
0	IO_L21N_0	C27	
0	IO_L21P_0/VREF_0	C28	
0	IO_L22N_0	B30	
0	IO_L22P_0	B31	
0	IO_L23N_0	K23	
0	IO_L23P_0	K22	
0	IO_L24N_0	C26	
0	IO_L24P_0	D27	
0	IO_L25N_0	A30	
0	IO_L25P_0	A31	
0	IO_L26N_0	G24	
0	IO_L26P_0	G25	
0	IO_L27N_0	E25	
0	IO_L27P_0/VREF_0	E24	
0	IO_L28N_0	D25	
0	IO_L28P_0	D26	
0	IO_L29N_0	H23	
0	IO_L29P_0	H22	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
4	IO_L67N_4	AN12	
4	IO_L67P_4	AN11	
4	IO_L68N_4	AE14	
4	IO_L68P_4	AE15	
4	IO_L69N_4	AJ13	
4	IO_L69P_4/VREF_4	AJ14	
4	IO_L70N_4	AL13	
4	IO_L70P_4	AL12	
4	IO_L71N_4	AF14	
4	IO_L71P_4	AF15	
4	IO_L72N_4	AM13	
4	IO_L72P_4	AM12	
4	IO_L73N_4	AP12	
4	IO_L73P_4	AP11	
4	IO_L74N_4	AG15	
4	IO_L74P_4	AG16	
4	IO_L75N_4	AN14	
4	IO_L75P_4/VREF_4	AN13	
4	IO_L76N_4	AP14	
4	IO_L76P_4	AP13	
4	IO_L77N_4	AD16	
4	IO_L77P_4	AD17	
4	IO_L78N_4	AK14	
4	IO_L78P_4	AK13	
4	IO_L79N_4	AN16	NC
4	IO_L79P_4	AP15	NC
4	IO_L80N_4	AE16	NC
4	IO_L80P_4	AE17	NC
4	IO_L81N_4	AH15	NC
4	IO_L81P_4/VREF_4	AJ15	NC
4	IO_L82N_4	AP17	NC
4	IO_L82P_4	AN17	NC
4	IO_L83N_4	AH17	NC
4	IO_L83P_4	AH16	NC
4	IO_L84N_4	AL15	NC
4	IO_L84P_4	AL14	NC

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
NA	GND	AP33	
NA	GND	AP32	
NA	GND	AP27	
NA	GND	AP8	
NA	GND	AP3	
NA	GND	AP2	
NA	GND	AN34	
NA	GND	AN33	
NA	GND	AN20	
NA	GND	AN15	
NA	GND	AN2	
NA	GND	AN1	
NA	GND	AM34	
NA	GND	AM32	
NA	GND	AM25	
NA	GND	AM10	
NA	GND	AM3	
NA	GND	AM1	
NA	GND	AL31	
NA	GND	AL4	
NA	GND	AK30	
NA	GND	AK23	
NA	GND	AK12	
NA	GND	AK5	
NA	GND	AJ29	
NA	GND	AJ6	
NA	GND	AH28	
NA	GND	AH21	
NA	GND	AH14	
NA	GND	AH7	
NA	GND	AG34	
NA	GND	AG27	
NA	GND	AG8	
NA	GND	AG1	
NA	GND	AF19	
NA	GND	AF16	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
NA	GND	V19	
NA	GND	V18	
NA	GND	V17	
NA	GND	V16	
NA	GND	V15	
NA	GND	V14	
NA	GND	U21	
NA	GND	U20	
NA	GND	U19	
NA	GND	U18	
NA	GND	U17	
NA	GND	U16	
NA	GND	U15	
NA	GND	U14	
NA	GND	T26	
NA	GND	T21	
NA	GND	T20	
NA	GND	T19	
NA	GND	T18	
NA	GND	T17	
NA	GND	T16	
NA	GND	T15	
NA	GND	T14	
NA	GND	T9	
NA	GND	R33	
NA	GND	R21	
NA	GND	R20	
NA	GND	R19	
NA	GND	R18	
NA	GND	R17	
NA	GND	R16	
NA	GND	R15	
NA	GND	R14	
NA	GND	R2	
NA	GND	P28	
NA	GND	P21	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
4	IO_L08P_4	AL12	NC	
4	IO_L09N_4	AP9	NC	
4	IO_L09P_4/VREF_4	AP8	NC	
4	IO_L10N_4	AV6	NC	
4	IO_L10P_4	AV5	NC	
4	IO_L11N_4	AM11	NC	
4	IO_L11P_4	AM12	NC	
4	IO_L12N_4	AN10	NC	
4	IO_L12P_4	AN9	NC	
4	IO_L19N_4	AU8		
4	IO_L19P_4	AU7		
4	IO_L20N_4	AH14		
4	IO_L20P_4	AH15		
4	IO_L21N_4	AT8		
4	IO_L21P_4/VREF_4	AT7		
4	IO_L22N_4	AW7		
4	IO_L22P_4	AW6		
4	IO_L23N_4	AK13		
4	IO_L23P_4	AK14		
4	IO_L24N_4	AR10		
4	IO_L24P_4	AR9		
4	IO_L25N_4	AV8		
4	IO_L25P_4	AV7		
4	IO_L26N_4	AJ14		
4	IO_L26P_4	AJ15		
4	IO_L27N_4	AP11		
4	IO_L27P_4/VREF_4	AP10		
4	IO_L28N_4	AU10		
4	IO_L28P_4	AU9		
4	IO_L29N_4	AL13		
4	IO_L29P_4	AL14		
4	IO_L30N_4	AN12		
4	IO_L30P_4	AN11		
4	IO_L31N_4	AW9	NC	
4	IO_L31P_4	AW8	NC	
4	IO_L32N_4	AM13	NC	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
4	IO_L32P_4	AM14	NC	
4	IO_L33N_4	AT10	NC	
4	IO_L33P_4/VREF_4	AT9	NC	
4	IO_L34N_4	AV10	NC	
4	IO_L34P_4	AV9	NC	
4	IO_L35N_4	AH16	NC	
4	IO_L35P_4	AH17	NC	
4	IO_L36N_4	AP13	NC	
4	IO_L36P_4	AP12	NC	
4	IO_L49N_4	AU12		
4	IO_L49P_4	AU11		
4	IO_L50N_4	AK15		
4	IO_L50P_4	AJ16		
4	IO_L51N_4	AT12		
4	IO_L51P_4/VREF_4	AT11		
4	IO_L52N_4	AN15		
4	IO_L52P_4	AN14		
4	IO_L53N_4	AR12		
4	IO_L53P_4	AR13		
4	IO_L54N_4	AT14		
4	IO_L54P_4	AT13		
4	IO_L55N_4	AW11		
4	IO_L55P_4	AW10		
4	IO_L56N_4	AM15		
4	IO_L56P_4	AM16		
4	IO_L57N_4	AP15		
4	IO_L57P_4/VREF_4	AP14		
4	IO_L58N_4	AV13		
4	IO_L58P_4	AV12		
4	IO_L59N_4	AK16		
4	IO_L59P_4	AK17		
4	IO_L60N_4	AR16		
4	IO_L60P_4	AR15		
4	IO_L67N_4	AW13		
4	IO_L67P_4	AW12		
4	IO_L68N_4	AL16		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
6	IO_L47N_6	AJ39		
6	IO_L48P_6	AG35		
6	IO_L48N_6	AH35		
6	IO_L49P_6	AG32		
6	IO_L49N_6	AF32		
6	IO_L50P_6	AH37		
6	IO_L50N_6	AG37		
6	IO_L51P_6	AD29		
6	IO_L51N_6/VREF_6	AE29		
6	IO_L52P_6	AD28		
6	IO_L52N_6	AC28		
6	IO_L53P_6	AH38		
6	IO_L53N_6	AG38		
6	IO_L54P_6	AF34		
6	IO_L54N_6	AG34		
6	IO_L55P_6	AE32		
6	IO_L55N_6	AD32		
6	IO_L56P_6	AH39		
6	IO_L56N_6	AG39		
6	IO_L57P_6	AE33		
6	IO_L57N_6/VREF_6	AF33		
6	IO_L58P_6	AD30		
6	IO_L58N_6	AC30		
6	IO_L59P_6	AF37		
6	IO_L59N_6	AE37		
6	IO_L60P_6	AF36		
6	IO_L60N_6	AG36		
6	IO_L67P_6	AD31		
6	IO_L67N_6	AC31		
6	IO_L68P_6	AE34		
6	IO_L68N_6	AD34		
6	IO_L69P_6	AD35		
6	IO_L69N_6/VREF_6	AE35		
6	IO_L70P_6	AB28		
6	IO_L70N_6	AA28		
6	IO_L71P_6	AF39		

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
3	IO_L03P_3	AD7	
3	IO_L02N_3/VRP_3	AE6	
3	IO_L02P_3/VRN_3	AF5	
3	IO_L01N_3	AH2	
3	IO_L01P_3	AH3	
4	IO_L01N_4/BUSY/DOUT(1)	AD9	
4	IO_L01P_4/INIT_B	AD10	
4	IO_L02N_4/D0/DIN(1)	AF7	
4	IO_L02P_4/D1	AG7	
4	IO_L03N_4/D2/ALT_VRP_4	AK3	
4	IO_L03P_4/D3/ALT_VRN_4	AJ5	
4	IO_L04N_4/VREF_4	AE8	
4	IO_L04P_4	AF8	
4	IO_L05N_4/VRP_4	AK4	
4	IO_L05P_4/VRN_4	AK5	
4	IO_L06N_4	AH6	
4	IO_L06P_4	AH7	
4	IO_L19N_4	AC10	
4	IO_L19P_4	AC11	
4	IO_L20N_4	AE9	
4	IO_L20P_4	AE10	
4	IO_L21N_4	AL4	
4	IO_L21P_4/VREF_4	AL5	
4	IO_L22N_4	AB12	
4	IO_L22P_4	AB13	
4	IO_L23N_4	AJ6	
4	IO_L23P_4	AJ8	
4	IO_L24N_4	AK6	
4	IO_L24P_4	AK7	
4	IO_L25N_4	AG8	NC
4	IO_L25P_4	AG9	NC
4	IO_L26N_4	AF9	NC
4	IO_L26P_4	AF11	NC
4	IO_L27N_4	AH8	NC
4	IO_L27P_4/VREF_4	AH9	NC
4	IO_L28N_4	AD11	NC
4	IO_L28P_4	AD12	NC