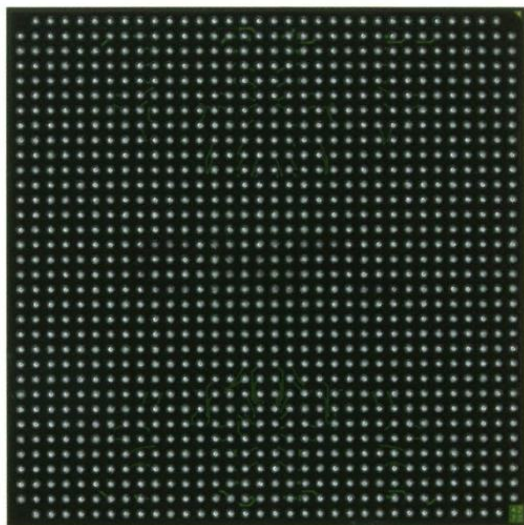




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Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	5760
Number of Logic Elements/Cells	-
Total RAM Bits	2211840
Number of I/O	824
Number of Gates	4000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v4000-5ffg1152c

Table 1: Virtex-II Field-Programmable Gate Array Family Members

Device	System Gates	CLB (1 CLB = 4 slices = Max 128 bits)			Multiplier Blocks	SelectRAM Blocks		DCMs	Max I/O Pads ⁽¹⁾
		Array Row x Col.	Slices	Maximum Distributed RAM Kbits		18 Kbit Blocks	Max RAM (Kbits)		
XC2V40	40K	8 x 8	256	8	4	4	72	4	88
XC2V80	80K	16 x 8	512	16	8	8	144	4	120
XC2V250	250K	24 x 16	1,536	48	24	24	432	8	200
XC2V500	500K	32 x 24	3,072	96	32	32	576	8	264
XC2V1000	1M	40 x 32	5,120	160	40	40	720	8	432
XC2V1500	1.5M	48 x 40	7,680	240	48	48	864	8	528
XC2V2000	2M	56 x 48	10,752	336	56	56	1,008	8	624
XC2V3000	3M	64 x 56	14,336	448	96	96	1,728	12	720
XC2V4000	4M	80 x 72	23,040	720	120	120	2,160	12	912
XC2V6000	6M	96 x 88	33,792	1,056	144	144	2,592	12	1,104
XC2V8000	8M	112 x 104	46,592	1,456	168	168	3,024	12	1,108

Notes:

1. See details in Table 2, "Maximum Number of User I/O Pads".

General Description

The Virtex-II family is a platform FPGA developed for high performance from low-density to high-density designs that are based on IP cores and customized modules. The family delivers complete solutions for telecommunication, wireless, networking, video, and DSP applications, including PCI, LVDS, and DDR interfaces.

The leading-edge 0.15 μm / 0.12 μm CMOS 8-layer metal process and the Virtex-II architecture are optimized for high speed with low power consumption. Combining a wide variety of flexible features and a large range of densities up to 10 million system gates, the Virtex-II family enhances programmable logic design capabilities and is a powerful alternative to mask-programmed gates arrays. As shown in Table 1, the Virtex-II family comprises 11 members, ranging from 40K to 8M system gates.

Packaging

Offerings include ball grid array (BGA) packages with 0.80 mm, 1.00 mm, and 1.27 mm pitches. In addition to traditional wire-bond interconnects, flip-chip interconnect is used in some of the BGA offerings. The use of flip-chip interconnect offers more I/Os than is possible in wire-bond versions of the similar packages. Flip-chip construction offers the combination of high pin count with high thermal capacity.

Wire-bond packages CS, FG, and BG are optionally available in Pb-free versions CSG, FGG, and BGG. See [Virtex-II Ordering Examples, page 6](#).

Table 2 shows the maximum number of user I/Os available. The Virtex-II device/package combination table (Table 6 at the end of this section) details the maximum number of I/Os for each device and package using wire-bond or flip-chip technology.

Table 2: Maximum Number of User I/O Pads

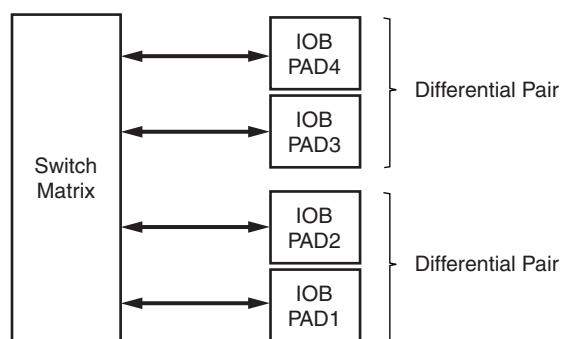
Device	Wire-Bond	Flip-Chip
XC2V40	88	-
XC2V80	120	-
XC2V250	200	-
XC2V500	264	-
XC2V1000	328	432
XC2V1500	392	528
XC2V2000	-	624
XC2V3000	516	720
XC2V4000	-	912
XC2V6000	-	1,104
XC2V8000	-	1,108

Detailed Description

Input/Output Blocks (IOBs)

Virtex-II™ I/O blocks (IOBs) are provided in groups of two or four on the perimeter of each device. Each IOB can be used as input and/or output for single-ended I/Os. Two IOBs can be used as a differential pair. A differential pair is always connected to the same switch matrix, as shown in **Figure 1**.

IOB blocks are designed for high performances I/Os, supporting 19 single-ended standards, as well as differential signaling with LVDS, LDT, Bus LVDS, and LVPECL.



DS031_30_101600

Figure 1: Virtex-II Input/Output Tile

Note: Differential I/Os must use the same clock.

Supported I/O Standards

Virtex-II IOB blocks feature SelectI/O-Ultra inputs and outputs that support a wide variety of I/O signaling standards. In addition to the internal supply voltage ($V_{CCINT} = 1.5V$), output driver supply voltage (V_{CCO}) is dependent on the I/O standard (see **Table 1** and **Table 2**). An auxiliary supply voltage ($V_{CCAUX} = 3.3V$) is required, regardless of the I/O standard used. For exact supply voltage absolute maximum ratings, see **DC Input and Output Levels** in Module 3.

All of the user IOBs have fixed-clamp diodes to V_{CCO} and to ground. As outputs, these IOBs are not compatible or compliant with 5V I/O standards. As inputs, these IOBs are not normally 5V tolerant, but can be used with 5V I/O standards when external current-limiting resistors are used. For more details, see the “5V Tolerant I/Os” Tech Topic at www.xilinx.com.

Table 3 lists supported I/O standards with Digitally Controlled Impedance. See **Digitally Controlled Impedance (DCI)**, page 8.

Table 1: Supported Single-Ended I/O Standards

IOSTANDARD Attribute	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Board Termination Voltage (V_{TT})
LVTTTL	3.3	3.3	N/R ⁽³⁾	N/R
LVC MOS33	3.3	3.3	N/R	N/R
LVC MOS25	2.5	2.5	N/R	N/R
LVC MOS18	1.8	1.8	N/R	N/R
LVC MOS15	1.5	1.5	N/R	N/R
PCI33_3	3.3	3.3	N/R	N/R
PCI66_3	3.3	3.3	N/R	N/R
PCI-X	3.3	3.3	N/R	N/R
GTL	Note (1)	Note (1)	0.8	1.2
GTLP	Note (1)	Note (1)	1.0	1.5
HSTL_I	1.5	N/R	0.75	0.75
HSTL_II	1.5	N/R	0.75	0.75
HSTL_III	1.5	N/R	0.9	1.5
HSTL_IV	1.5	N/R	0.9	1.5
HSTL_I_18	1.8	N/R	0.9	0.9
HSTL_II_18	1.8	N/R	0.9	0.9
HSTL_III_18	1.8	N/R	1.1	1.8
HSTL_IV_18	1.8	N/R	1.1	1.8
SSTL18_I ⁽²⁾	1.8	N/R	0.9	0.9
SSTL18_II	1.8	N/R	0.9	0.9
SSTL2_I	2.5	N/R	1.25	1.25
SSTL2_II	2.5	N/R	1.25	1.25
SSTL3_I	3.3	N/R	1.5	1.5
SSTL3_II	3.3	N/R	1.5	1.5
AGP-2X/AGP	3.3	N/R	1.32	N/R

Notes:

- V_{CCO} of GTL or GTLP should not be lower than the termination voltage or the voltage seen at the I/O pad. Example: If the pin High level is 1.5V, connect V_{CCO} to 1.5V.
- SSTL18_I is not a JEDEC-supported standard.
- N/R = no requirement.

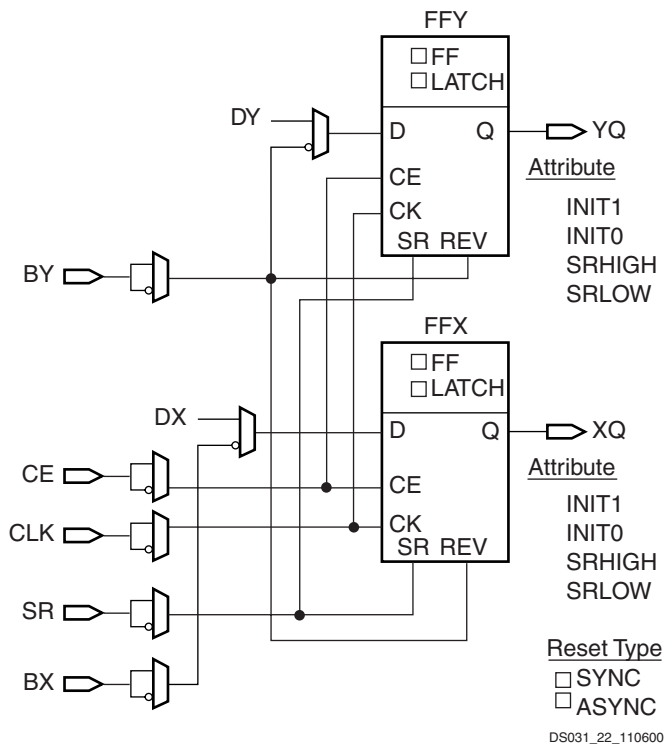


Figure 17: Register / Latch Configuration in a Slice

The set and reset functionality of a register or a latch can be configured as follows:

- No set or reset
- Synchronous set
- Synchronous reset
- Synchronous set and reset
- Asynchronous set (preset)
- Asynchronous reset (clear)
- Asynchronous set and reset (preset and clear)

The synchronous reset has precedence over a set, and an asynchronous clear has precedence over a preset.

Distributed SelectRAM Memory

Each function generator (LUT) can implement a 16 x 1-bit synchronous RAM resource called a distributed SelectRAM element. The SelectRAM elements are configurable within a CLB to implement the following:

- Single-Port 16 x 8 bit RAM
- Single-Port 32 x 4 bit RAM
- Single-Port 64 x 2 bit RAM
- Single-Port 128 x 1 bit RAM
- Dual-Port 16 x 4 bit RAM
- Dual-Port 32 x 2 bit RAM
- Dual-Port 64 x 1 bit RAM

Distributed SelectRAM memory modules are synchronous (write) resources. The combinatorial read access time is extremely fast, while the synchronous write simplifies high-speed designs. A synchronous read can be implemented with a storage element in the same slice. The distributed SelectRAM memory and the storage element share the same clock input. A Write Enable (WE) input is active High, and is driven by the SR input.

Table 9 shows the number of LUTs (2 per slice) occupied by each distributed SelectRAM configuration.

Table 9: Distributed SelectRAM Configurations

RAM	Number of LUTs
16 x 1S	1
16 x 1D	2
32 x 1S	2
32 x 1D	4
64 x 1S	4
64 x 1D	8
128 x 1S	8

Notes:

1. S = single-port configuration; D = dual-port configuration

For single-port configurations, distributed SelectRAM memory has one address port for synchronous writes and asynchronous reads.

For dual-port configurations, distributed SelectRAM memory has one port for synchronous writes and asynchronous reads and another port for asynchronous reads. The function generator (LUT) has separated read address inputs (A1, A2, A3, A4) and write address inputs (WG1/WF1, WG2/WF2, WG3/WF3, WG4/WF4).

In single-port mode, read and write addresses share the same address bus. In dual-port mode, one function generator (R/W port) is connected with shared read and write addresses. The second function generator has the A inputs (read) connected to the second read-only port address and the W inputs (write) shared with the first read/write port address.

Shift Registers

Each function generator can also be configured as a 16-bit shift register. The write operation is synchronous with a clock input (CLK) and an optional clock enable, as shown in **Figure 21**. A dynamic read access is performed through the 4-bit address bus, A[3:0]. The configurable 16-bit shift register cannot be set or reset. The read is asynchronous, however the storage element or flip-flop is available to implement a synchronous read. The storage element should always be used with a constant address. For example, when building an 8-bit shift register and configuring the addresses to point to the 7th bit, the 8th bit can be the flip-flop. The overall system performance is improved by using the superior clock-to-out of the flip-flops.

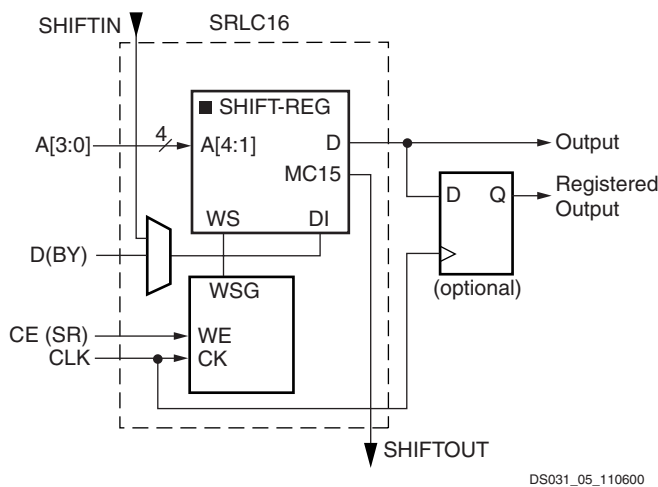


Figure 21: Shift Register Configurations

An additional dedicated connection between shift registers allows connecting the last bit of one shift register to the first bit of the next, without using the ordinary LUT output. (See **Figure 22**.) Longer shift registers can be built with dynamic access to any bit in the chain. The shift register chaining and the MUXF5, MUXF6, and MUXF7 multiplexers allow up to a 128-bit shift register with addressable access to be implemented in one CLB.

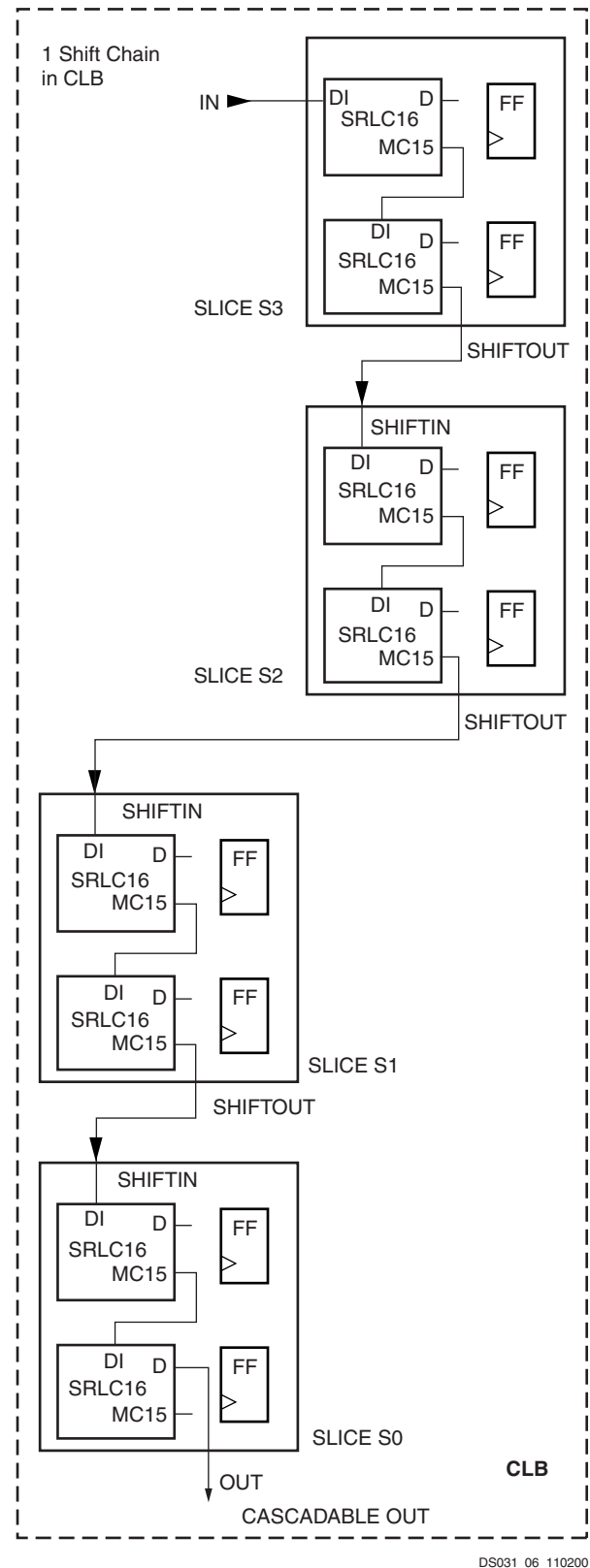


Figure 22: Cascadable Shift Register

The Virtex-II implementation process is comprised of Synthesis, translation, mapping, place and route, and configuration file generation. While the tools can be run individually, many designers choose to run the entire implementation process with the click of a button. To assist those who prefer to script their design flows, Xilinx provides Xflow, an automated single command line process.

Design Verification

In addition to conventional design verification using static timing analysis or simulation techniques, Xilinx offers powerful in-circuit debugging techniques using ChipScope ILA (Integrated Logic Analysis). The reconfigurable nature of Xilinx FPGAs means that designs can be verified in real time without the need for extensive sets of software simulation vectors.

For simulation, the system extracts post-layout timing information from the design database, and back-annotates this information into the netlist for use by the simulator. The back annotation features a variety of patented Xilinx techniques, resulting in the industry's most powerful simulation flows. Alternatively, timing-critical portions of a design can be verified using the Xilinx static timing analyzer or a third party static timing analysis tool like Synopsys Prime Time™, by exporting timing data in the STAMP data format.

For in-circuit debugging, ChipScope ILA enables designers to analyze the real-time behavior of a device while operating at full system speeds. Logic analysis commands and captured data are transferred between the ChipScope software and ILA cores within the Virtex-II FPGA, using industry standard JTAG protocols. These JTAG transactions are driven over an optional download cable (MultiLINX or JTAG), connecting the Virtex device in the target system to a PC or workstation.

ChipScope ILA was designed to look and feel like a logic analyzer, making it easy to begin debugging a design immediately. Modifications to the desired logic analysis can be downloaded directly into the system in a matter of minutes.

Other Unique Features of Virtex-II Design Flow

Xilinx design flows feature a number of unique capabilities. Among these are efficient incremental HDL design flows; a

robust capability that is enabled by Xilinx exclusive hierarchical floorplanning capabilities. Another powerful design capability only available in the Xilinx design flow is "Modular Design", part of the Xilinx suite of team design tools, which enables autonomous design, implementation, and verification of design modules.

Incremental Synthesis

Xilinx unique hierarchical floorplanning capabilities enable designers to create a programmable logic design by isolating design changes within one hierarchical "logic block", and perform synthesis, verification and implementation processes on that specific logic block. By preserving the logic in unchanged portions of a design, Xilinx incremental design makes the high-density design process more efficient.

Xilinx hierarchical floorplanning capabilities can be specified using the high-level floorplanner or a preferred RTL floorplanner (see the Xilinx web site for a list of supported EDA partners). When used in conjunction with one of the EDA partners' floorplanners, higher performance results can be achieved, as many synthesis tools use this more predictable detailed physical implementation information to establish more aggressive and accurate timing estimates when performing their logic optimizations.

Modular Design

Xilinx innovative modular design capabilities take the incremental design process one step further by enabling the designer to delegate responsibility for completing the design, synthesis, verification, and implementation of a hierarchical "logic block" to an arbitrary number of designers - assigning a specific region within the target FPGA for exclusive use by each of the team members.

This team design capability enables an autonomous approach to design modules, changing the hand-off point to the lead designer or integrator from "my module works in simulation" to "my module works in the FPGA". This unique design methodology also leverages the Xilinx hierarchical floorplanning capabilities and enables the Xilinx (or EDA partner) floorplanner to manage the efficient implementation of very high-density FPGAs.

ments to begin changing state in response to the logic and the user clock.

The relative timing of these events can be changed via configuration options in software. In addition, the GTS and GWE events can be made dependent on the DONE pins of multiple devices all going High, forcing the devices to start synchronously. The sequence can also be paused at any stage, until lock has been achieved on any or all DCMs, as well as the DCI.

Readback

In this mode, configuration data from the Virtex-II FPGA device can be read back. Readback is supported only in the SelectMAP (master and slave) and Boundary-Scan mode.

Along with the configuration data, it is possible to read back the contents of all registers, distributed SelectRAM, and block RAM resources. This capability is used for real-time debugging. For more detailed configuration information, see the *Virtex-II Platform FPGA User Guide*.

Bitstream Encryption

Virtex-II devices have an on-chip decryptor using one or two sets of three keys for triple-key Data Encryption Standard (DES) operation. Xilinx software tools offer an optional encryption of the configuration data (bitstream) with a triple-key DES determined by the designer.

The keys are stored in the FPGA by JTAG instruction and retained by a battery connected to the V_{BATT} pin, when the device is not powered. Virtex-II devices can be configured with the corresponding encrypted bitstream, using any of the configuration modes described previously.

A detailed description of how to use bitstream encryption is provided in the *Virtex-II Platform FPGA User Guide*. For devices that support this feature, please contact your sales representative for specific ordering part number.

Partial Reconfiguration

Partial reconfiguration of Virtex-II devices can be accomplished in either Slave SelectMAP mode or Boundary-Scan mode. Instead of resetting the chip and doing a full configuration, new data is loaded into a specified area of the chip, while the rest of the chip remains in operation. Data is loaded on a column basis, with the smallest load unit being a configuration “frame” of the bitstream (device size dependent).

Partial reconfiguration is useful for applications that require different designs to be loaded into the same area of a chip, or that require the ability to change portions of a design without having to reset or reconfigure the entire chip.

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
11/07/00	1.0	Early access draft.
12/06/00	1.1	Initial release.
01/15/01	1.2	Added values to the tables in the Virtex-II Performance Characteristics and Virtex-II Switching Characteristics sections.
01/25/01	1.3	The data sheet was divided into four modules (per the current style standard). A note was added to Table 1 .
04/02/01	1.5	- Under Input/Output Individual Options, the range of values for optional pull-up and pull-down resistors was changed to 10 - 60 KΩ from 50 - 100 KΩ. - Skipped v1.4 to sync up modules. Reverted to traditional double-column format.
07/30/01	1.6	- Added Table 6. - Changed definition of multiply and divide integer ranges under Digital Clock Manager (DCM). - Made numerous minor edits throughout this module.
10/02/01	1.7	Updated descriptions under Digitally Controlled Impedance (DCI), Global Clock Multiplexer Buffers, Digital Clock Manager (DCM), and Creating a Design.
10/12/01	1.8	Made clarifying edits under Digital Clock Manager (DCM).
11/29/01	1.9	Changed bitstream lengths for each device in Table 26.

Virtex-II Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex-II devices. The numbers reported here are worst-case values; they have all been fully characterized. Note that these values are subject to the same guidelines as [Virtex-II Switching Characteristics, page 9](#) (speed files).

Table 11 provides pin-to-pin values (in nanoseconds) including IOB delays; that is, delay through the device from input pin to output pin. In the case of multiple inputs and outputs, the worst delay is reported.

Table 11: Pin-to-Pin Performance

Description	Device Used & Speed Grade	Pin-to-Pin (with I/O delays)	Units
Basic Functions			
16-bit Address Decoder	XC2V1000 -5	6.3	ns
32-bit Address Decoder	XC2V1000 -5	7.7	ns
64-bit Address Decoder	XC2V1000 -5	9.3	ns
4:1 MUX	XC2V1000 -5	5.7	ns
8:1 MUX	XC2V1000 -5	6.5	ns
16:1 MUX	XC2V1000 -5	6.7	ns
32:1 MUX	XC2V1000 -5	8.7	ns
Combinatorial (pad to LUT to pad)	XC2V1000 -5	5.0	ns
Memory			
Block RAM			
Pad to setup		1.6	ns
Clock to Pad		9.5	ns
Distributed RAM			
Pad to setup	XC2V1000 -5	2.7	ns
Clock to Pad	XC2V1000 -5	5.1 (no clk skew)	ns

Table 12 shows internal (register-to-register) performance. Values are reported in MHz.

Table 12: Register-to-Register Performance

Description	Device Used & Speed Grade	Register-to-Register Performance	Units
Basic Functions			
16-bit Address Decoder	XC2V1000 -5	398	MHz
32-bit Address Decoder	XC2V1000 -5	291	MHz
64-bit Address Decoder	XC2V1000 -5	274	MHz
4:1 MUX	XC2V1000 -5	563	MHz
8:1 MUX	XC2V1000 -5	454	MHz
16:1 MUX	XC2V1000 -5	414	MHz
32:1 MUX	XC2V1000 -5	323	MHz
Register to LUT to Register	XC2V1000 -5	613	MHz

BG575/BGG575 Standard BGA Package

As shown in Table 9, XC2V1000, XC2V1500, and XC2V2000 Virtex-II devices are available in the BG575/BGG575 BGA package. Pins in the XC2V1000, XC2V1500, and XC2V2000 devices are the same, except for the pin differences in the XC2V1000 and XC2V1500 devices shown in the No Connect columns. Following this table are the **BG575/BGG575 Standard BGA Package Specifications (1.27mm pitch)**.

Table 9: BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
0	IO_L01N_0	A3		
0	IO_L01P_0	A4		
0	IO_L02N_0	D5		
0	IO_L02P_0	C5		
0	IO_L03N_0/VRP_0	E6		
0	IO_L03P_0/VRN_0	D6		
0	IO_L04N_0/VREF_0	F7		
0	IO_L04P_0	E7		
0	IO_L05N_0	G8		
0	IO_L05P_0	H9		
0	IO_L06N_0	A5		
0	IO_L06P_0	A6		
0	IO_L19N_0	B5		
0	IO_L19P_0	B6		
0	IO_L21N_0	D7		
0	IO_L21P_0/VREF_0	C7		
0	IO_L22N_0	F8		
0	IO_L22P_0	E8		
0	IO_L24N_0	G9		
0	IO_L24P_0	F9		
0	IO_L49N_0	G10		
0	IO_L49P_0	H10		
0	IO_L51N_0	B7		
0	IO_L51P_0/VREF_0	B8		
0	IO_L52N_0	D8		
0	IO_L52P_0	C8		
0	IO_L54N_0	E9		
0	IO_L54P_0	D9		
0	IO_L67N_0	A8	NC	
0	IO_L67P_0	A9	NC	
0	IO_L69N_0	C9	NC	

Table 9: BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
7	IO_L46P_7	H2		
7	IO_L46N_7	G2		
7	IO_L45P_7/VREF_7	H3		
7	IO_L45N_7	H4		
7	IO_L43P_7	G3		
7	IO_L43N_7	G4		
7	IO_L24P_7	H5		
7	IO_L24N_7	H6		
7	IO_L22P_7	J6		
7	IO_L22N_7	J7		
7	IO_L21P_7/VREF_7	K7		
7	IO_L21N_7	K8		
7	IO_L19P_7	E1		
7	IO_L19N_7	E2		
7	IO_L06P_7	D2		
7	IO_L06N_7	D3		
7	IO_L04P_7	E3		
7	IO_L04N_7	E4		
7	IO_L03P_7/VREF_7	F4		
7	IO_L03N_7	F5		
7	IO_L02P_7/VRN_7	G5		
7	IO_L02N_7/VRP_7	G6		
7	IO_L01P_7	H7		
7	IO_L01N_7	J8		
0	VCCO_0	J12		
0	VCCO_0	J11		
0	VCCO_0	J10		
0	VCCO_0	F11		
0	VCCO_0	C6		
0	VCCO_0	B11		
1	VCCO_1	J15		
1	VCCO_1	J14		
1	VCCO_1	J13		
1	VCCO_1	F14		
1	VCCO_1	C19		

Table 10: BG728 BGA — XC2V3000

Bank	Pin Description	Pin Number
5	IO_L52N_5	AC10
5	IO_L52P_5	AB10
5	IO_L51N_5/VREF_5	Y9
5	IO_L51P_5	Y10
5	IO_L49N_5	AG9
5	IO_L49P_5	AG8
5	IO_L30N_5	AF9
5	IO_L30P_5	AE9
5	IO_L28N_5	AD9
5	IO_L28P_5	AC9
5	IO_L27N_5/VREF_5	AB9
5	IO_L27P_5	AA9
5	IO_L25N_5	AE8
5	IO_L25P_5	AE7
5	IO_L24N_5	AD8
5	IO_L24P_5	AC8
5	IO_L22N_5	AB8
5	IO_L22P_5	AA8
5	IO_L21N_5/VREF_5	AG7
5	IO_L21P_5	AF7
5	IO_L19N_5	AC7
5	IO_L19P_5	AB7
5	IO_L06N_5	AG6
5	IO_L06P_5	AF6
5	IO_L05N_5/VRP_5	AE6
5	IO_L05P_5/VRN_5	AD6
5	IO_L04N_5	AG5
5	IO_L04P_5/VREF_5	AF5
5	IO_L03N_5/D4/ALT_VRP_5	AE5
5	IO_L03P_5/D5/ALT_VRN_5	AD5
5	IO_L02N_5/D6	AG4
5	IO_L02P_5/D7	AF4
5	IO_L01N_5/RDWR_B	AG3
5	IO_L01P_5/CS_B	AF3
6	IO_L01P_6	AE1

Table 10: BG728 BGA — XC2V3000

Bank	Pin Description	Pin Number
6	VCCO_6	V9
6	VCCO_6	U10
6	VCCO_6	U9
6	VCCO_6	T10
6	VCCO_6	T7
6	VCCO_6	T3
6	VCCO_6	R10
7	VCCO_7	M10
7	VCCO_7	M7
7	VCCO_7	M3
7	VCCO_7	L10
7	VCCO_7	L9
7	VCCO_7	K9
7	VCCO_7	G4
7	VCCO_7	N10
NA	CCLK	AA22
NA	PROG_B	C4
NA	DONE	AC22
NA	M0	AC6
NA	M1	Y7
NA	M2	AE4
NA	HSWAP_EN	D5
NA	TCK	G20
NA	TDI	H7
NA	TDO	G22
NA	TMS	F21
NA	PWRDWN_B	AE24
NA	DXN	G8
NA	DXP	F7
NA	VBATT	D23
NA	RSVD	C24
NA	VCCAUX	AF14
NA	VCCAUX	AE26
NA	VCCAUX	AE2

Table 10: BG728 BGA — XC2V3000

Bank	Pin Description	Pin Number
NA	VCCINT	K10
NA	GND	AG27
NA	GND	AG26
NA	GND	AG14
NA	GND	AG2
NA	GND	AG1
NA	GND	AF27
NA	GND	AF26
NA	GND	AF20
NA	GND	AF8
NA	GND	AF2
NA	GND	AF1
NA	GND	AE25
NA	GND	AE3
NA	GND	AD24
NA	GND	AD14
NA	GND	AD4
NA	GND	AC23
NA	GND	AC17
NA	GND	AC11
NA	GND	AC5
NA	GND	AB22
NA	GND	AB6
NA	GND	AA21
NA	GND	AA7
NA	GND	Y26
NA	GND	Y20
NA	GND	Y8
NA	GND	Y2
NA	GND	W14
NA	GND	U23
NA	GND	U5
NA	GND	T16
NA	GND	T15
NA	GND	T14
NA	GND	T13

Table 12: FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
3	IO_L23P_3	AJ3	
3	IO_L22N_3	AF7	
3	IO_L22P_3	AG7	
3	IO_L21N_3/VREF_3	AL1	
3	IO_L21P_3	AK1	
3	IO_L20N_3	AH2	
3	IO_L20P_3	AJ2	
3	IO_L19N_3	AJ4	
3	IO_L19P_3	AK4	
3	IO_L06N_3	AE10	
3	IO_L06P_3	AD10	
3	IO_L05N_3	AK2	
3	IO_L05P_3	AL2	
3	IO_L04N_3	AH6	
3	IO_L04P_3	AJ5	
3	IO_L03N_3/VREF_3	AE11	
3	IO_L03P_3	AF11	
3	IO_L02N_3/VRP_3	AK3	
3	IO_L02P_3/VRN_3	AL3	
3	IO_L01N_3	AF10	
3	IO_L01P_3	AG9	
4	IO_L01N_4/BUSY/DOUT ⁽¹⁾	AM4	
4	IO_L01P_4/INIT_B	AL5	
4	IO_L02N_4/D0/DIN ⁽¹⁾	AG10	
4	IO_L02P_4/D1	AH11	
4	IO_L03N_4/D2/ALT_VRP_4	AK7	
4	IO_L03P_4/D3/ALT_VRN_4	AK8	
4	IO_L04N_4/VREF_4	AL6	
4	IO_L04P_4	AM6	
4	IO_L05N_4/VRP_4	AK9	
4	IO_L05P_4/VRN_4	AJ8	
4	IO_L06N_4	AM8	
4	IO_L06P_4	AM7	
4	IO_L19N_4	AN3	
4	IO_L19P_4	AM2	

Table 12: FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
2	VCCO_2	R11	
2	VCCO_2	R5	
2	VCCO_2	P12	
2	VCCO_2	P11	
2	VCCO_2	N12	
2	VCCO_2	N11	
2	VCCO_2	M11	
2	VCCO_2	K1	
2	VCCO_2	G4	
3	VCCO_3	AH4	
3	VCCO_3	AE1	
3	VCCO_3	AC11	
3	VCCO_3	AB12	
3	VCCO_3	AB11	
3	VCCO_3	AA12	
3	VCCO_3	AA11	
3	VCCO_3	Y12	
3	VCCO_3	Y11	
3	VCCO_3	Y5	
3	VCCO_3	W12	
3	VCCO_3	W1	
3	VCCO_3	V12	
4	VCCO_4	AP16	
4	VCCO_4	AP10	
4	VCCO_4	AL7	
4	VCCO_4	AK15	
4	VCCO_4	AD15	
4	VCCO_4	AD14	
4	VCCO_4	AD13	
4	VCCO_4	AD12	
4	VCCO_4	AC17	
4	VCCO_4	AC16	
4	VCCO_4	AC15	
4	VCCO_4	AC14	
4	VCCO_4	AC13	
5	VCCO_5	AP25	

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
0	IO_L52P_0	A30		
0	IO_L53N_0	G26		
0	IO_L53P_0	G25		
0	IO_L54N_0	D26		
0	IO_L54P_0	D27		
0	IO_L55N_0	B27		
0	IO_L55P_0	B28		
0	IO_L56N_0	H25		
0	IO_L56P_0	H24		
0	IO_L57N_0	F25		
0	IO_L57P_0/VREF_0	F26		
0	IO_L58N_0	A27		
0	IO_L58P_0	A28		
0	IO_L59N_0	K24		
0	IO_L59P_0	K23		
0	IO_L60N_0	E24		
0	IO_L60P_0	E25		
0	IO_L67N_0	C26		
0	IO_L67P_0	C27		
0	IO_L68N_0	J24		
0	IO_L68P_0	J23		
0	IO_L69N_0	D24		
0	IO_L69P_0/VREF_0	D25		
0	IO_L70N_0	A25		
0	IO_L70P_0	A26		
0	IO_L71N_0	M22		
0	IO_L71P_0	M21		
0	IO_L72N_0	G23		
0	IO_L72P_0	G24		
0	IO_L73N_0	B25		
0	IO_L73P_0	C25		
0	IO_L74N_0	L22		
0	IO_L74P_0	L21		
0	IO_L75N_0	F23		
0	IO_L75P_0/VREF_0	F24		
0	IO_L76N_0	C23		

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
4	IO_L08P_4	AL12	NC	
4	IO_L09N_4	AP9	NC	
4	IO_L09P_4/VREF_4	AP8	NC	
4	IO_L10N_4	AV6	NC	
4	IO_L10P_4	AV5	NC	
4	IO_L11N_4	AM11	NC	
4	IO_L11P_4	AM12	NC	
4	IO_L12N_4	AN10	NC	
4	IO_L12P_4	AN9	NC	
4	IO_L19N_4	AU8		
4	IO_L19P_4	AU7		
4	IO_L20N_4	AH14		
4	IO_L20P_4	AH15		
4	IO_L21N_4	AT8		
4	IO_L21P_4/VREF_4	AT7		
4	IO_L22N_4	AW7		
4	IO_L22P_4	AW6		
4	IO_L23N_4	AK13		
4	IO_L23P_4	AK14		
4	IO_L24N_4	AR10		
4	IO_L24P_4	AR9		
4	IO_L25N_4	AV8		
4	IO_L25P_4	AV7		
4	IO_L26N_4	AJ14		
4	IO_L26P_4	AJ15		
4	IO_L27N_4	AP11		
4	IO_L27P_4/VREF_4	AP10		
4	IO_L28N_4	AU10		
4	IO_L28P_4	AU9		
4	IO_L29N_4	AL13		
4	IO_L29P_4	AL14		
4	IO_L30N_4	AN12		
4	IO_L30P_4	AN11		
4	IO_L31N_4	AW9	NC	
4	IO_L31P_4	AW8	NC	
4	IO_L32N_4	AM13	NC	

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
4	IO_L32P_4	AM14	NC	
4	IO_L33N_4	AT10	NC	
4	IO_L33P_4/VREF_4	AT9	NC	
4	IO_L34N_4	AV10	NC	
4	IO_L34P_4	AV9	NC	
4	IO_L35N_4	AH16	NC	
4	IO_L35P_4	AH17	NC	
4	IO_L36N_4	AP13	NC	
4	IO_L36P_4	AP12	NC	
4	IO_L49N_4	AU12		
4	IO_L49P_4	AU11		
4	IO_L50N_4	AK15		
4	IO_L50P_4	AJ16		
4	IO_L51N_4	AT12		
4	IO_L51P_4/VREF_4	AT11		
4	IO_L52N_4	AN15		
4	IO_L52P_4	AN14		
4	IO_L53N_4	AR12		
4	IO_L53P_4	AR13		
4	IO_L54N_4	AT14		
4	IO_L54P_4	AT13		
4	IO_L55N_4	AW11		
4	IO_L55P_4	AW10		
4	IO_L56N_4	AM15		
4	IO_L56P_4	AM16		
4	IO_L57N_4	AP15		
4	IO_L57P_4/VREF_4	AP14		
4	IO_L58N_4	AV13		
4	IO_L58P_4	AV12		
4	IO_L59N_4	AK16		
4	IO_L59P_4	AK17		
4	IO_L60N_4	AR16		
4	IO_L60P_4	AR15		
4	IO_L67N_4	AW13		
4	IO_L67P_4	AW12		
4	IO_L68N_4	AL16		

FF1517 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)

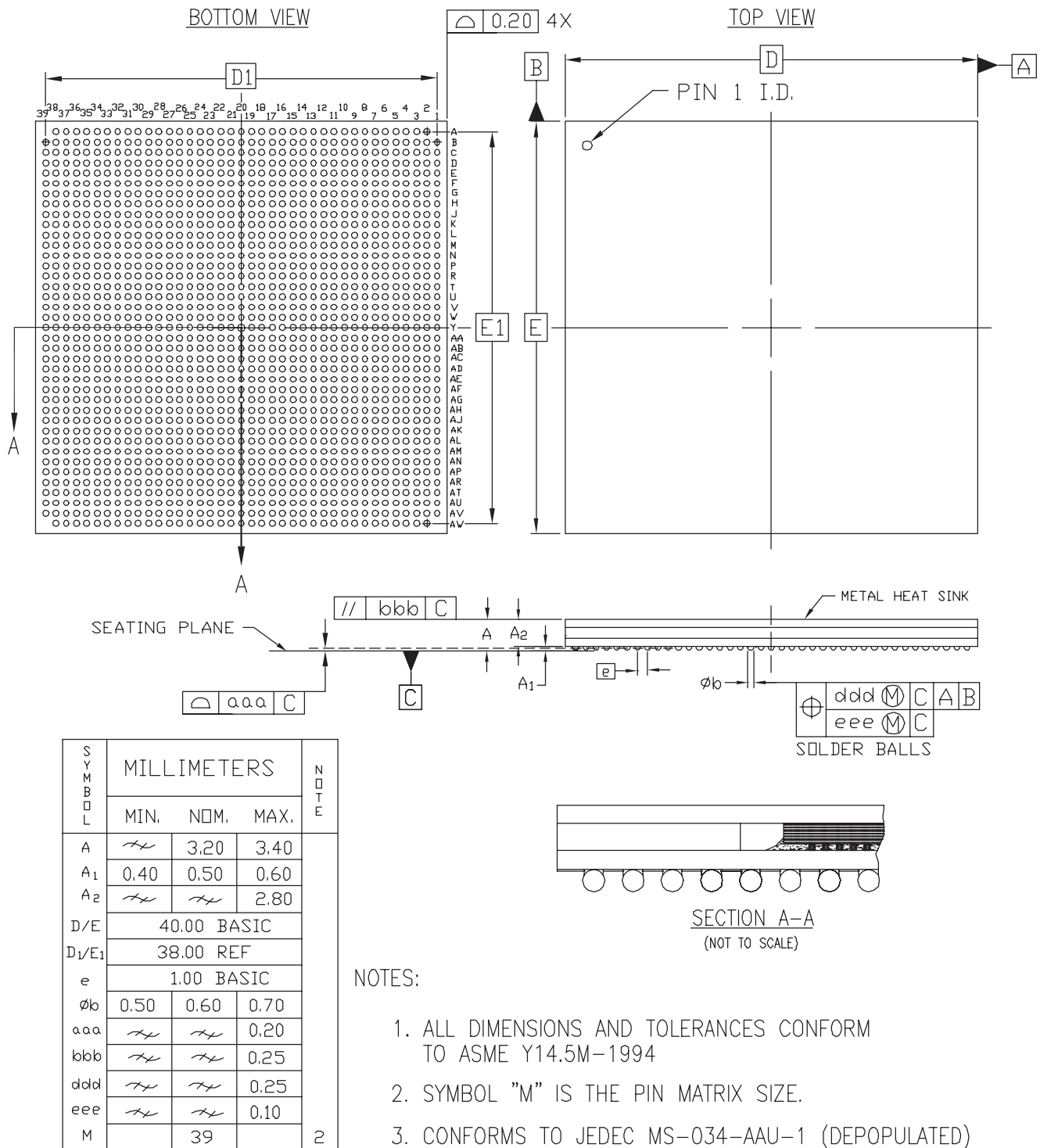


Figure 9: FF1517 Flip-Chip Fine-Pitch BGA Package Specifications

Table 14: BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000

Bank	Pin Description	Pin Number	No Connect in XC2V2000
6	IO_L20P_6	AD25	
6	IO_L20N_6	AC24	
6	IO_L21P_6	AG30	
6	IO_L21N_6/VREF_6	AF30	
6	IO_L22P_6	AD26	
6	IO_L22N_6	AC26	
6	IO_L23P_6	AF29	
6	IO_L23N_6	AD29	
6	IO_L24P_6	AE28	
6	IO_L24N_6	AD28	
6	IO_L25P_6	AB24	NC
6	IO_L25N_6	AA24	NC
6	IO_L27P_6	AC25	NC
6	IO_L27N_6/VREF_6	AB25	NC
6	IO_L43P_6	AF31	
6	IO_L43N_6	AE31	
6	IO_L44P_6	AA23	
6	IO_L44N_6	Y23	
6	IO_L45P_6	AE30	
6	IO_L45N_6/VREF_6	AC30	
6	IO_L46P_6	AC28	
6	IO_L46N_6	AA28	
6	IO_L47P_6	AD27	
6	IO_L47N_6	AC27	
6	IO_L48P_6	AA25	
6	IO_L48N_6	Y25	
6	IO_L49P_6	AC29	
6	IO_L49N_6	AB29	
6	IO_L50P_6	AB27	
6	IO_L50N_6	AA27	
6	IO_L51P_6	AA26	
6	IO_L51N_6/VREF_6	Y26	
6	IO_L52P_6	AD31	
6	IO_L52N_6	AC31	
6	IO_L53P_6	W22	
6	IO_L53N_6	V22	
6	IO_L54P_6	Y27	
6	IO_L54N_6	W27	

Table 14: BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000

Bank	Pin Description	Pin Number	No Connect in XC2V2000
6	IO_L67P_6	AB30	
6	IO_L67N_6	AA30	
6	IO_L68P_6	W26	
6	IO_L68N_6	V26	
6	IO_L69P_6	AB31	
6	IO_L69N_6/VREF_6	AA31	
6	IO_L70P_6	AA29	
6	IO_L70N_6	Y29	
6	IO_L71P_6	Y24	
6	IO_L71N_6	W24	
6	IO_L72P_6	V25	
6	IO_L72N_6	U25	
6	IO_L73P_6	Y28	
6	IO_L73N_6	W28	
6	IO_L74P_6	W23	
6	IO_L74N_6	V23	
6	IO_L75P_6	Y30	
6	IO_L75N_6/VREF_6	W30	
6	IO_L76P_6	Y31	
6	IO_L76N_6	W31	
6	IO_L77P_6	V27	
6	IO_L77N_6	U27	
6	IO_L78P_6	W29	
6	IO_L78N_6	U29	
6	IO_L91P_6	U23	
6	IO_L91N_6	T23	
6	IO_L92P_6	U26	
6	IO_L92N_6	T26	
6	IO_L93P_6	V28	
6	IO_L93N_6/VREF_6	U28	
6	IO_L94P_6	U24	
6	IO_L94N_6	T24	
6	IO_L95P_6	V30	
6	IO_L95N_6	U30	
6	IO_L96P_6	V31	
6	IO_L96N_6	U31	
7	IO_L96P_7	T27	