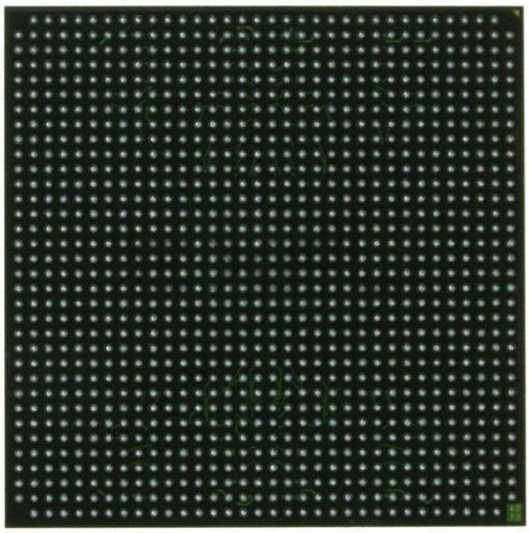

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	5760
Number of Logic Elements/Cells	-
Total RAM Bits	2211840
Number of I/O	824
Number of Gates	4000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v4000-5ffg1152i

Architecture

Virtex-II Array Overview

Virtex-II devices are user-programmable gate arrays with various configurable elements. The Virtex-II architecture is optimized for high-density and high-performance logic designs. As shown in Figure 1, the programmable device is comprised of input/output blocks (IOBs) and internal configurable logic blocks (CLBs).

Programmable I/O blocks provide the interface between package pins and the internal configurable logic. Most popular and leading-edge I/O standards are supported by the programmable IOBs.

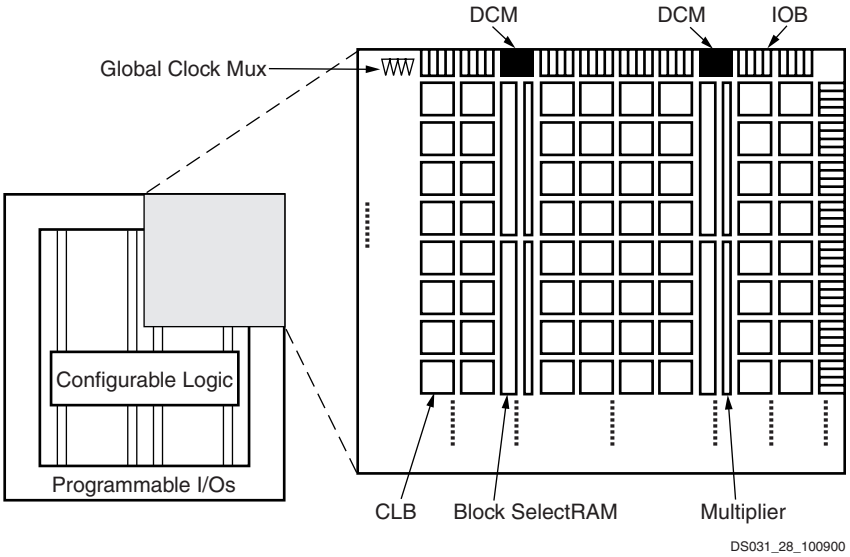


Figure 1: **Virtex-II Architecture Overview**

The internal configurable logic includes four major elements organized in a regular array.

- Configurable Logic Blocks (CLBs) provide functional elements for combinatorial and synchronous logic, including basic storage elements. BUFTs (3-state buffers) associated with each CLB element drive dedicated segmentable horizontal routing resources.
- Block SelectRAM memory modules provide large 18 Kbit storage elements of dual-port RAM.
- Multiplier blocks are 18-bit x 18-bit dedicated multipliers.
- DCM (Digital Clock Manager) blocks provide self-calibrating, fully digital solutions for clock distribution delay compensation, clock multiplication and division, coarse- and fine-grained clock phase shifting.

A new generation of programmable routing resources called Active Interconnect Technology interconnects all of these elements. The general routing matrix (GRM) is an array of routing switches. Each programmable element is tied to a switch matrix, allowing multiple connections to the general routing matrix. The overall programmable interconnection is hierarchical and designed to support high-speed designs.

All programmable elements, including the routing resources, are controlled by values stored in static memory cells. These values are loaded in the memory cells during configuration and can be reloaded to change the functions of the programmable elements.

Virtex-II Features

This section briefly describes Virtex-II features.

Input/Output Blocks (IOBs)

IOBs are programmable and can be categorized as follows:

- Input block with an optional single-data-rate or double-data-rate (DDR) register
- Output block with an optional single-data-rate or DDR register, and an optional 3-state buffer, to be driven directly or through a single or DDR register
- Bidirectional block (any combination of input and output configurations)

These registers are either edge-triggered D-type flip-flops or level-sensitive latches.

IOBs support the following single-ended I/O standards:

- LVTTL, LVCMOS (3.3V, 2.5V, 1.8V, and 1.5V)
- PCI-X compatible (133 MHz and 66 MHz) at 3.3V
- PCI compliant (66 MHz and 33 MHz) at 3.3V
- CardBus compliant (33 MHz) at 3.3V
- GTL and GTLP

Figure 18, Figure 19, and Figure 20 illustrate various example configurations.

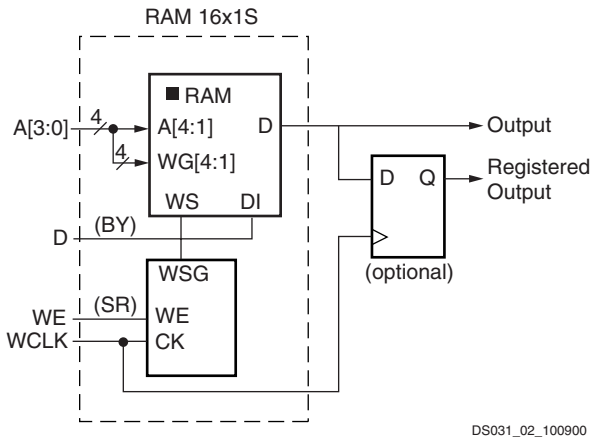


Figure 18: **Distributed SelectRAM (RAM16x1S)**

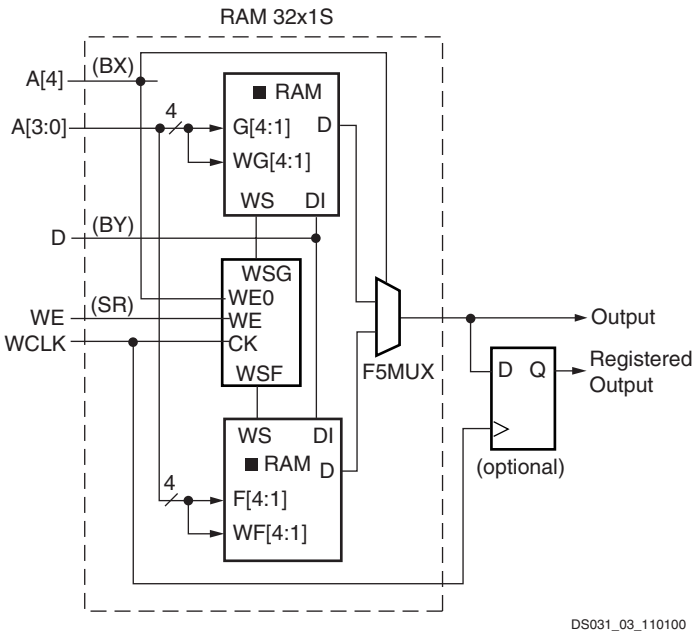


Figure 19: **Single-Port Distributed SelectRAM (RAM32x1S)**

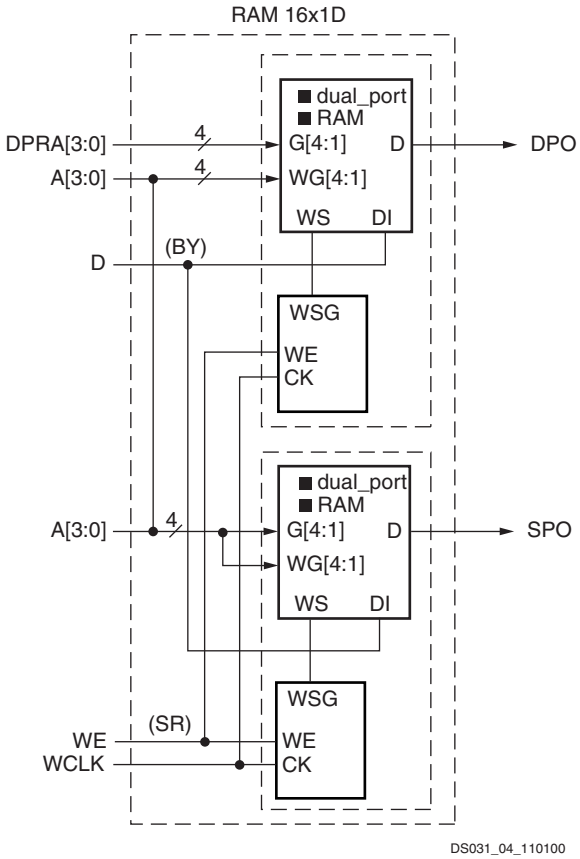


Figure 20: **Dual-Port Distributed SelectRAM (RAM16x1D)**

Similar to the RAM configuration, each function generator (LUT) can implement a 16 x 1-bit ROM. Five configurations are available: ROM16x1, ROM32x1, ROM64x1, ROM128x1, and ROM256x1. The ROM elements are cascadable to implement wider or/and deeper ROM. ROM contents are loaded at configuration. Table 10 shows the number of LUTs occupied by each configuration.

Table 10: **ROM Configuration**

ROM	Number of LUTs
16 x 1	1
32 x 1	2
64 x 1	4
128 x 1	8 (1 CLB)
256 x 1	16 (2 CLBs)

Shift Registers

Each function generator can also be configured as a 16-bit shift register. The write operation is synchronous with a clock input (CLK) and an optional clock enable, as shown in Figure 21. A dynamic read access is performed through the 4-bit address bus, A[3:0]. The configurable 16-bit shift register cannot be set or reset. The read is asynchronous, however the storage element or flip-flop is available to implement a synchronous read. The storage element should always be used with a constant address. For example, when building an 8-bit shift register and configuring the addresses to point to the 7th bit, the 8th bit can be the flip-flop. The overall system performance is improved by using the superior clock-to-out of the flip-flops.

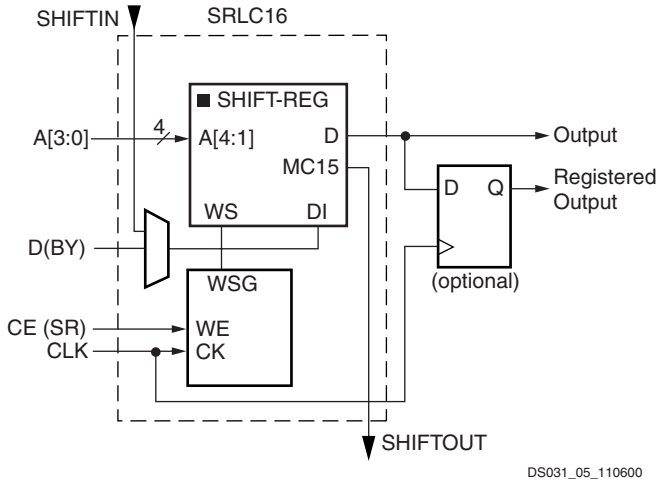


Figure 21: **Shift Register Configurations**

An additional dedicated connection between shift registers allows connecting the last bit of one shift register to the first bit of the next, without using the ordinary LUT output. (See Figure 22.) Longer shift registers can be built with dynamic access to any bit in the chain. The shift register chaining and the MUXF5, MUXF6, and MUXF7 multiplexers allow up to a 128-bit shift register with addressable access to be implemented in one CLB.

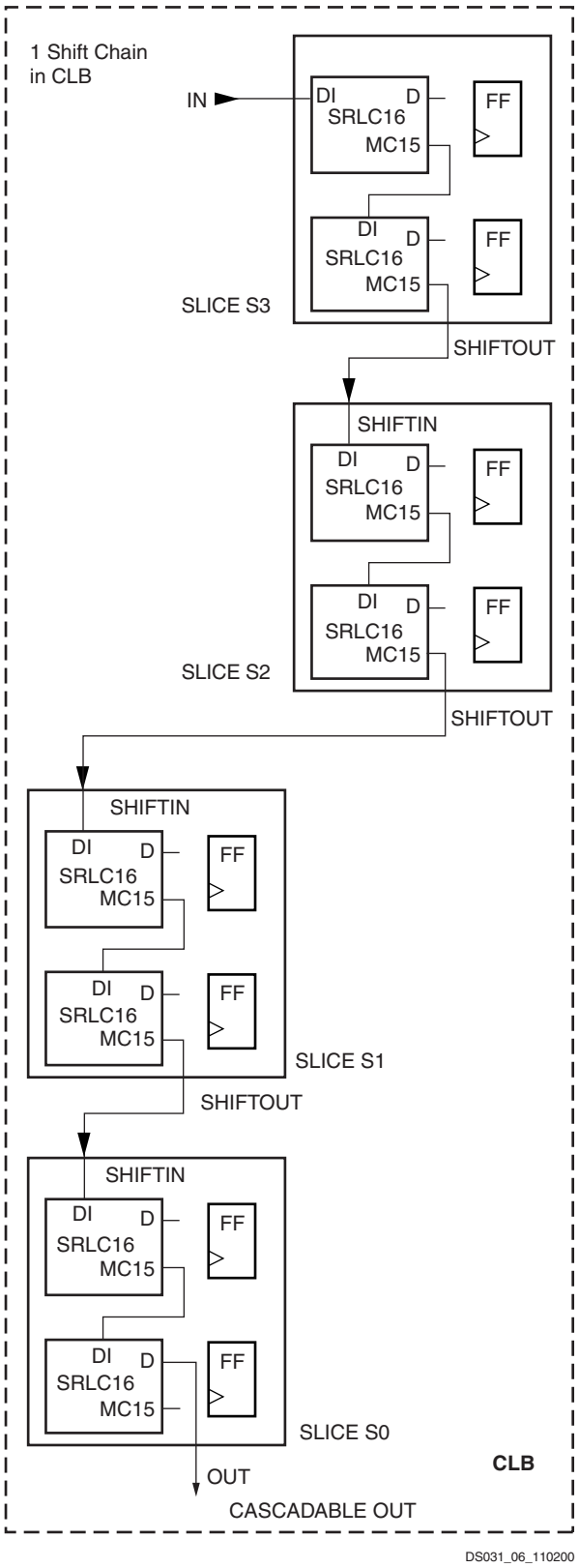


Figure 22: **Cascadable Shift Register**

Table 17: **IOB Output Switching Characteristics Standard Adjustments *(Continued)***

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-6	-5	-4	
LVCMOS, 2.5V, Fast, 16 mA	LVCMOS25_F16	$T_{OLVCMOS25\_F16}$	–0.18	–0.19	–0.21	ns
LVCMOS, 2.5V, Fast, 24 mA	LVCMOS25_F24	$T_{OLVCMOS25\_F24}$	–0.35	–0.36	–0.40	ns
LVCMOS, 1.8V, Slow, 2 mA	LVCMOS18_S2	$T_{OLVCMOS18\_S2}$	15.62	16.10	17.71	ns
LVCMOS, 1.8V, Slow, 4 mA	LVCMOS18_S4	$T_{OLVCMOS18\_S4}$	10.20	10.51	11.57	ns
LVCMOS, 1.8V, Slow, 6 mA	LVCMOS18_S6	$T_{OLVCMOS18\_S6}$	7.52	7.75	8.53	ns
LVCMOS, 1.8V, Slow, 8 mA	LVCMOS18_S8	$T_{OLVCMOS18\_S8}$	6.87	7.08	7.78	ns
LVCMOS, 1.8V, Slow, 12 mA	LVCMOS18_S12	$T_{OLVCMOS18\_S12}$	5.54	5.71	6.28	ns
LVCMOS, 1.8V, Slow, 16 mA	LVCMOS18_S16	$T_{OLVCMOS18\_S16}$	5.31	5.47	6.02	ns
LVCMOS, 1.8V, Fast, 2 mA	LVCMOS18_F2	$T_{OLVCMOS18\_F2}$	5.55	5.72	6.30	ns
LVCMOS, 1.8V, Fast, 4 mA	LVCMOS18_F4	$T_{OLVCMOS18\_F4}$	1.89	1.95	2.15	ns
LVCMOS, 1.8V, Fast, 6 mA	LVCMOS18_F6	$T_{OLVCMOS18\_F6}$	0.83	0.85	0.94	ns
LVCMOS, 1.8V, Fast, 8 mA	LVCMOS18_F8	$T_{OLVCMOS18\_F8}$	0.70	0.72	0.80	ns
LVCMOS, 1.8V, Fast, 12 mA	LVCMOS18_F12	$T_{OLVCMOS18\_F12}$	0.26	0.27	0.30	ns
LVCMOS, 1.8V, Fast, 16 mA	LVCMOS18_F16	$T_{OLVCMOS18\_F16}$	0.23	0.23	0.26	ns
LVCMOS, 1.5V, Slow, 2 mA	LVCMOS15_S2	$T_{OLVCMOS15\_S2}$	18.96	19.55	21.50	ns
LVCMOS, 1.5V, Slow, 4 mA	LVCMOS15_S4	$T_{OLVCMOS15\_S4}$	12.77	13.17	14.48	ns
LVCMOS, 1.5V, Slow, 6 mA	LVCMOS15_S6	$T_{OLVCMOS15\_S6}$	12.05	12.42	13.66	ns
LVCMOS, 1.5V, Slow, 8 mA	LVCMOS15_S8	$T_{OLVCMOS15\_S8}$	9.75	10.06	11.06	ns
LVCMOS, 1.5V, Slow, 12 mA	LVCMOS15_S12	$T_{OLVCMOS15\_S12}$	9.04	9.32	10.25	ns
LVCMOS, 1.5V, Slow, 16 mA	LVCMOS15_S16	$T_{OLVCMOS15\_S16}$	8.21	8.46	9.31	ns
LVCMOS, 1.5V, Fast, 2 mA	LVCMOS15_F2	$T_{OLVCMOS15\_F2}$	5.09	5.25	5.78	ns
LVCMOS, 1.5V, Fast, 4 mA	LVCMOS15_F4	$T_{OLVCMOS15\_F4}$	2.01	2.07	2.27	ns
LVCMOS, 1.5V, Fast, 6 mA	LVCMOS15_F6	$T_{OLVCMOS15\_F6}$	1.46	1.51	1.66	ns
LVCMOS, 1.5V, Fast, 8 mA	LVCMOS15_F8	$T_{OLVCMOS15\_F8}$	0.93	0.96	1.05	ns
LVCMOS, 1.5V, Fast, 12 mA	LVCMOS15_F12	$T_{OLVCMOS15\_F12}$	0.74	0.77	0.84	ns
LVCMOS, 1.5V, Fast, 16 mA	LVCMOS15_F16	$T_{OLVCMOS15\_F16}$	0.67	0.69	0.75	ns
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	T_{OLVDS_25}	–0.31	–0.32	–0.36	ns
LVDS, 3.3V	LVDS_33	T_{OLVDS_33}	–0.25	–0.26	–0.29	ns
LVDSEXT (LVDS Extended Mode), 2.5V	LVDSEXT_25	$T_{OLVDSEXT\_25}$	–0.18	–0.19	–0.21	ns
LVDSEXT, 3.3V	LVDSEXT_33	$T_{OLVDSEXT\_33}$	–0.17	–0.18	–0.19	ns
ULVDS (Ultra LVDS), 2.5V	ULVDS_25	T_{OULVDS_25}	–0.20	–0.21	–0.23	ns
BLVDS (Bus LVDS), 2.5V	BLVDS_25	T_{OBLVDS_25}	0.67	0.69	0.76	ns
LDT (HyperTransport), 2.5V	LDT_25	T_{OLDT_25}	–0.20	–0.21	–0.23	ns
LVPECL (Low-Voltage Positive Electron-Coupled Logic), 3.3V	LVPECL_33	$T_{OLVPECL\_33}$	0.29	0.30	0.33	ns
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3	T_{OPCI33_3}	1.15	1.19	1.31	ns
PCI, 66 MHz, 3.3V	PCI66_3	T_{OPCI66_3}	–0.01	–0.01	–0.01	ns
PCI-X, 133 MHz, 3.3V	PCIX	T_{OPCIX}	–0.01	–0.01	–0.01	ns
GTL (Gunning Transceiver Logic)	GTL	T_{OGTL}	–0.31	–0.32	–0.36	ns
GTL Plus	GTLP	T_{OGTLP}	–0.17	–0.18	–0.20	ns
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	T_{OHSTL_I}	0.26	0.27	0.29	ns
HSTL, Class II	HSTL_II	T_{OHSTL_II}	–0.15	–0.16	–0.17	ns
HSTL, Class III	HSTL_III	T_{OHSTL_III}	–0.17	–0.17	–0.19	ns
HSTL, Class IV	HSTL_IV	T_{OHSTL_IV}	–0.40	–0.41	–0.45	ns
HSTL, Class I, 1.8V	HSTL_I_18	$T_{OHSTL\_I\_18}$	0.03	0.03	0.04	ns

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 18 shows the test setup parameters used for measuring Input standard adjustments (see Table 15, page 11).

Table 18: **Input Delay Measurement Methodology**

Description	IOSTANDARD Attribute	V_L (1,2)	V_H (1,2)	V_{MEAS} (1,4,5)	V_{REF} (1,3,5)
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL	0	3.0	1.4	–
LVCMOS (Low-Voltage CMOS), 3.3V	LVCMOS33	0	3.3	1.65	–
LVCMOS, 2.5V	LVCMOS25	0	2.5	1.25	–
LVCMOS, 1.8V	LVCMOS18	0	1.8	0.9	–
LVCMOS, 1.5V	LVCMOS15	0	1.5	0.75	–
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3	Per PCI Specification			–
PCI, 66 MHz, 3.3V	PCI66_3	Per PCI Specification			–
PCI-X, 133 MHz, 3.3V	PCIX	Per PCI-X Specification			–
GTL (Gunning Transceiver Logic)	GTL	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	0.80
GTL Plus	GTLP	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	1.0
HSTL (High-Speed Transceiver Logic), Class I & II	HSTL_I, HSTL_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.75
HSTL, Class III & IV	HSTL_III, HSTL_IV	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL, Class III & IV, 1.8V	HSTL_III_18, HSTL_IV_18	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	1.08
SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V	SSTL3_I, SSTL3_II	V_{REF} – 1.00	V_{REF} + 1.00	V_{REF}	1.5
SSTL, Class I & II, 2.5V	SSTL2_I, SSTL2_II	V_{REF} – 0.75	V_{REF} + 0.75	V_{REF}	1.25
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
AGP-2X/AGP (Accelerated Graphics Port)	AGP	V_{REF} – (0.2 x V_{CCO})	V_{REF} + (0.2 x V_{CCO})	V_{REF}	AGP Spec
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	1.2 – 0.125	1.2 + 0.125	1.2	
LVDS, 3.3V	LVDS_33	1.2 – 0.125	1.2 + 0.125	1.2	
LVDSEXT (LVDS Extended Mode), 2.5V	LVDSEXT_25	1.2 – 0.125	1.2 + 0.125	1.2	
LVDSEXT, 3.3V	LVDSEXT_33	1.2 – 0.125	1.2 + 0.125	1.2	
ULVDS (Ultra LVDS), 2.5V	ULVDS_25	0.6 – 0.125	0.6 + 0.125	0.6	
LDT (HyperTransport), 2.5V	LDT_25	0.6 – 0.125	0.6 + 0.125	0.6	
LVPECL (Low-Voltage Positive Electron-Coupled Logic), 3.3V	LVPECL_33	1.6 – 0.3	1.6 + 0.3	1.6	

Notes:
1. Input delay measurement methodology parameters for LVDCI and HSLVDCI are the same as for LVCMOS standards of the same voltage. Parameters for all other DCI standards are the same as for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H.
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical. See **Virtex-II Platform FPGA User Guide** for min/max specifications.
4. Input voltage level from which measurement starts.
5. Note that this is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 1.

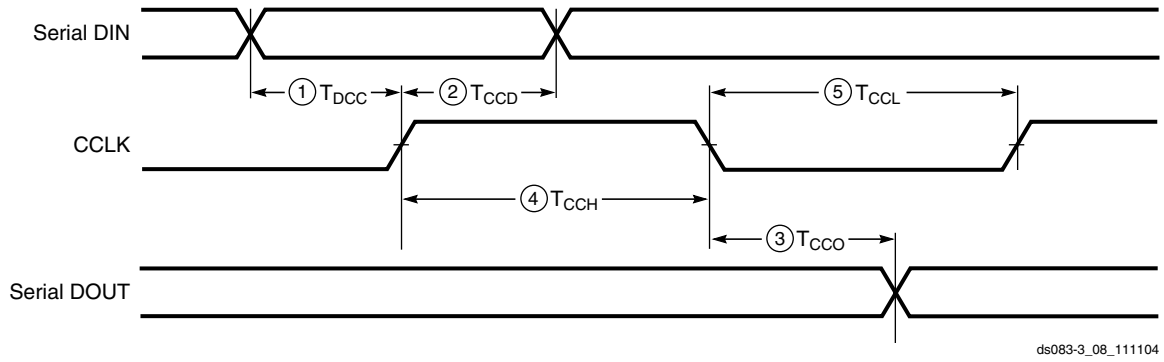


Figure 3: **Slave Serial Mode Timing Sequence**

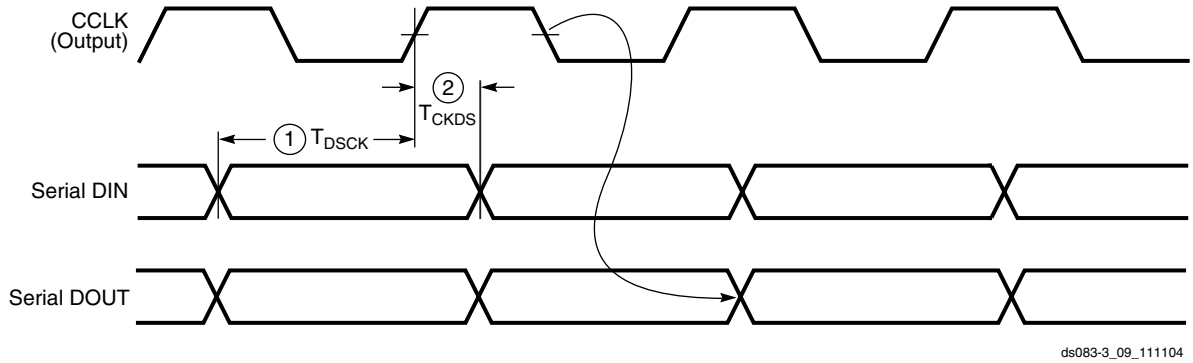


Figure 4: **Master Serial Mode Timing Sequence**

Table 31: **Master/Slave Serial Mode Timing Characteristics**

	Description	Figure References	Symbol	Value	Units
CCLK	DIN setup/hold, slave mode (Figure 3)	1/2	T_{DCC}/T_{CCD}	5.0/0.0	ns, min
	DIN setup/hold, master mode (Figure 4)	1/2	T_{DSCK}/T_{CKDS}	5.0/0.0	ns, min
	DOUT	3	T_{CCO}	12.0	ns, max
	High time	4	T_{CCH}	5.0	ns, min
	Low time	5	T_{CCL}	5.0	ns, min
	Maximum start-up frequency		$F_{CC\_STARTUP}$	50	MHz, max
	Maximum frequency		F_{CC_SERIAL}	66(1)	MHz, max
	Frequency tolerance, master mode with respect to nominal			+45% –30%	

Notes:
1. If no provision is made in the design to adjust the frequency of CCLK, F_{CC_SERIAL} should not exceed $F_{CC\_STARTUP}$.

Master/Slave SelectMAP Parameters

Figure 5 is a generic timing diagram for data loading using SelectMAP. For other data loading diagrams, refer to the ***Virtex-II Pro Platform FPGA User Guide***.

Table 47: **Sample Window**

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
Sampling Error at Receiver Pins(1)	T_{SAMP}	XC2V40	500	500	550	ps
		XC2V80	500	500	550	ps
		XC2V250	500	500	550	ps
		XC2V500	500	500	550	ps
		XC2V1000	500	500	550	ps
		XC2V1500	500	500	550	ps
		XC2V2000	500	500	550	ps
		XC2V3000	500	500	550	ps
		XC2V4000	500	500	550	ps
		XC2V6000	500	500	550	ps
		XC2V8000		500	550	ps

Notes:
1. This parameter indicates the total sampling error of Virtex-II DDR input registers across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 and CLK180 DCM jitter
   - Worst-case Duty-Cycle Distortion - T_{DCD_CLK180}
   - DCM accuracy (phase offset)
   - DCM phase shift resolution.

   These measurements do not include package or clock tree skew.

Table 48: **Pin-to-Pin Setup/Hold: Source-Synchronous Configuration**

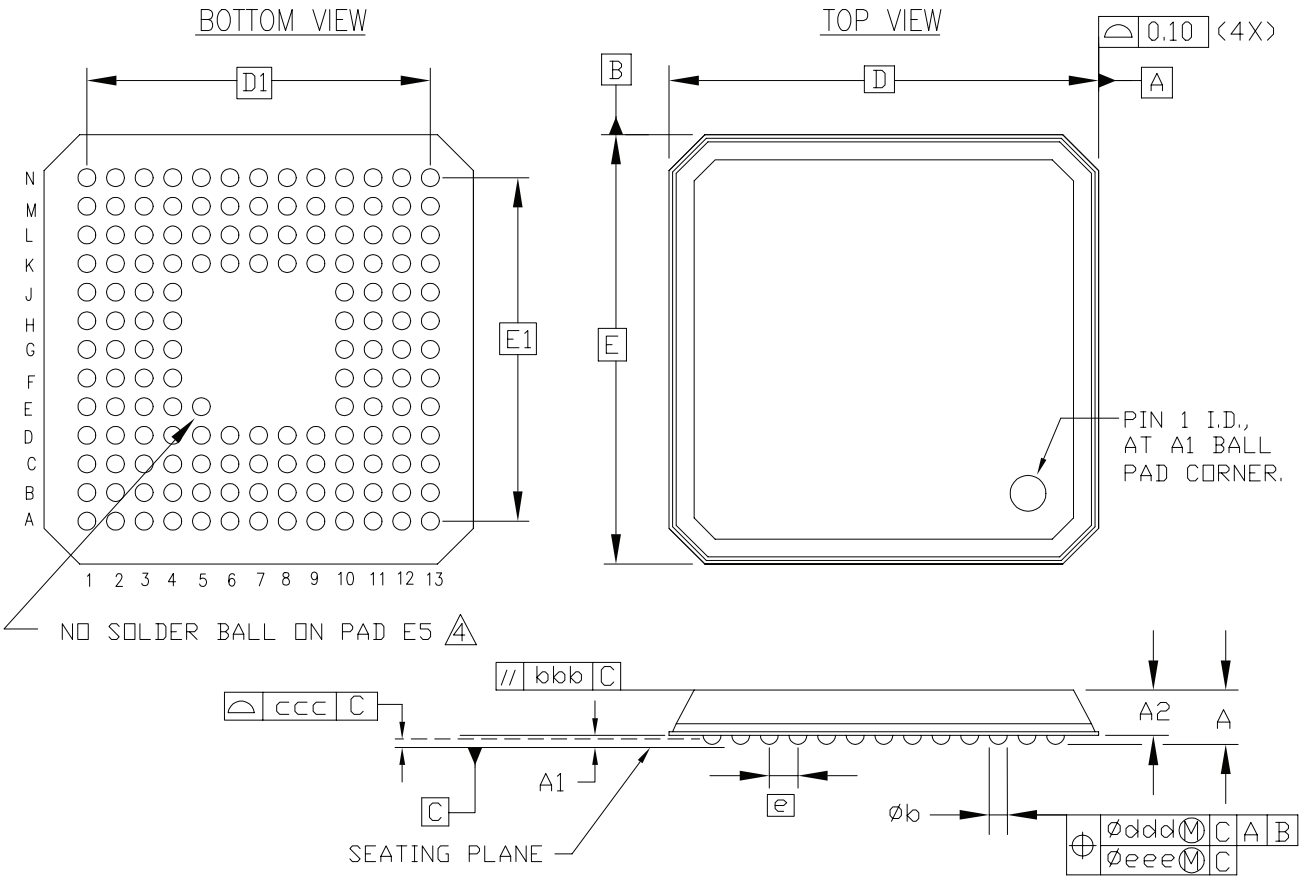
Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
Data Input Set-Up and Hold Times Relative to a Forwarded Clock Input Pin, Using DCM and Global Clock Buffer. For situations where clock and data inputs conform to different standards, adjust the setup and hold values accordingly using the values shown in IOB Input Switching Characteristics Standard Adjustments, page 11.						
No Delay Global Clock and IFF with DCM	T_{PSDCM}/ T_{PHDCM}	XC2V40	0.2/0.5	0.2/0.5	0.2/0.5	ns
		XC2V80	0.2/0.5	0.2/0.5	0.2/0.5	ns
		XC2V250	0.2/0.5	0.2/0.5	0.2/0.5	ns
		XC2V500	0.2/0.5	0.2/0.5	0.2/0.5	ns
		XC2V1000	0.2/0.5	0.2/0.5	0.2/0.5	ns
		XC2V1500	0.2/0.5	0.2/0.5	0.2/0.5	ns
		XC2V2000	0.2/0.5	0.2/0.5	0.2/0.5	ns
		XC2V3000	0.2/0.5	0.2/0.5	0.2/0.6	ns
		XC2V4000	0.2/0.5	0.2/0.6	0.2/0.6	ns
		XC2V6000	0.2/0.5	0.2/0.6	0.2/0.6	ns
		XC2V8000		0.2/0.6	0.2/0.7	ns

Notes:
1. IFF = Input Flip-Flop
2. The timing values were measured using the fine-phase adjustment feature of the DCM.
3. The worst-case duty-cycle distortion and DCM jitter on CLK0 and CLK180 is included in these measurements.

Table 5: **CS144/CSG144 — XC2V40, XC2V80, and XC2V250**

Bank	Pin Description	Pin Number	No Connect in the XC2V40
2	IO_L96N_2	G11	
2	IO_L96P_2	G13	
3	IO_L96N_3	G12	
3	IO_L96P_3	H12	
3	IO_L94N_3	H11	
3	IO_L94P_3	J13	
3	IO_L03N_3/VREF_3	J10	
3	IO_L03P_3	K13	
3	IO_L02N_3/VRP_3	K12	
3	IO_L02P_3/VRN_3	K11	
3	IO_L01N_3	K10	
3	IO_L01P_3	L13	
4	IO_L01N_4/BUSY/DOUT(1)	M11	
4	IO_L01P_4/INIT_B	N11	
4	IO_L02N_4/D0/DIN(1)	L10	
4	IO_L02P_4/D1	M10	
4	IO_L03N_4/D2/ALT_VRP_4	N10	
4	IO_L03P_4/D3/ALT_VRN_4	K9	
4	IO_L94N_4/VREF_4	N9	
4	IO_L94P_4	K8	
4	IO_L95N_4/GCLK3S	L8	
4	IO_L95P_4/GCLK2P	M8	
4	IO_L96N_4/GCLK1S	N8	
4	IO_L96P_4/GCLK0P	K7	
5	IO_L96N_5/GCLK7S	N7	
5	IO_L96P_5/GCLK6P	M7	
5	IO_L95N_5/GCLK5S	N6	
5	IO_L95P_5/GCLK4P	M6	
5	IO_L94N_5	L6	
5	IO_L94P_5/VREF_5	K6	
5	IO_L03N_5/D4/ALT_VRP_5	L5	
5	IO_L03P_5/D5/ALT_VRN_5	K5	
5	IO_L02N_5/D6	N4	
5	IO_L02P_5/D7	M4	
5	IO_L01N_5/RDWR_B	L4	
5	IO_L01P_5/CS_B	K4	

CS144/CSG144 Chip-Scale BGA Package Specifications (0.80mm pitch)



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A	~	~	1.20
A_1	0.20	~	~
A_2	0.65	~	~
D/E	12.00 BSC		
D_1/E_1	9.60 BSC		
e	0.80 BSC		
øb	0.40	0.45	0.50
bbb	~	~	0.20
ccc	~	~	0.12
ddd	~	~	0.15
eee	~	~	0.08
M	13		

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MO–216–BAG–2 (DEPOPULATED).
4. PAD 'E5' IS FOR PAD 'A1' CORNER INDICATION.

144–BALL CHIP SCALE BGA (CS144/CSG144)

Figure 1: **CS144/CSG144 Chip-Scale BGA Package Specifications**

Table 6: **FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
6	VCCO_6	J5		
7	VCCO_7	H6		
7	VCCO_7	H5		
7	VCCO_7	G6		
NA	CCLK	P15		
NA	PROG_B	A2		
NA	DONE	R14		
NA	M0	T2		
NA	M1	P2		
NA	M2	R3		
NA	HSWAP_EN	B3		
NA	TCK	A15		
NA	TDI	C2		
NA	TDO	C15		
NA	TMS	B14		
NA	PWRDWN_B	T15		
NA	RSVD	A4		
NA	RSVD	A3		
NA	VBATT	A14		
NA	RSVD	A13		
NA	VCCAUX	R16		
NA	VCCAUX	R1		
NA	VCCAUX	B16		
NA	VCCAUX	B1		
NA	VCCINT	N13		
NA	VCCINT	N4		
NA	VCCINT	M12		
NA	VCCINT	M5		
NA	VCCINT	E12		
NA	VCCINT	E5		
NA	VCCINT	D13		
NA	VCCINT	D4		

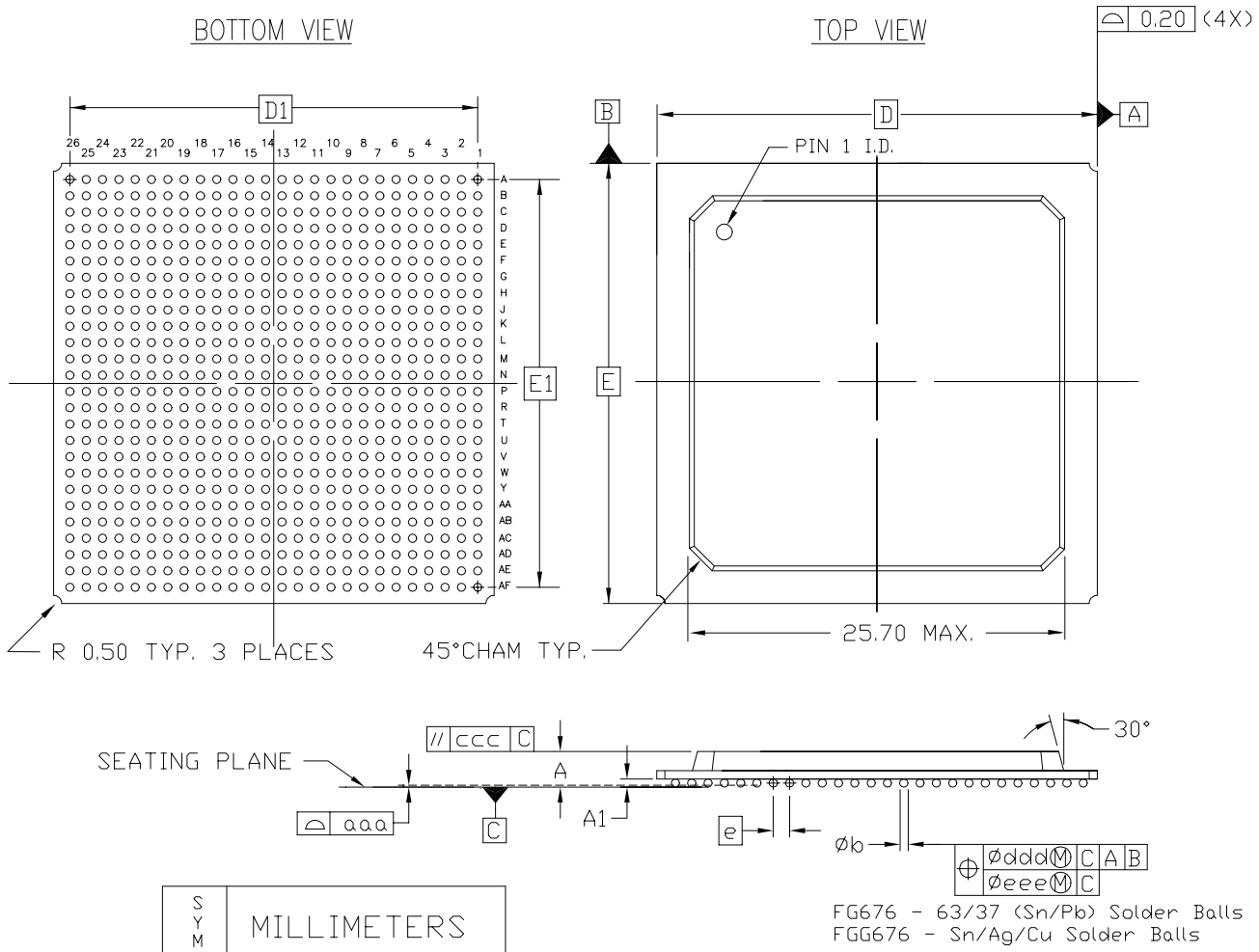
Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
2	IO_L45N_2	H19		
2	IO_L45P_2/VREF_2	H20		
2	IO_L46N_2	H21		
2	IO_L46P_2	H22		
2	IO_L48N_2	J17		
2	IO_L48P_2	J18		
2	IO_L49N_2	J19	NC	
2	IO_L49P_2	J20	NC	
2	IO_L51N_2	J21	NC	
2	IO_L51P_2/VREF_2	J22	NC	
2	IO_L52N_2	K17	NC	
2	IO_L52P_2	K18	NC	
2	IO_L54N_2	K19	NC	
2	IO_L54P_2	K20	NC	
2	IO_L91N_2	K21		
2	IO_L91P_2	K22		
2	IO_L93N_2	L17		
2	IO_L93P_2/VREF_2	L18		
2	IO_L94N_2	L19		
2	IO_L94P_2	L20		
2	IO_L96N_2	L21		
2	IO_L96P_2	L22		
3	IO_L96N_3	M21		
3	IO_L96P_3	M20		
3	IO_L94N_3	M19		
3	IO_L94P_3	M18		
3	IO_L93N_3/VREF_3	M17		
3	IO_L93P_3	N17		
3	IO_L91N_3	N22		
3	IO_L91P_3	N21		
3	IO_L54N_3	N20	NC	
3	IO_L54P_3	N19	NC	
3	IO_L52N_3	N18	NC	

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
5	IO_L70N_5	W11		
5	IO_L70P_5	Y10		
5	IO_L69N_5/VREF_5	Y11		
5	IO_L69P_5	AA11		
5	IO_L67N_5	AF9		
5	IO_L67P_5	AF8		
5	IO_L54N_5	AE9		
5	IO_L54P_5	AD9		
5	IO_L52N_5	AB10		
5	IO_L52P_5	AA10		
5	IO_L51N_5/VREF_5	AD10		
5	IO_L51P_5	AC10		
5	IO_L49N_5	AE8		
5	IO_L49P_5	AF7		
5	IO_L28N_5	AD8	NC	NC
5	IO_L28P_5	AC8	NC	NC
5	IO_L27N_5/VREF_5	AB9	NC	NC
5	IO_L27P_5	AC9	NC	NC
5	IO_L25N_5	AA9	NC	NC
5	IO_L25P_5	Y9	NC	NC
5	IO_L24N_5	AF6		
5	IO_L24P_5	AE6		
5	IO_L22N_5	AB8		
5	IO_L22P_5	AA8		
5	IO_L21N_5/VREF_5	AC7		
5	IO_L21P_5	AD7		
5	IO_L19N_5	AF5		
5	IO_L19P_5	AE5		
5	IO_L06N_5	AF4		
5	IO_L06P_5	AE4		
5	IO_L05N_5/VRP_5	AF3		
5	IO_L05P_5/VRN_5	AE3		
5	IO_L04N_5	Y8		
5	IO_L04P_5/VREF_5	Y7		
5	IO_L03N_5/D4/ALT_VRP_5	AB7		
5	IO_L03P_5/D5/ALT_VRN_5	AA7		
5	IO_L02N_5/D6	AD6		

FG676/FGG676 Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A		2.25	2.60
A_1	0.40	0.50	0.60
D/E	27.00 BSC		
D_1/E_1	25.00 REF		
e	1.00 BSC		
øb	0.50	0.60	0.70
aaa			0.20
ccc			0.35
ddd			0.30
eee			0.10
M	26		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-AAL-1

676-BALL FINE PITCH BGA (FG676/FGG676)

Figure 4: **FG676/FGG676 Fine-Pitch BGA Package Specifications**

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
7	VCCO_7	F3		
NA	CCLK	AB23		
NA	PROG_B	C1		
NA	DONE	AB21		
NA	M0	AC4		
NA	M1	AB4		
NA	M2	AD3		
NA	HSWAP_EN	C2		
NA	TCK	C23		
NA	TDI	D1		
NA	TDO	C24		
NA	TMS	C21		
NA	PWRDWN_B	AC21		
NA	DXN	B4		
NA	DXP	C4		
NA	VBATT	B21		
NA	RSVD	A22		
NA	VCCAUX	AD13		
NA	VCCAUX	AC22		
NA	VCCAUX	AC3		
NA	VCCAUX	N1		
NA	VCCAUX	M24		
NA	VCCAUX	B22		
NA	VCCAUX	B3		
NA	VCCAUX	A12		
NA	VCCINT	U17		
NA	VCCINT	U8		
NA	VCCINT	T16		
NA	VCCINT	T9		
NA	VCCINT	R15		
NA	VCCINT	R14		
NA	VCCINT	R13		
NA	VCCINT	R12		
NA	VCCINT	R11		

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
3	IO_L72N_3	T20
3	IO_L72P_3	T19
3	IO_L70N_3	U27
3	IO_L70P_3	U26
3	IO_L69N_3/VREF_3	U25
3	IO_L69P_3	V25
3	IO_L67N_3	U21
3	IO_L67P_3	U20
3	IO_L54N_3	V27
3	IO_L54P_3	V26
3	IO_L52N_3	V24
3	IO_L52P_3	V23
3	IO_L51N_3/VREF_3	V22
3	IO_L51P_3	W22
3	IO_L49N_3	V21
3	IO_L49P_3	V20
3	IO_L48N_3	W27
3	IO_L48P_3	Y27
3	IO_L46N_3	W26
3	IO_L46P_3	W25
3	IO_L45N_3/VREF_3	W24
3	IO_L45P_3	W23
3	IO_L43N_3	W21
3	IO_L43P_3	W20
3	IO_L28N_3	W19
3	IO_L28P_3	Y19
3	IO_L27N_3/VREF_3	Y25
3	IO_L27P_3	Y24
3	IO_L25N_3	Y23
3	IO_L25P_3	AA23
3	IO_L24N_3	Y22
3	IO_L24P_3	Y21
3	IO_L22N_3	AA27
3	IO_L22P_3	AB27
3	IO_L21N_3/VREF_3	AA26
3	IO_L21P_3	AA25

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
3	IO_L19N_3	AB26
3	IO_L19P_3	AB25
3	IO_L06N_3	AB24
3	IO_L06P_3	AB23
3	IO_L04N_3	AC27
3	IO_L04P_3	AC26
3	IO_L03N_3/VREF_3	AC25
3	IO_L03P_3	AC24
3	IO_L02N_3/VRP_3	AD27
3	IO_L02P_3/VRN_3	AE27
3	IO_L01N_3	AD26
3	IO_L01P_3	AD25
4	IO_L01N_4/BUSY/DOUT(1)	AF25
4	IO_L01P_4/INIT_B	AG25
4	IO_L02N_4/D0/DIN(1)	AF24
4	IO_L02P_4/D1	AG24
4	IO_L03N_4/D2/ALT_VRP_4	AD23
4	IO_L03P_4/D3/ALT_VRN_4	AE23
4	IO_L04N_4/VREF_4	AF23
4	IO_L04P_4	AG23
4	IO_L05N_4/VRP_4	AD22
4	IO_L05P_4/VRN_4	AE22
4	IO_L06N_4	AF22
4	IO_L06P_4	AG22
4	IO_L19N_4	AC21
4	IO_L19P_4	AB21
4	IO_L21N_4	AE21
4	IO_L21P_4/VREF_4	AE20
4	IO_L22N_4	AF21
4	IO_L22P_4	AG21
4	IO_L24N_4	AB20
4	IO_L24P_4	AA20
4	IO_L25N_4	AC20
4	IO_L25P_4	AD20
4	IO_L27N_4	AG20

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
NA	VCCINT	K10
NA	GND	AG27
NA	GND	AG26
NA	GND	AG14
NA	GND	AG2
NA	GND	AG1
NA	GND	AF27
NA	GND	AF26
NA	GND	AF20
NA	GND	AF8
NA	GND	AF2
NA	GND	AF1
NA	GND	AE25
NA	GND	AE3
NA	GND	AD24
NA	GND	AD14
NA	GND	AD4
NA	GND	AC23
NA	GND	AC17
NA	GND	AC11
NA	GND	AC5
NA	GND	AB22
NA	GND	AB6
NA	GND	AA21
NA	GND	AA7
NA	GND	Y26
NA	GND	Y20
NA	GND	Y8
NA	GND	Y2
NA	GND	W14
NA	GND	U23
NA	GND	U5
NA	GND	T16
NA	GND	T15
NA	GND	T14
NA	GND	T13

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
4	IO_L20N_4	AJ10	
4	IO_L20P_4	AJ9	
4	IO_L21N_4	AH9	
4	IO_L21P_4/VREF_4	AH10	
4	IO_L22N_4	AN5	
4	IO_L22P_4	AN4	
4	IO_L23N_4	AE12	
4	IO_L23P_4	AE13	
4	IO_L24N_4	AM9	
4	IO_L24P_4	AL8	
4	IO_L25N_4	AP5	
4	IO_L25P_4	AP4	
4	IO_L26N_4	AG11	
4	IO_L26P_4	AG12	
4	IO_L27N_4	AN7	
4	IO_L27P_4/VREF_4	AN6	
4	IO_L28N_4	AL10	
4	IO_L28P_4	AL9	
4	IO_L29N_4	AF12	
4	IO_L29P_4	AF13	
4	IO_L30N_4	AK10	
4	IO_L30P_4	AK11	
4	IO_L49N_4	AP7	
4	IO_L49P_4	AP6	
4	IO_L50N_4	AH13	
4	IO_L50P_4	AH12	
4	IO_L51N_4	AJ11	
4	IO_L51P_4/VREF_4	AJ12	
4	IO_L52N_4	AP9	
4	IO_L52P_4	AN8	
4	IO_L53N_4	AG13	
4	IO_L53P_4	AG14	
4	IO_L54N_4	AM11	
4	IO_L54P_4	AL11	
4	IO_L60N_4	AN10	NC
4	IO_L60P_4	AN9	NC

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
2	VCCO_2	R11	
2	VCCO_2	R5	
2	VCCO_2	P12	
2	VCCO_2	P11	
2	VCCO_2	N12	
2	VCCO_2	N11	
2	VCCO_2	M11	
2	VCCO_2	K1	
2	VCCO_2	G4	
3	VCCO_3	AH4	
3	VCCO_3	AE1	
3	VCCO_3	AC11	
3	VCCO_3	AB12	
3	VCCO_3	AB11	
3	VCCO_3	AA12	
3	VCCO_3	AA11	
3	VCCO_3	Y12	
3	VCCO_3	Y11	
3	VCCO_3	Y5	
3	VCCO_3	W12	
3	VCCO_3	W1	
3	VCCO_3	V12	
4	VCCO_4	AP16	
4	VCCO_4	AP10	
4	VCCO_4	AL7	
4	VCCO_4	AK15	
4	VCCO_4	AD15	
4	VCCO_4	AD14	
4	VCCO_4	AD13	
4	VCCO_4	AD12	
4	VCCO_4	AC17	
4	VCCO_4	AC16	
4	VCCO_4	AC15	
4	VCCO_4	AC14	
4	VCCO_4	AC13	
5	VCCO_5	AP25	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	GND	Y17		
NA	GND	Y16		
NA	GND	Y10		
NA	GND	Y7		
NA	GND	Y4		
NA	GND	Y1		
NA	GND	W24		
NA	GND	W23		
NA	GND	W22		
NA	GND	W21		
NA	GND	W20		
NA	GND	W19		
NA	GND	W18		
NA	GND	W17		
NA	GND	W16		
NA	GND	V24		
NA	GND	V23		
NA	GND	V22		
NA	GND	V21		
NA	GND	V20		
NA	GND	V19		
NA	GND	V18		
NA	GND	V17		
NA	GND	V16		
NA	GND	U36		
NA	GND	U32		
NA	GND	U24		
NA	GND	U23		
NA	GND	U22		
NA	GND	U21		
NA	GND	U20		
NA	GND	U19		
NA	GND	U18		
NA	GND	U17		
NA	GND	U16		
NA	GND	U8		