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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	5760
Number of Logic Elements/Cells	-
Total RAM Bits	2211840
Number of I/O	912
Number of Gates	4000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FCBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v4000-5ffg1517c

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *Without* DCM

Table 35: Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *Without* DCM

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
LVTTL Global Clock Input to Output Delay using Output flip-flop, 12 mA, Fast Slew Rate, <i>without</i> DCM. For data <i>output</i> with different standards, adjust the delays with the values shown in <i>IOB Output Switching Characteristics Standard Adjustments</i> , page 14.						
Global Clock and OFF without DCM	T _{ICKOF}	XC2V40	3.46	3.58	3.69	ns
		XC2V80	3.62	3.58	3.69	ns
		XC2V250	3.79	3.88	4.47	ns
		XC2V500	3.85	3.88	4.47	ns
		XC2V1000	4.02	4.28	4.62	ns
		XC2V1500	4.16	4.28	4.62	ns
		XC2V2000	4.30	4.43	5.10	ns
		XC2V3000	4.49	4.64	5.34	ns
		XC2V4000	4.82	4.99	5.74	ns
		XC2V6000	5.19	5.38	5.93	ns
		XC2V8000		6.09	7.00	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with test setup shown in [Figure 1](#). For other I/O standards, see [Table 19](#).

Input Clock Tolerances

Table 39: Input Clock Tolerances

Description	Symbol	Constraints F _{CLKIN}	Speed Grade						Units
			-6		-5		-4		
			Min	Max	Min	Max	Min	Max	
Input Clock Low/High Pulse Width									
PSCLK	PSCLK_PULSE	< 1MHz	25.00		25.00		25.00		ns
PSCLK and CLKIN ⁽³⁾	PSCLK_PULSE and CLKIN_PULSE	1 – 10 MHz	25.00		25.00		25.00		ns
		10 – 25 MHz	10.00		10.00		10.00		ns
		25 – 50 MHz	5.00		5.00		5.00		ns
		50 – 100 MHz	3.00		3.00		3.00		ns
		100 – 150 MHz	2.40		2.40		2.40		ns
		150 – 200 MHz	2.00		2.00		2.00		ns
		200 – 250 MHz	1.80		1.80		1.80		ns
		250 – 300 MHz	1.50		1.50		1.50		ns
		300 – 350 MHz	1.30		1.30		1.30		ns
		350 – 400 MHz	1.15		1.15		1.15		ns
> 400 MHz	1.05		1.05		1.05		ns		
Input Clock Cycle-Cycle Jitter (Low Frequency Mode)									
CLKIN (using DLL outputs) ⁽¹⁾	CLKIN_CYC_JITT_DLL_LF			±300		±300		±300	ps
CLKIN (using CLKFX outputs) ⁽²⁾	CLKIN_CYC_JITT_FX_LF			±300		±300		±300	ps
Input Clock Cycle-Cycle Jitter (High Frequency Mode)									
CLKIN (using DLL outputs) ⁽¹⁾	CLKIN_CYC_JITT_DLL_HF			±150		±150		±150	ps
CLKIN (using CLKFX outputs) ⁽²⁾	CLKIN_CYC_JITT_FX_HF			±150		±150		±150	ps
Input Clock Period Jitter (Low Frequency Mode)									
CLKIN (using DLL outputs) ⁽¹⁾	CLKIN_PER_JITT_DLL_LF			±1		±1		±1	ns
CLKIN (using CLKFX outputs) ⁽²⁾	CLKIN_PER_JITT_FX_LF			±1		±1		±1	ns
Input Clock Period Jitter (High Frequency Mode)									
CLKIN (using DLL outputs) ⁽¹⁾	CLKIN_PER_JITT_DLL_HF			±1		±1		±1	ns
CLKIN (using CLKFX outputs) ⁽²⁾	CLKIN_PER_JITT_FX_HF			±1		±1		±1	ns
Feedback Clock Path Delay Variation									
CLKFB off-chip feedback	CLKFB_DELAY_VAR_EXT			±1		±1		±1	ns

Notes:

- “DLL outputs” is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
- If both DLL and CLKFX outputs are used, follow the more restrictive specification.
- If DCM phase shift feature is used and CLKIN frequency > 200 Mhz, CLKIN duty cycle must be within ±5% (45/55 to 55/45).

Miscellaneous Timing Parameters

Table 42: Miscellaneous Timing Parameters

Description	Symbol	Constraints F _{CLKIN}	Speed Grade			Units
			-6	-5	-4	
Time Required to Achieve LOCK						
Using DLL outputs ⁽¹⁾	LOCK_DLL					
	LOCK_DLL_60	> 60MHz	20.0	20.0	20.0	μs
	LOCK_DLL_50_60	50 - 60 MHz	25.0	25.0	25.0	μs
	LOCK_DLL_40_50	40 - 50 MHz	50.0	50.0	50.0	μs
	LOCK_DLL_30_40	30 - 40 MHz	90.0	90.0	90.0	μs
	LOCK_DLL_24_30	24 - 30 MHz	120.0	120.0	120.0	μs
Using CLKFX outputs	LOCK_FX_MIN		10.0	10.0	10.0	ms
	LOCK_FX_MAX		10.0	10.0	10.0	ms
Additional lock time with fine-phase shifting	LOCK_DLL_FINE_SHIFT		50.0	50.0	50.0	μs
Fine-Phase Shifting						
Absolute shifting range	FINE_SHIFT_RANGE		10.0	10.0	10.0	ns
Delay Lines						
Tap delay resolution	DCM_TAP_MIN		30.0	30.0	30.0	ps
	DCM_TAP_MAX		60.0	60.0	60.0	ps

Notes:

- "DLL outputs" is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
- Specification also applies to PSCLK.

Frequency Synthesis

Table 43: Frequency Synthesis

Attribute	Min	Max
CLKFX_MULTIPLY	2	32
CLKFX_DIVIDE	1	32

Parameter Cross Reference

Table 44: Parameter Cross Reference

Libraries Guide	Data Sheet
DLL_CLKOUT_{MINIMAX}_LF	CLKOUT_FREQ_{1X 2X DV}_LF
DFS_CLKOUT_{MINIMAX}_LF	CLKOUT_FREQ_FX_LF
DLL_CLKIN_{MINIMAX}_LF	CLKIN_FREQ_DLL_LF
DFS_CLKIN_{MINIMAX}_LF	CLKIN_FREQ_FX_LF
DLL_CLKOUT_{MINIMAX}_HF	CLKOUT_FREQ_{1X DV}_HF
DFS_CLKOUT_{MINIMAX}_HF	CLKOUT_FREQ_FX_HF
DLL_CLKIN_{MINIMAX}_HF	CLKIN_FREQ_DLL_HF
DFS_CLKIN_{MINIMAX}_HF	CLKIN_FREQ_FX_HF

Date	Version	Revision
07/30/01	1.6	- Updated values in the Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables. - Added values to the Virtex-II Pin-to-Pin Output Parameter Guidelines and Virtex-II Pin-to-Pin Input Parameter Guidelines tables. - Added Frequency Synthesis table.
10/02/01	1.7	- Updated values in the Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables. - Updated the speed grade designations used in data sheets, and added Table 13, which shows the current speed grade designation for each device.
10/05/01	1.8	Corrected the speed grade designation for the XC2V1000 device in Table 13.
10/12/01	1.9	Updated values in the Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables.
11/28/01	2.0	Updated values in Table 3, Table 4, Table 5, Virtex-II Performance Characteristics, and Virtex-II Switching Characteristics tables.
01/03/02	2.1	- Updated values in Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables, based on values extracted from speedsfile version 1.96. - Changed the speed grade designation for the XC2V6000 device in Table 13.
07/16/02	2.2	- Updated values in Table 4, "Quiescent Supply Current." - Updated values in Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables, based on values extracted from speedsfile version 1.111. - Added Enhanced Multiplier Switching Characteristics section. - Added footnote to Table 37, "Global Clock Setup and Hold for LVTTTL Standard, Without DCM." - Added Source-Synchronous Switching Characteristics section.
09/26/02	2.3	- Removed mention of MIL-M-38510/605 specification. - Added footnotes to Table 2 and Table 6.
12/06/02	2.4	- Revised SSTL2 values in Table 6 to match the latest JEDEC specification. - Added footnote regarding V_{IN} PCI compliance to Table 1. - Added footnote regarding CLKOUT_DUTY_CYCLE_DLL to Table 41.
05/07/03	2.5	- Updated values in Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables, based on values extracted from speedsfile version 1.114. Table 4, Quiescent Supply Current, and Table 5, Minimum Power On Current Required for Virtex-II Devices: Added parameters for XC2V8000 device. Table 16, IOB Output Switching Characteristics: Changed parameter designator T_{IOTON} to T_{IOTP}. Table 26, Enhanced Multiplier Switching Characteristics: Corrected all parameter designators from $T_{MULT_P[nn]}$ to $T_{MULT1_P[nn]}$ in order to correspond with designators used in speedsfile. Table 27, Enhanced Pipelined Multiplier Switching Characteristics: Corrected all parameter designators from $T_{MULTCK_P[nn]}$ to $T_{MULTCK1_P[nn]}$ in order to correspond with designators used in speedsfile. - Removed old Table 19, Standard Capacitive Loads. - Added Figure 1, page 17, showing test configuration for measuring I/O standard adjustments.
06/19/03	2.5.1	Removed footnotes in Table 34 and Table 36 that stated DCM jitter was included in the measurements.

Table 6: FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
3	IO_L96N_3	J16		
3	IO_L96P_3	J15		
3	IO_L94N_3	J14		
3	IO_L94P_3	J13		
3	IO_L93N_3/VREF_3	K16	NC	
3	IO_L93P_3	K15	NC	
3	IO_L91N_3	K14	NC	
3	IO_L91P_3	K13	NC	
3	IO_L45N_3/VREF_3	K12	NC	NC
3	IO_L45P_3	L12	NC	NC
3	IO_L43N_3	L16	NC	NC
3	IO_L43P_3	L15	NC	NC
3	IO_L06N_3	L14	NC	
3	IO_L06P_3	L13	NC	
3	IO_L04N_3	M16	NC	
3	IO_L04P_3	M15	NC	
3	IO_L03N_3/VREF_3	M14		
3	IO_L03P_3	M13		
3	IO_L02N_3/VRP_3	N15		
3	IO_L02P_3/VRN_3	N14		
3	IO_L01N_3	N16		
3	IO_L01P_3	P16		
4	IO_L01N_4/BUSY/DOUT ⁽¹⁾	T14		
4	IO_L01P_4/INIT_B	T13		
4	IO_L02N_4/D0/DIN ⁽¹⁾	P13		
4	IO_L02P_4/D1	R13		
4	IO_L03N_4/D2/ALT_VRP_4	N12		
4	IO_L03P_4/D3/ALT_VRN_4	P12		
4	IO_L04N_4/VREF_4	R12	NC	NC
4	IO_L04P_4	T12	NC	NC
4	IO_L05N_4/VRP_4	N11	NC	NC
4	IO_L05P_4/VRN_4	P11	NC	NC

FG456/FGG456 Fine-Pitch BGA Package

As shown in Table 7, XC2V250, XC2V500, and XC2V1000 Virtex-II devices are available in the FG456/FGG456 fine-pitch BGA package. Pins in the XC2V250, XC2V500, and XC2V1000 devices are the same, except for the pin differences in the XC2V250 and XC2V500 devices shown in the No Connect columns. Following this table are the **FG456/FGG456 Fine-Pitch BGA Package Specifications (1.00mm pitch)**.

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
0	IO_L01N_0	B4		
0	IO_L01P_0	A4		
0	IO_L02N_0	C4		
0	IO_L02P_0	C5		
0	IO_L03N_0/VRP_0	B5		
0	IO_L03P_0/VRN_0	A5		
0	IO_L04N_0/VREF_0	D6		
0	IO_L04P_0	C6		
0	IO_L05N_0	B6		
0	IO_L05P_0	A6		
0	IO_L06N_0	E7		
0	IO_L06P_0	E8		
0	IO_L21N_0	D7	NC	NC
0	IO_L21P_0/VREF_0	C7	NC	NC
0	IO_L22N_0	B7	NC	NC
0	IO_L22P_0	A7	NC	NC
0	IO_L24N_0	D8	NC	NC
0	IO_L24P_0	C8	NC	NC
0	IO_L49N_0	B8	NC	
0	IO_L49P_0	A8	NC	
0	IO_L51N_0	E9	NC	
0	IO_L51P_0/VREF_0	F9	NC	
0	IO_L52N_0	D9	NC	
0	IO_L52P_0	C9	NC	
0	IO_L54N_0	B9	NC	
0	IO_L54P_0	A9	NC	
0	IO_L91N_0/VREF_0	E10		
0	IO_L91P_0	F10		
0	IO_L92N_0	D10		
0	IO_L92P_0	C10		

Table 7: FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
3	IO_L52P_3	P18	NC	
3	IO_L51N_3/VREF_3	P22	NC	
3	IO_L51P_3	P21	NC	
3	IO_L49N_3	P20	NC	
3	IO_L49P_3	P19	NC	
3	IO_L48N_3	R22		
3	IO_L48P_3	R21		
3	IO_L46N_3	R20		
3	IO_L46P_3	R19		
3	IO_L45N_3/VREF_3	R18		
3	IO_L45P_3	P17		
3	IO_L43N_3	T22		
3	IO_L43P_3	T21		
3	IO_L24N_3	T20	NC	NC
3	IO_L24P_3	T19	NC	NC
3	IO_L22N_3	U22	NC	NC
3	IO_L22P_3	U21	NC	NC
3	IO_L21N_3/VREF_3	U20	NC	NC
3	IO_L21P_3	U19	NC	NC
3	IO_L19N_3	T18	NC	NC
3	IO_L19P_3	U18	NC	NC
3	IO_L06N_3	V22		
3	IO_L06P_3	V21		
3	IO_L04N_3	V20		
3	IO_L04P_3	V19		
3	IO_L03N_3/VREF_3	W22		
3	IO_L03P_3	W21		
3	IO_L02N_3/VRP_3	Y22		
3	IO_L02P_3/VRN_3	Y21		
3	IO_L01N_3	W20		
3	IO_L01P_3	AA20		
4	IO_L01N_4/BUSY/DOUT ⁽¹⁾	AB19		
4	IO_L01P_4/INIT_B	AA19		

Table 7: FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
7	VCCO_7	H6		
7	VCCO_7	G6		
NA	CCLK	Y19		
NA	PROG_B	A2		
NA	DONE	AB20		
NA	M0	AB2		
NA	M1	W3		
NA	M2	AB3		
NA	HSWAP_EN	B3		
NA	TCK	C19		
NA	TDI	D3		
NA	TDO	D20		
NA	TMS	B20		
NA	PWRDWN_B	AB21		
NA	DXN	D5		
NA	DXP	A3		
NA	VBATT	A21		
NA	RSVD	A20		
NA	VCCAUX	AB11		
NA	VCCAUX	AA22		
NA	VCCAUX	AA1		
NA	VCCAUX	M22		
NA	VCCAUX	L1		
NA	VCCAUX	B22		
NA	VCCAUX	B1		
NA	VCCAUX	A12		
NA	VCCINT	U17		
NA	VCCINT	U6		
NA	VCCINT	T16		
NA	VCCINT	T15		
NA	VCCINT	T8		
NA	VCCINT	T7		

Table 7: FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
NA	VCCINT	R16		
NA	VCCINT	R7		
NA	VCCINT	H16		
NA	VCCINT	H7		
NA	VCCINT	G16		
NA	VCCINT	G15		
NA	VCCINT	G8		
NA	VCCINT	G7		
NA	VCCINT	F17		
NA	VCCINT	F6		
NA	GND	AB22		
NA	GND	AB1		
NA	GND	AA21		
NA	GND	AA2		
NA	GND	Y20		
NA	GND	Y3		
NA	GND	W19		
NA	GND	W4		
NA	GND	P14		
NA	GND	P13		
NA	GND	P12		
NA	GND	P11		
NA	GND	P10		
NA	GND	P9		
NA	GND	N14		
NA	GND	N13		
NA	GND	N12		
NA	GND	N11		
NA	GND	N10		
NA	GND	N9		
NA	GND	M14		
NA	GND	M13		
NA	GND	M12		
NA	GND	M11		

Table 10: BG728 BGA — XC2V3000

Bank	Pin Description	Pin Number
4	IO_L27P_4/VREF_4	AG19
4	IO_L28N_4	AB19
4	IO_L28P_4	AA19
4	IO_L30N_4	AC19
4	IO_L30P_4	AD19
4	IO_L49N_4	AE19
4	IO_L49P_4	AF19
4	IO_L51N_4	AA18
4	IO_L51P_4/VREF_4	Y18
4	IO_L52N_4	AB18
4	IO_L52P_4	AC18
4	IO_L54N_4	AD18
4	IO_L54P_4	AE18
4	IO_L67N_4	AF18
4	IO_L67P_4	AG18
4	IO_L69N_4	AA17
4	IO_L69P_4/VREF_4	Y17
4	IO_L70N_4	AB17
4	IO_L70P_4	AB16
4	IO_L72N_4	AD17
4	IO_L72P_4	AE17
4	IO_L73N_4	AF17
4	IO_L73P_4	AG17
4	IO_L75N_4	Y16
4	IO_L75P_4/VREF_4	W16
4	IO_L76N_4	AC16
4	IO_L76P_4	AD16
4	IO_L78N_4	AF16
4	IO_L78P_4	AG16
4	IO_L91N_4/VREF_4	W15
4	IO_L91P_4	Y15
4	IO_L92N_4	AB15
4	IO_L92P_4	AA15
4	IO_L93N_4	AC15
4	IO_L93P_4	AD15
4	IO_L94N_4/VREF_4	AE15

Table 11: FF896 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
0	IO_L53N_0	G20		
0	IO_L53P_0	G19		
0	IO_L54N_0	D21		
0	IO_L54P_0	D22		
0	IO_L67N_0	E20	NC	
0	IO_L67P_0	E21	NC	
0	IO_L68N_0	H19	NC	
0	IO_L68P_0	H18	NC	
0	IO_L69N_0	D20	NC	
0	IO_L69P_0/VREF_0	D19	NC	
0	IO_L70N_0	A20	NC	
0	IO_L70P_0	A21	NC	
0	IO_L71N_0	F19	NC	
0	IO_L71P_0	F18	NC	
0	IO_L72N_0	C19	NC	
0	IO_L72P_0	C20	NC	
0	IO_L73N_0	B18	NC	NC
0	IO_L73P_0	B19	NC	NC
0	IO_L74N_0	G18	NC	NC
0	IO_L74P_0	H17	NC	NC
0	IO_L75N_0	E18	NC	NC
0	IO_L75P_0/VREF_0	D18	NC	NC
0	IO_L76N_0	A18	NC	NC
0	IO_L76P_0	A19	NC	NC
0	IO_L77N_0	J17	NC	NC
0	IO_L77P_0	J16	NC	NC
0	IO_L78N_0	E16	NC	NC
0	IO_L78P_0	E17	NC	NC
0	IO_L91N_0/VREF_0	B17		
0	IO_L91P_0	B16		
0	IO_L92N_0	F17		
0	IO_L92P_0	F16		
0	IO_L93N_0	D16		
0	IO_L93P_0	D17		
0	IO_L94N_0/VREF_0	A17		
0	IO_L94P_0	A16		
0	IO_L95N_0/GCLK7P	H16		

Table 11: FF896 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
3	IO_L24N_3	AC8		
3	IO_L24P_3	AB8		
3	IO_L23N_3	AE2		
3	IO_L23P_3	AF3		
3	IO_L22N_3	AD3		
3	IO_L22P_3	AE3		
3	IO_L21N_3/VREF_3	AD6		
3	IO_L21P_3	AD7		
3	IO_L20N_3	AF1		
3	IO_L20P_3	AG1		
3	IO_L19N_3	AD4		
3	IO_L19P_3	AE4		
3	IO_L06N_3	AD8		
3	IO_L06P_3	AE7		
3	IO_L05N_3	AG2		
3	IO_L05P_3	AH2		
3	IO_L04N_3	AD5		
3	IO_L04P_3	AE5		
3	IO_L03N_3/VREF_3	AC9		
3	IO_L03P_3	AD9		
3	IO_L02N_3/VRP_3	AH1		
3	IO_L02P_3/VRN_3	AJ1		
3	IO_L01N_3	AF4		
3	IO_L01P_3	AG3		
4	IO_L01N_4/BUSY/DOUT ⁽¹⁾	AK2		
4	IO_L01P_4/INIT_B	AJ3		
4	IO_L02N_4/D0/DIN ⁽¹⁾	AE8		
4	IO_L02P_4/D1	AF9		
4	IO_L03N_4/D2/ALT_VRP_4	AH5		
4	IO_L03P_4/D3/ALT_VRN_4	AH6		
4	IO_L04N_4/VREF_4	AJ4		
4	IO_L04P_4	AK4		
4	IO_L05N_4/VRP_4	AC10		
4	IO_L05P_4/VRN_4	AC11		
4	IO_L06N_4	AH7		
4	IO_L06P_4	AG6		

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
0	IO_L22P_0	A34		
0	IO_L23N_0	K27		
0	IO_L23P_0	K26		
0	IO_L24N_0	F29		
0	IO_L24P_0	F30		
0	IO_L25N_0	B32		
0	IO_L25P_0	B33		
0	IO_L26N_0	L26		
0	IO_L26P_0	L25		
0	IO_L27N_0	G28		
0	IO_L27P_0/VREF_0	G29		
0	IO_L28N_0	C30		
0	IO_L28P_0	C31		
0	IO_L29N_0	J27		
0	IO_L29P_0	J26		
0	IO_L30N_0	D30		
0	IO_L30P_0	D31		
0	IO_L31N_0	A31	NC	
0	IO_L31P_0	A32	NC	
0	IO_L32N_0	H27	NC	
0	IO_L32P_0	H26	NC	
0	IO_L33N_0	F27	NC	
0	IO_L33P_0/VREF_0	F28	NC	
0	IO_L34N_0	B30	NC	
0	IO_L34P_0	B31	NC	
0	IO_L35N_0	M24	NC	
0	IO_L35P_0	M23	NC	
0	IO_L36N_0	D28	NC	
0	IO_L36P_0	D29	NC	
0	IO_L49N_0	C28		
0	IO_L49P_0	C29		
0	IO_L50N_0	K25		
0	IO_L50P_0	L24		
0	IO_L51N_0	E27		
0	IO_L51P_0/VREF_0	E28		
0	IO_L52N_0	A29		

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
2	IO_L33P_2/VREF_2	J4	NC	
2	IO_L34N_2	K2	NC	
2	IO_L34P_2	J2	NC	
2	IO_L35N_2	P12	NC	
2	IO_L35P_2	R12	NC	
2	IO_L36N_2	M6	NC	
2	IO_L36P_2	L6	NC	
2	IO_L43N_2	L3		
2	IO_L43P_2	K3		
2	IO_L44N_2	N9		
2	IO_L44P_2	P9		
2	IO_L45N_2	M4		
2	IO_L45P_2/VREF_2	L4		
2	IO_L46N_2	L1		
2	IO_L46P_2	K1		
2	IO_L47N_2	P10		
2	IO_L47P_2	R10		
2	IO_L48N_2	N5		
2	IO_L48P_2	M5		
2	IO_L49N_2	N3		
2	IO_L49P_2	M3		
2	IO_L50N_2	N8		
2	IO_L50P_2	P8		
2	IO_L51N_2	T11		
2	IO_L51P_2/VREF_2	R11		
2	IO_L52N_2	N2		
2	IO_L52P_2	M2		
2	IO_L53N_2	T12		
2	IO_L53P_2	U12		
2	IO_L54N_2	P6		
2	IO_L54P_2	N6		
2	IO_L55N_2	N1		
2	IO_L55P_2	M1		
2	IO_L56N_2	R8		
2	IO_L56P_2	T8		
2	IO_L57N_2	R7		

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
3	IO_L58N_3	AD5		
3	IO_L58P_3	AE5		
3	IO_L57N_3/VREF_3	AE11		
3	IO_L57P_3	AD11		
3	IO_L56N_3	AG1		
3	IO_L56P_3	AH1		
3	IO_L55N_3	AD6		
3	IO_L55P_3	AE6		
3	IO_L54N_3	AF10		
3	IO_L54P_3	AE10		
3	IO_L53N_3	AG2		
3	IO_L53P_3	AH2		
3	IO_L52N_3	AF4		
3	IO_L52P_3	AG4		
3	IO_L51N_3/VREF_3	AG8		
3	IO_L51P_3	AF8		
3	IO_L50N_3	AH3		
3	IO_L50P_3	AJ3		
3	IO_L49N_3	AE7		
3	IO_L49P_3	AF7		
3	IO_L48N_3	AG9		
3	IO_L48P_3	AF9		
3	IO_L47N_3	AF6		
3	IO_L47P_3	AG6		
3	IO_L46N_3	AG5		
3	IO_L46P_3	AH5		
3	IO_L45N_3/VREF_3	AF12		
3	IO_L45P_3	AE12		
3	IO_L44N_3	AJ1		
3	IO_L44P_3	AK1		
3	IO_L43N_3	AH4		
3	IO_L43P_3	AJ4		
3	IO_L36N_3	AG11	NC	
3	IO_L36P_3	AF11	NC	
3	IO_L35N_3	AK2	NC	
3	IO_L35P_3	AL2	NC	

FF1517 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)

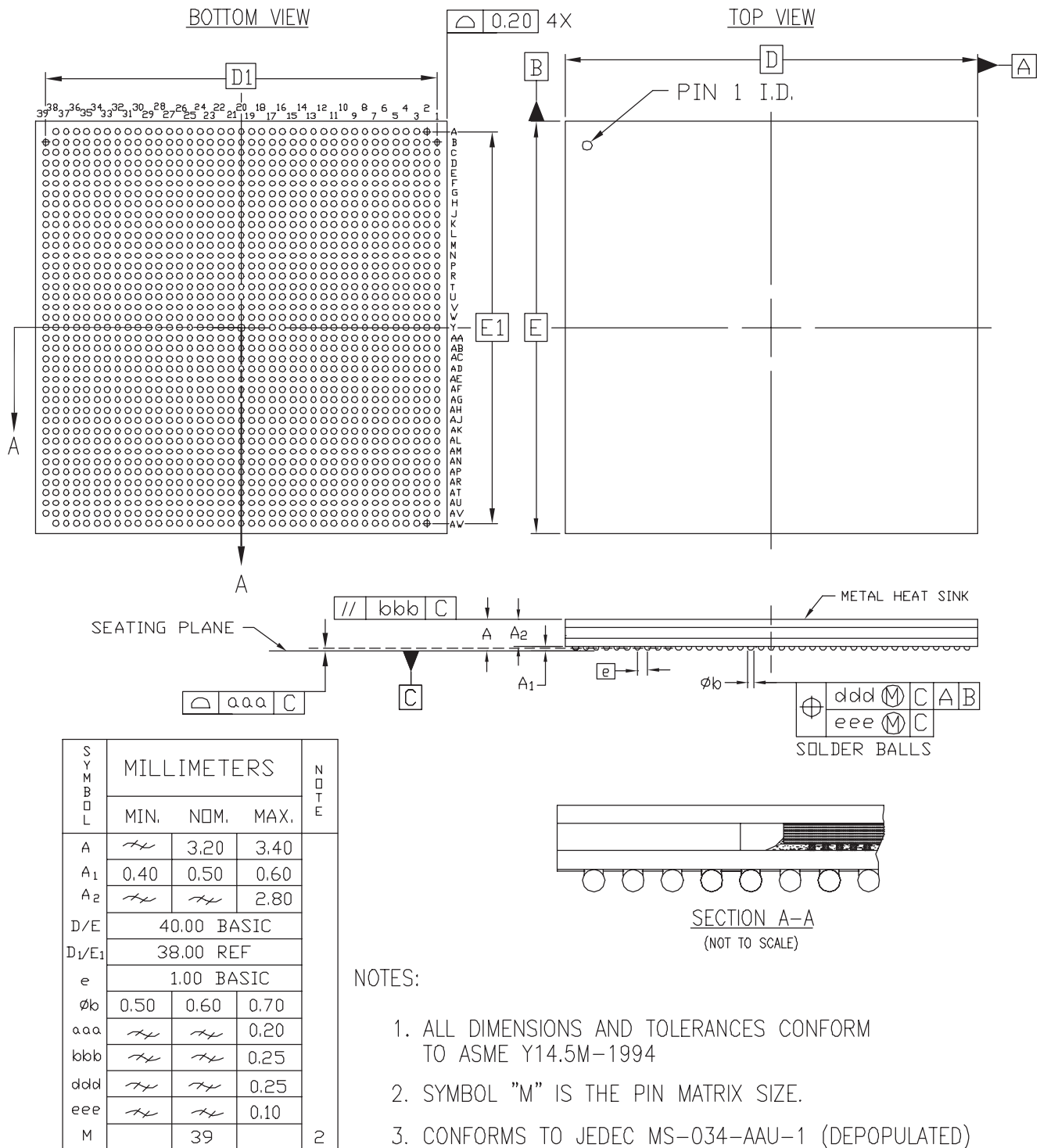


Figure 9: FF1517 Flip-Chip Fine-Pitch BGA Package Specifications

Table 14: BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000

Bank	Pin Description	Pin Number	No Connect in XC2V2000
0	IO_L92N_0	F17	
0	IO_L92P_0	F16	
0	IO_L93N_0	B18	
0	IO_L93P_0	B17	
0	IO_L94N_0/VREF_0	J17	
0	IO_L94P_0	J16	
0	IO_L95N_0/GCLK7P	E17	
0	IO_L95P_0/GCLK6S	E16	
0	IO_L96N_0/GCLK5P	A18	
0	IO_L96P_0/GCLK4S	A17	
1	IO_L96N_1/GCLK3P	C16	
1	IO_L96P_1/GCLK2S	C15	
1	IO_L95N_1/GCLK1P	H16	
1	IO_L95P_1/GCLK0S	H15	
1	IO_L94N_1	A15	
1	IO_L94P_1/VREF_1	A14	
1	IO_L93N_1	F15	
1	IO_L93P_1	F14	
1	IO_L92N_1	G15	
1	IO_L92P_1	G14	
1	IO_L91N_1	B15	
1	IO_L91P_1/VREF_1	B14	
1	IO_L78N_1	D15	
1	IO_L78P_1	E15	
1	IO_L77N_1	J15	
1	IO_L77P_1	K14	
1	IO_L76N_1	D14	
1	IO_L76P_1	D13	
1	IO_L75N_1/VREF_1	E14	
1	IO_L75P_1	E13	
1	IO_L74N_1	A13	
1	IO_L74P_1	A12	
1	IO_L73N_1	F13	
1	IO_L73P_1	F12	
1	IO_L72N_1	J14	
1	IO_L72P_1	J13	
1	IO_L71N_1	B13	

Table 14: BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000

Bank	Pin Description	Pin Number	No Connect in XC2V2000
2	IO_L23N_2	E2	
2	IO_L23P_2	F2	
2	IO_L24N_2	H4	
2	IO_L24P_2	J4	
2	IO_L25N_2	K8	NC
2	IO_L25P_2	L8	NC
2	IO_L27N_2	J7	NC
2	IO_L27P_2/VREF_2	K7	NC
2	IO_L43N_2	F1	
2	IO_L43P_2	G1	
2	IO_L44N_2	L9	
2	IO_L44P_2	M9	
2	IO_L45N_2	G2	
2	IO_L45P_2/VREF_2	J2	
2	IO_L46N_2	H3	
2	IO_L46P_2	J3	
2	IO_L47N_2	J6	
2	IO_L47P_2	L6	
2	IO_L48N_2	J5	
2	IO_L48P_2	K5	
2	IO_L49N_2	H1	
2	IO_L49P_2	J1	
2	IO_L50N_2	N10	
2	IO_L50P_2	P10	
2	IO_L51N_2	L7	
2	IO_L51P_2/VREF_2	M7	
2	IO_L52N_2	K3	
2	IO_L52P_2	L3	
2	IO_L53N_2	M8	
2	IO_L53P_2	N8	
2	IO_L54N_2	L5	
2	IO_L54P_2	M5	
2	IO_L67N_2	K2	
2	IO_L67P_2	L2	
2	IO_L68N_2	M6	
2	IO_L68P_2	N6	
2	IO_L69N_2	L4	
2	IO_L69P_2/VREF_2	M4	

Table 14: BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000

Bank	Pin Description	Pin Number	No Connect in XC2V2000
3	IO_L93P_3	V1	
3	IO_L92N_3	U8	
3	IO_L92P_3	W8	
3	IO_L91N_3	U2	
3	IO_L91P_3	V2	
3	IO_L78N_3	U7	
3	IO_L78P_3	V7	
3	IO_L77N_3	U4	
3	IO_L77P_3	V4	
3	IO_L76N_3	W1	
3	IO_L76P_3	Y1	
3	IO_L75N_3/VREF_3	V5	
3	IO_L75P_3	W5	
3	IO_L74N_3	W2	
3	IO_L74P_3	Y2	
3	IO_L73N_3	W6	
3	IO_L73P_3	Y6	
3	IO_L72N_3	Y5	
3	IO_L72P_3	AA5	
3	IO_L71N_3	W3	
3	IO_L71P_3	Y3	
3	IO_L70N_3	W4	
3	IO_L70P_3	Y4	
3	IO_L69N_3/VREF_3	U9	
3	IO_L69P_3	V9	
3	IO_L68N_3	AA1	
3	IO_L68P_3	AB1	
3	IO_L67N_3	Y7	
3	IO_L67P_3	AA7	
3	IO_L54N_3	AA6	
3	IO_L54P_3	AC6	
3	IO_L53N_3	AA2	
3	IO_L53P_3	AB2	
3	IO_L52N_3	AA4	
3	IO_L52P_3	AC4	
3	IO_L51N_3/VREF_3	V10	
3	IO_L51P_3	W10	
3	IO_L50N_3	AA3	

Table 14: BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000

Bank	Pin Description	Pin Number	No Connect in XC2V2000
3	IO_L50P_3	AB3	
3	IO_L49N_3	AB5	
3	IO_L49P_3	AC5	
3	IO_L48N_3	W9	
3	IO_L48P_3	Y9	
3	IO_L47N_3	AC1	
3	IO_L47P_3	AD1	
3	IO_L46N_3	AC3	
3	IO_L46P_3	AD3	
3	IO_L45N_3/VREF_3	Y8	
3	IO_L45P_3	AA8	
3	IO_L44N_3	AC2	
3	IO_L44P_3	AE2	
3	IO_L43N_3	AB7	
3	IO_L43P_3	AC7	
3	IO_L27N_3/VREF_3	Y10	NC
3	IO_L27P_3	AA10	NC
3	IO_L25N_3	AE1	NC
3	IO_L25P_3	AF1	NC
3	IO_L24N_3	AF2	
3	IO_L24P_3	AG2	
3	IO_L23N_3	AA9	
3	IO_L23P_3	AB9	
3	IO_L22N_3	AD4	
3	IO_L22P_3	AE4	
3	IO_L21N_3/VREF_3	AD5	
3	IO_L21P_3	AE5	
3	IO_L20N_3	AB8	
3	IO_L20P_3	AC8	
3	IO_L19N_3	AG1	
3	IO_L19P_3	AH1	
3	IO_L06N_3	AF4	
3	IO_L06P_3	AG4	
3	IO_L05N_3	AB10	
3	IO_L05P_3	AB11	
3	IO_L04N_3	AF3	
3	IO_L04P_3	AG3	
3	IO_L03N_3/VREF_3	AD6	