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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	5760
Number of Logic Elements/Cells	-
Total RAM Bits	2211840
Number of I/O	912
Number of Gates	4000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FCBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v4000-5ffg1517i

Multiplexers

Virtex-II function generators and associated multiplexers can implement the following:

- 4:1 multiplexer in one slice
- 8:1 multiplexer in two slices
- 16:1 multiplexer in one CLB element (4 slices)
- 32:1 multiplexer in two CLB elements (8 slices)

Each Virtex-II slice has one MUXF5 multiplexer and one MUXFX multiplexer. The MUXFX multiplexer implements the MUXF6, MUXF7, or MUXF8, as shown in Figure 23. Each CLB element has two MUXF6 multiplexers, one MUXF7 multiplexer and one MUXF8 multiplexer. Examples of multiplexers are shown in the *Virtex-II Platform FPGA User Guide*. Any LUT can implement a 2:1 multiplexer.

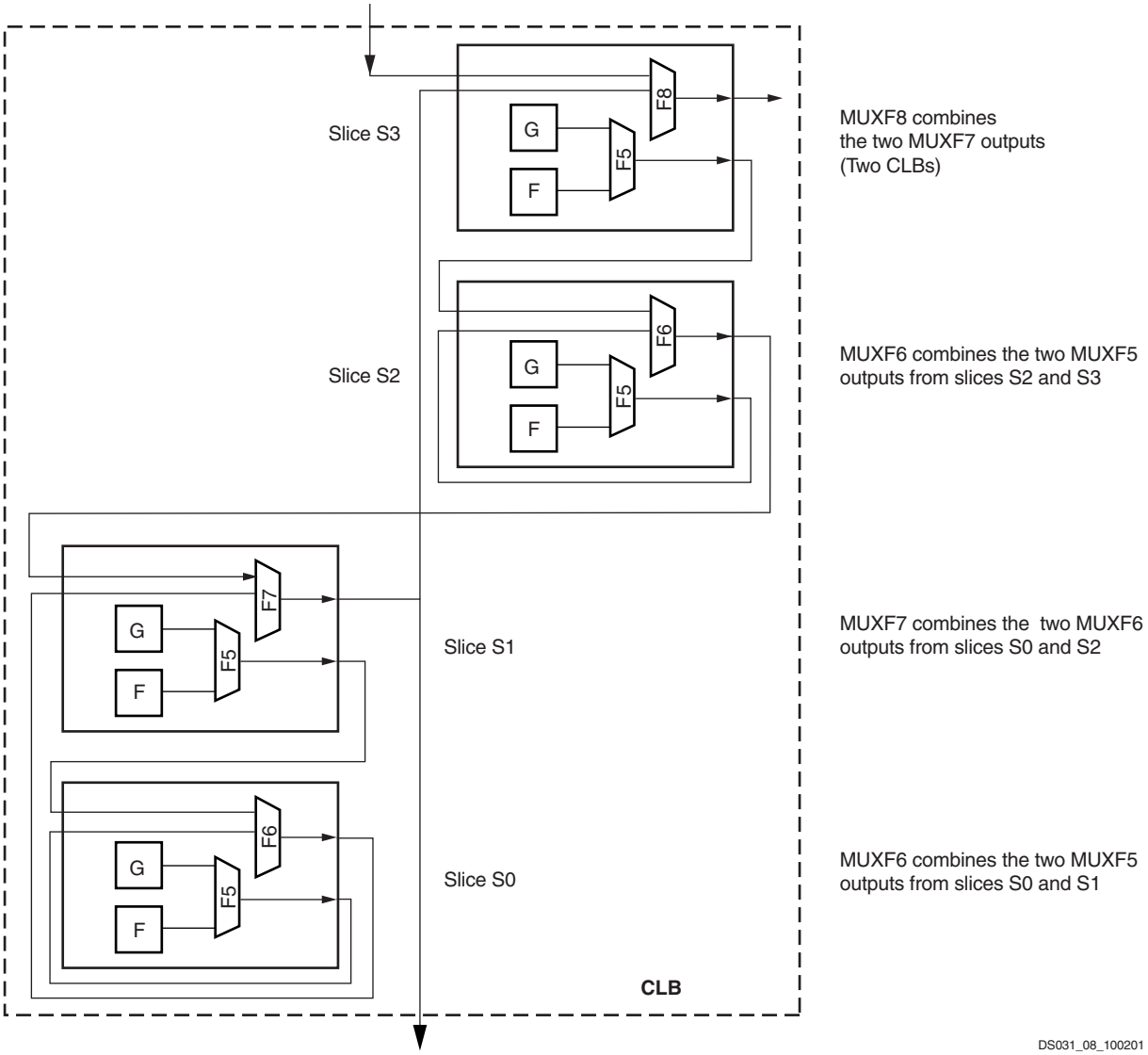

Figure 23: **MUXF5 and MUXFX multiplexers**

Fast Lookahead Carry Logic

Dedicated carry logic provides fast arithmetic addition and subtraction. The Virtex-II CLB has two separate carry chains, as shown in the Figure 24.

The height of the carry chains is two bits per slice. The carry chain in the Virtex-II device is running upward. The dedicated carry path and carry multiplexer (MUXCY) can also be used to cascade function generators for implementing wide logic functions.

Arithmetic Logic

The arithmetic logic includes an XOR gate that allows a 2-bit full adder to be implemented within a slice. In addition, a dedicated AND (MULT_AND) gate (shown in Figure 16) improves the efficiency of multiplier implementation.

Table 14: **IOB Input Switching Characteristics *(Continued)***

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
Propagation Delays						
Pad to output IQ via transparent latch, no delay	T_{IOPLI}	All	0.83	0.91	1.05	ns, Max
Pad to output IQ via transparent latch, with delay	T_{IOPLID}	XC2V40	3.23	3.55	4.09	ns, Max
		XC2V80	3.23	3.55	4.09	ns, Max
		XC2V250	3.23	3.55	4.09	ns, Max
		XC2V500	3.23	3.55	4.09	ns, Max
		XC2V1000	3.23	3.55	4.09	ns, Max
		XC2V1500	3.23	3.55	4.09	ns, Max
		XC2V2000	3.23	3.55	4.09	ns, Max
		XC2V3000	3.32	3.65	4.20	ns, Max
		XC2V4000	3.32	3.65	4.20	ns, Max
		XC2V6000	3.60	3.95	4.55	ns, Max
		XC2V8000		3.95	4.55	ns, Max
Clock CLK to output IQ	T_{IOCKIQ}	All		0.67	0.77	ns, Max
Setup and Hold Times With Respect to Clock at IOB Input Register						
Pad, no delay	T_{IOPICK}/T_{IOICKP}	All	0.84/–0.36	0.92/–0.39	1.06/–0.45	ns, Min
Pad, with delay	$T_{IOPICKD}/T_{IOICKPD}$	XC2V40	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V80	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V250	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V500	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V1000	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V1500	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V2000	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V3000	3.33/–2.10	3.67/–2.31	4.22/–2.66	ns, Min
		XC2V4000	3.33/–2.10	3.67/–2.31	4.22/–2.66	ns, Min
		XC2V6000	3.61/–2.29	3.97/–2.52	4.56/–2.90	ns, Min
		XC2V8000		3.97/–2.52	4.56/–2.90	ns, Min
ICE input	$T_{IOICECK}/T_{IOCKICE}$	All		0.21/ 0.04	0.24/ 0.04	ns, Min
SR input (IFF, synchronous)	$T_{IOSRCKI}$	All	0.27	0.30	0.34	ns, Min
Set/Reset Delays						
SR input to IQ (asynchronous)	T_{IOSRIQ}	All	1.11	1.22	1.40	ns, Max
GSR to output IQ	T_{GSRQ}	All	5.44	5.98	6.88	ns, Max

Notes:
1. Input timing for LVTTL is measured at 1.4 V. For other I/O standards, see Table 18.

CLB Distributed RAM Switching Characteristics

Table 22: **CLB Distributed RAM Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Sequential Delays					
Clock CLK to X/Y outputs (WE active) in 16 x 1 mode	$T_{SHCKO16}$	1.63	1.79	2.05	ns, Max
Clock CLK to X/Y outputs (WE active) in 32 x 1 mode	$T_{SHCKO32}$	1.97	2.17	2.49	ns, Max
Clock CLK to F5 output	$T_{SHCKOF5}$	1.77	1.94	2.23	ns, Max
Setup and Hold Times Before/After Clock CLK					
BX/BY data inputs (DIN)	T_{DS}/T_{DH}	0.53/–0.09	0.58/–0.10	0.67/–0.11	ns, Min
F/G address inputs	T_{AS}/T_{AH}	0.40/ 0.00	0.44/ 0.00	0.50/ 0.00	ns, Min
SR input (WS)	T_{WES}/T_{WEH}	0.42/–0.01	0.46/–0.01	0.53/–0.01	ns, Min
Clock CLK					
Minimum Pulse Width, High	T_{WPH}	0.57	0.63	0.72	ns, Min
Minimum Pulse Width, Low	T_{WPL}	0.57	0.63	0.72	ns, Min
Minimum clock period to meet address write cycle time	T_{WC}	1.14	1.25	1.44	ns, Min

CLB Shift Register Switching Characteristics

Table 23: **CLB Shift Register Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Sequential Delays					
Clock CLK to X/Y outputs	T_{REG}	2.31	2.54	2.92	ns, Max
Clock CLK to X/Y outputs	T_{REG32}	2.65	2.92	3.35	ns, Max
Clock CLK to XB output via MC15 LUT output	T_{REGXB}	2.23	2.46	2.82	ns, Max
Clock CLK to YB output via MC15 LUT output	T_{REGYB}	2.18	2.40	2.75	ns, Max
Clock CLK to Shiftout	T_{CKSH}	1.92	2.11	2.43	ns, Max
Clock CLK to F5 output	T_{REGF5}	2.45	2.69	3.09	ns, Max
Setup and Hold Times Before/After Clock CLK					
BX/BY data inputs (DIN)	T_{SRLDS}/T_{SRLDH}	0.53/–0.07	0.58/–0.08	0.67/–0.09	ns, Min
SR input (WS)	T_{WSS}/T_{WSH}	0.19/–0.06	0.21/–0.07	0.24/–0.08	ns, Min
Clock CLK					
Minimum Pulse Width, High	T_{SRPH}	0.57	0.63	0.72	ns, Min
Minimum Pulse Width, Low	T_{SRPL}	0.57	0.63	0.72	ns, Min

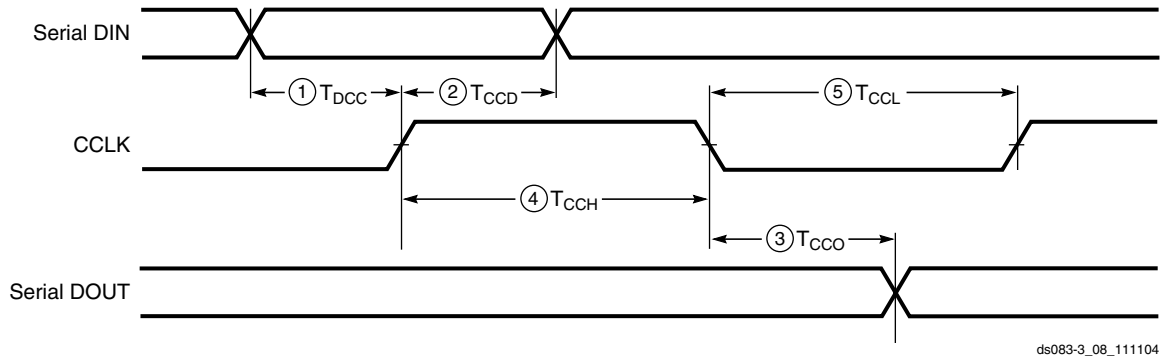

Figure 3: **Slave Serial Mode Timing Sequence**

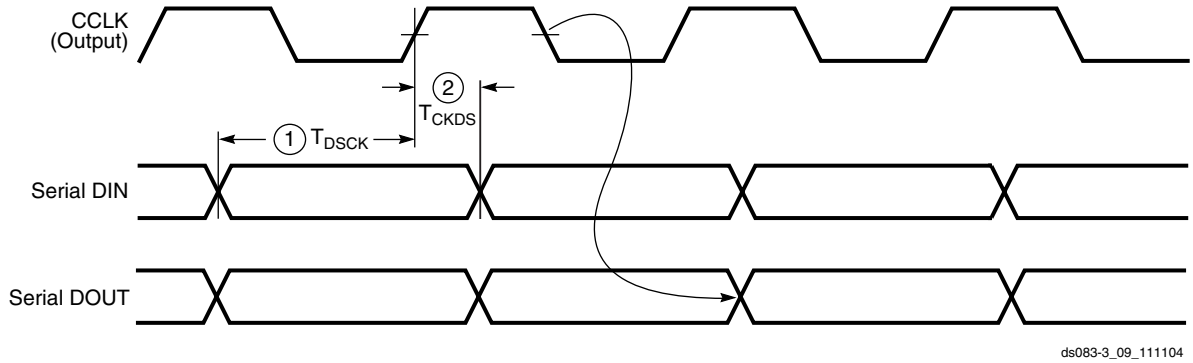

Figure 4: **Master Serial Mode Timing Sequence**

Table 31: **Master/Slave Serial Mode Timing Characteristics**

	Description	Figure References	Symbol	Value	Units
CCLK	DIN setup/hold, slave mode (Figure 3)	1/2	T_{DCC}/T_{CCD}	5.0/0.0	ns, min
	DIN setup/hold, master mode (Figure 4)	1/2	T_{DSCK}/T_{CKDS}	5.0/0.0	ns, min
	DOUT	3	T_{CCO}	12.0	ns, max
	High time	4	T_{CCH}	5.0	ns, min
	Low time	5	T_{CCL}	5.0	ns, min
	Maximum start-up frequency		$F_{CC\_STARTUP}$	50	MHz, max
	Maximum frequency		F_{CC_SERIAL}	66(1)	MHz, max
	Frequency tolerance, master mode with respect to nominal			+45% –30%	

Notes:
1. If no provision is made in the design to adjust the frequency of CCLK, F_{CC_SERIAL} should not exceed $F_{CC\_STARTUP}$.

Master/Slave SelectMAP Parameters

Figure 5 is a generic timing diagram for data loading using SelectMAP. For other data loading diagrams, refer to the ***Virtex-II Pro Platform FPGA User Guide***.

Input Clock Tolerances

Table 39: **Input Clock Tolerances**

Description	Symbol	Constraints F_{CLKIN}	Speed Grade						Units
			-6		-5		-4		
			Min	Max	Min	Max	Min	Max	
Input Clock Low/High Pulse Width									
PSCLK	PSCLK_PULSE	< 1MHz	25.00		25.00		25.00		ns
PSCLK and CLKIN(3)	PSCLK_PULSE and CLKIN_PULSE	1 – 10 MHz	25.00		25.00		25.00		ns
		10 – 25 MHz	10.00		10.00		10.00		ns
		25 – 50 MHz	5.00		5.00		5.00		ns
		50 – 100 MHz	3.00		3.00		3.00		ns
		100 – 150 MHz	2.40		2.40		2.40		ns
		150 – 200 MHz	2.00		2.00		2.00		ns
		200 – 250 MHz	1.80		1.80		1.80		ns
		250 – 300 MHz	1.50		1.50		1.50		ns
		300 – 350 MHz	1.30		1.30		1.30		ns
		350 – 400 MHz	1.15		1.15		1.15		ns
		> 400 MHz	1.05		1.05		1.05		ns
Input Clock Cycle-Cycle Jitter (Low Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_CYC_JITT_DLL_LF			±300		±300		±300	ps
CLKIN (using CLKFX outputs)(2)	CLKIN_CYC_JITT_FX_LF			±300		±300		±300	ps
Input Clock Cycle-Cycle Jitter (High Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_CYC_JITT_DLL_HF			±150		±150		±150	ps
CLKIN (using CLKFX outputs)(2)	CLKIN_CYC_JITT_FX_HF			±150		±150		±150	ps
Input Clock Period Jitter (Low Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_PER_JITT_DLL_LF			±1		±1		±1	ns
CLKIN (using CLKFX outputs)(2)	CLKIN_PER_JITT_FX_LF			±1		±1		±1	ns
Input Clock Period Jitter (High Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_PER_JITT_DLL_HF			±1		±1		±1	ns
CLKIN (using CLKFX outputs)(2)	CLKIN_PER_JITT_FX_HF			±1		±1		±1	ns
Feedback Clock Path Delay Variation									
CLKFB off-chip feedback	CLKFB_DELAY_VAR_EXT			±1		±1		±1	ns

Notes:
1. "DLL outputs" is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. If both DLL and CLKFX outputs are used, follow the more restrictive specification.
3. If DCM phase shift feature is used and CLKIN frequency > 200 Mhz, CLKIN duty cycle must be within ±5% (45/55 to 55/45).

Miscellaneous Timing Parameters

Table 42: **Miscellaneous Timing Parameters**

Description	Symbol	Constraints F_{CLKIN}	Speed Grade			Units
			-6	-5	-4	
Time Required to Achieve LOCK						
Using DLL outputs(1)	LOCK_DLL					
	LOCK_DLL_60	> 60MHz	20.0	20.0	20.0	µs
	LOCK_DLL_50_60	50 - 60 MHz	25.0	25.0	25.0	µs
	LOCK_DLL_40_50	40 - 50 MHz	50.0	50.0	50.0	µs
	LOCK_DLL_30_40	30 - 40 MHz	90.0	90.0	90.0	µs
	LOCK_DLL_24_30	24 - 30 MHz	120.0	120.0	120.0	µs
Using CLKFX outputs	LOCK_FX_MIN		10.0	10.0	10.0	ms
	LOCK_FX_MAX		10.0	10.0	10.0	ms
Additional lock time with fine-phase shifting	LOCK_DLL_FINE_SHIFT		50.0	50.0	50.0	µs
Fine-Phase Shifting						
Absolute shifting range	FINE_SHIFT_RANGE		10.0	10.0	10.0	ns
Delay Lines						
Tap delay resolution	DCM_TAP_MIN		30.0	30.0	30.0	ps
	DCM_TAP_MAX		60.0	60.0	60.0	ps

Notes:
1. "DLL outputs" is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. Specification also applies to PSCLK.

Frequency Synthesis

Table 43: **Frequency Synthesis**

Attribute	Min	Max
CLKFX_MULTIPLY	2	32
CLKFX_DIVIDE	1	32

Parameter Cross Reference

Table 44: **Parameter Cross Reference**

Libraries Guide	Data Sheet
DLL_CLKOUT_{MIN|MAX}_LF	CLKOUT_FREQ_{1X|2X|DV}_LF
DFS_CLKOUT_{MIN|MAX}_LF	CLKOUT_FREQ_FX_LF
DLL_CLKIN_{MIN|MAX}_LF	CLKIN_FREQ_DLL_LF
DFS_CLKIN_{MIN|MAX}_LF	CLKIN_FREQ_FX_LF
DLL_CLKOUT_{MIN|MAX}_HF	CLKOUT_FREQ_{1X|DV}_HF
DFS_CLKOUT_{MIN|MAX}_HF	CLKOUT_FREQ_FX_HF
DLL_CLKIN_{MIN|MAX}_HF	CLKIN_FREQ_DLL_HF
DFS_CLKIN_{MIN|MAX}_HF	CLKIN_FREQ_FX_HF

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
4	IO_L95N_4/GCLK3S	W12		
4	IO_L95P_4/GCLK2P	Y12		
4	IO_L96N_4/GCLK1S	AA12		
4	IO_L96P_4/GCLK0P	AB12		
5	IO_L96N_5/GCLK7S	AA11		
5	IO_L96P_5/GCLK6P	Y11		
5	IO_L95N_5/GCLK5S	W11		
5	IO_L95P_5/GCLK4P	V11		
5	IO_L94N_5	U11		
5	IO_L94P_5/VREF_5	U10		
5	IO_L93N_5	AB10		
5	IO_L93P_5	AA10		
5	IO_L92N_5	Y10		
5	IO_L92P_5	W10		
5	IO_L91N_5	V10		
5	IO_L91P_5/VREF_5	V9		
5	IO_L54N_5	AB9	NC	
5	IO_L54P_5	AA9	NC	
5	IO_L52N_5	Y9	NC	
5	IO_L52P_5	W9	NC	
5	IO_L51N_5/VREF_5	AB8	NC	
5	IO_L51P_5	AA8	NC	
5	IO_L49N_5	Y8	NC	
5	IO_L49P_5	W8	NC	
5	IO_L24N_5	U9	NC	NC
5	IO_L24P_5	V8	NC	NC
5	IO_L22N_5	AB7	NC	NC
5	IO_L22P_5	AA7	NC	NC
5	IO_L21N_5/VREF_5	Y7	NC	NC
5	IO_L21P_5	W7	NC	NC
5	IO_L19N_5	AB6	NC	NC
5	IO_L19P_5	AA6	NC	NC
5	IO_L06N_5	Y6		

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
6	IO_L52N_6	U1		
6	IO_L54P_6	U7		
6	IO_L54N_6	T7		
6	IO_L67P_6	U4		
6	IO_L67N_6	U3		
6	IO_L69P_6	U6		
6	IO_L69N_6/VREF_6	U5		
6	IO_L70P_6	T5		
6	IO_L70N_6	T6		
6	IO_L72P_6	T8		
6	IO_L72N_6	R8		
6	IO_L73P_6	T2	NC	
6	IO_L73N_6	T1	NC	
6	IO_L75P_6	T4	NC	
6	IO_L75N_6/VREF_6	T3	NC	
6	IO_L76P_6	R6	NC	
6	IO_L76N_6	R5	NC	
6	IO_L78P_6	R4	NC	
6	IO_L78N_6	R3	NC	
6	IO_L91P_6	R2		
6	IO_L91N_6	R1		
6	IO_L93P_6	R7		
6	IO_L93N_6/VREF_6	P7		
6	IO_L94P_6	P6		
6	IO_L94N_6	P5		
6	IO_L96P_6	P4		
6	IO_L96N_6	P3		
7	IO_L96P_7	P1		
7	IO_L96N_7	N1		
7	IO_L94P_7	N4		
7	IO_L94N_7	N5		
7	IO_L93P_7/VREF_7	N6		
7	IO_L93N_7	N7		
7	IO_L91P_7	P8		
7	IO_L91N_7	N8		
7	IO_L78P_7	M1	NC	

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
3	VCCO_3	V19		
3	VCCO_3	U25		
3	VCCO_3	U19		
3	VCCO_3	T18		
3	VCCO_3	R18		
3	VCCO_3	P18		
4	VCCO_4	AE20		
4	VCCO_4	AE17		
4	VCCO_4	W18		
4	VCCO_4	W17		
4	VCCO_4	V16		
4	VCCO_4	V15		
4	VCCO_4	V14		
5	VCCO_5	AE10		
5	VCCO_5	AE7		
5	VCCO_5	W10		
5	VCCO_5	W9		
5	VCCO_5	V13		
5	VCCO_5	V12		
5	VCCO_5	V11		
6	VCCO_6	Y2		
6	VCCO_6	V8		
6	VCCO_6	U8		
6	VCCO_6	U2		
6	VCCO_6	T9		
6	VCCO_6	R9		
6	VCCO_6	P9		
7	VCCO_7	N9		
7	VCCO_7	M9		
7	VCCO_7	L9		
7	VCCO_7	K8		
7	VCCO_7	K2		
7	VCCO_7	J8		
7	VCCO_7	G2		
NA	CCLK	AB21		
NA	PROG_B	C4		

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
NA	VCCINT	R10		
NA	VCCINT	P15		
NA	VCCINT	P10		
NA	VCCINT	N15		
NA	VCCINT	N10		
NA	VCCINT	M15		
NA	VCCINT	M10		
NA	VCCINT	L15		
NA	VCCINT	L10		
NA	VCCINT	K15		
NA	VCCINT	K14		
NA	VCCINT	K13		
NA	VCCINT	K12		
NA	VCCINT	K11		
NA	VCCINT	K10		
NA	VCCINT	J16		
NA	VCCINT	J9		
NA	VCCINT	H17		
NA	VCCINT	H8		
NA	GND	AD24		
NA	GND	AD23		
NA	GND	AD18		
NA	GND	AD7		
NA	GND	AD2		
NA	GND	AD1		
NA	GND	AC24		
NA	GND	AC23		
NA	GND	AC2		
NA	GND	AC1		
NA	GND	AB22		
NA	GND	AB3		
NA	GND	AA21		
NA	GND	AA15		
NA	GND	AA10		
NA	GND	AA4		
NA	GND	Y20		

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
3	IO_L72N_3	T20
3	IO_L72P_3	T19
3	IO_L70N_3	U27
3	IO_L70P_3	U26
3	IO_L69N_3/VREF_3	U25
3	IO_L69P_3	V25
3	IO_L67N_3	U21
3	IO_L67P_3	U20
3	IO_L54N_3	V27
3	IO_L54P_3	V26
3	IO_L52N_3	V24
3	IO_L52P_3	V23
3	IO_L51N_3/VREF_3	V22
3	IO_L51P_3	W22
3	IO_L49N_3	V21
3	IO_L49P_3	V20
3	IO_L48N_3	W27
3	IO_L48P_3	Y27
3	IO_L46N_3	W26
3	IO_L46P_3	W25
3	IO_L45N_3/VREF_3	W24
3	IO_L45P_3	W23
3	IO_L43N_3	W21
3	IO_L43P_3	W20
3	IO_L28N_3	W19
3	IO_L28P_3	Y19
3	IO_L27N_3/VREF_3	Y25
3	IO_L27P_3	Y24
3	IO_L25N_3	Y23
3	IO_L25P_3	AA23
3	IO_L24N_3	Y22
3	IO_L24P_3	Y21
3	IO_L22N_3	AA27
3	IO_L22P_3	AB27
3	IO_L21N_3/VREF_3	AA26
3	IO_L21P_3	AA25

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
4	IO_L73P_4	AJ12	NC	NC
4	IO_L74N_4	AE13	NC	NC
4	IO_L74P_4	AE14	NC	NC
4	IO_L75N_4	AF13	NC	NC
4	IO_L75P_4/VREF_4	AG13	NC	NC
4	IO_L76N_4	AK13	NC	NC
4	IO_L76P_4	AK12	NC	NC
4	IO_L77N_4	AB14	NC	NC
4	IO_L77P_4	AB15	NC	NC
4	IO_L78N_4	AF15	NC	NC
4	IO_L78P_4	AF14	NC	NC
4	IO_L91N_4/VREF_4	AJ14		
4	IO_L91P_4	AJ15		
4	IO_L92N_4	AC14		
4	IO_L92P_4	AC15		
4	IO_L93N_4	AG15		
4	IO_L93P_4	AG14		
4	IO_L94N_4/VREF_4	AK14		
4	IO_L94P_4	AK15		
4	IO_L95N_4/GCLK3S	AD15		
4	IO_L95P_4/GCLK2P	AE15		
4	IO_L96N_4/GCLK1S	AH14		
4	IO_L96P_4/GCLK0P	AH15		
5	IO_L96N_5/GCLK7S	AH16		
5	IO_L96P_5/GCLK6P	AH17		
5	IO_L95N_5/GCLK5S	AE16		
5	IO_L95P_5/GCLK4P	AD16		
5	IO_L94N_5	AJ16		
5	IO_L94P_5/VREF_5	AJ17		
5	IO_L93N_5	AG17		
5	IO_L93P_5	AG16		
5	IO_L92N_5	AC16		
5	IO_L92P_5	AC17		
5	IO_L91N_5	AK17		
5	IO_L91P_5/VREF_5	AK18		
5	IO_L78N_5	AF17	NC	NC

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
2	IO_L81N_2	R7	NC
2	IO_L81P_2/VREF_2	R6	NC
2	IO_L82N_2	U5	NC
2	IO_L82P_2	T5	NC
2	IO_L83N_2	T10	NC
2	IO_L83P_2	U10	NC
2	IO_L84N_2	U4	NC
2	IO_L84P_2	T4	NC
2	IO_L91N_2	T2	
2	IO_L91P_2	R1	
2	IO_L92N_2	U7	
2	IO_L92P_2	T7	
2	IO_L93N_2	T6	
2	IO_L93P_2/VREF_2	U6	
2	IO_L94N_2	U1	
2	IO_L94P_2	U2	
2	IO_L95N_2	U9	
2	IO_L95P_2	U8	
2	IO_L96N_2	U3	
2	IO_L96P_2	V4	
3	IO_L96N_3	V6	
3	IO_L96P_3	W6	
3	IO_L95N_3	V5	
3	IO_L95P_3	W5	
3	IO_L94N_3	V7	
3	IO_L94P_3	W7	
3	IO_L93N_3/VREF_3	V10	
3	IO_L93P_3	W10	
3	IO_L92N_3	V1	
3	IO_L92P_3	V2	
3	IO_L91N_3	W3	
3	IO_L91P_3	Y3	
3	IO_L84N_3	V9	NC
3	IO_L84P_3	V8	NC
3	IO_L83N_3	W4	NC

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
5	IO_L79P_5	AP21	NC
5	IO_L78N_5	AK22	
5	IO_L78P_5	AK21	
5	IO_L77N_5	AD18	
5	IO_L77P_5	AD19	
5	IO_L76N_5	AN22	
5	IO_L76P_5	AN21	
5	IO_L75N_5/VREF_5	AJ20	
5	IO_L75P_5	AH20	
5	IO_L74N_5	AG19	
5	IO_L74P_5	AG20	
5	IO_L73N_5	AP24	
5	IO_L73P_5	AP23	
5	IO_L72N_5	AL23	
5	IO_L72P_5	AL22	
5	IO_L71N_5	AF20	
5	IO_L71P_5	AF21	
5	IO_L70N_5	AM24	
5	IO_L70P_5	AM23	
5	IO_L69N_5/VREF_5	AJ21	
5	IO_L69P_5	AJ22	
5	IO_L68N_5	AJ24	
5	IO_L68P_5	AJ23	
5	IO_L67N_5	AN24	
5	IO_L67P_5	AN23	
5	IO_L60N_5	AN26	NC
5	IO_L60P_5	AN25	NC
5	IO_L54N_5	AL25	
5	IO_L54P_5	AL24	
5	IO_L53N_5	AE20	
5	IO_L53P_5	AE21	
5	IO_L52N_5	AN27	
5	IO_L52P_5	AP26	
5	IO_L51N_5/VREF_5	AP29	
5	IO_L51P_5	AP28	
5	IO_L50N_5	AG21	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
NA	GND	V19	
NA	GND	V18	
NA	GND	V17	
NA	GND	V16	
NA	GND	V15	
NA	GND	V14	
NA	GND	U21	
NA	GND	U20	
NA	GND	U19	
NA	GND	U18	
NA	GND	U17	
NA	GND	U16	
NA	GND	U15	
NA	GND	U14	
NA	GND	T26	
NA	GND	T21	
NA	GND	T20	
NA	GND	T19	
NA	GND	T18	
NA	GND	T17	
NA	GND	T16	
NA	GND	T15	
NA	GND	T14	
NA	GND	T9	
NA	GND	R33	
NA	GND	R21	
NA	GND	R20	
NA	GND	R19	
NA	GND	R18	
NA	GND	R17	
NA	GND	R16	
NA	GND	R15	
NA	GND	R14	
NA	GND	R2	
NA	GND	P28	
NA	GND	P21	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
1	IO_L93N_1	E19		
1	IO_L93P_1	E20		
1	IO_L92N_1	J19		
1	IO_L92P_1	J18		
1	IO_L91N_1	A18		
1	IO_L91P_1/VREF_1	A19		
1	IO_L84N_1	D18		
1	IO_L84P_1	D19		
1	IO_L83N_1	K19		
1	IO_L83P_1	K18		
1	IO_L82N_1	B18		
1	IO_L82P_1	B19		
1	IO_L81N_1/VREF_1	G18		
1	IO_L81P_1	G19		
1	IO_L80N_1	E18		
1	IO_L80P_1	E17		
1	IO_L79N_1	A16		
1	IO_L79P_1	A17		
1	IO_L78N_1	F17		
1	IO_L78P_1	F18		
1	IO_L77N_1	L19		
1	IO_L77P_1	L18		
1	IO_L76N_1	B16		
1	IO_L76P_1	B17		
1	IO_L75N_1/VREF_1	G16		
1	IO_L75P_1	G17		
1	IO_L74N_1	M19		
1	IO_L74P_1	M18		
1	IO_L73N_1	C16		
1	IO_L73P_1	C17		
1	IO_L72N_1	D15		
1	IO_L72P_1	D16		
1	IO_L71N_1	J17		
1	IO_L71P_1	J16		
1	IO_L70N_1	A14		
1	IO_L70P_1	A15		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
5	IO_L01N_5/RDWR_B	AU36		
5	IO_L01P_5/CS_B	AV36		
6	IO_L01P_6	AJ27		
6	IO_L01N_6	AH27		
6	IO_L02P_6/VRN_6	AT38		
6	IO_L02N_6/VRP_6	AR37		
6	IO_L03P_6	AP36		
6	IO_L03N_6/VREF_6	AR36		
6	IO_L04P_6	AJ28		
6	IO_L04N_6	AH29		
6	IO_L05P_6	AT39		
6	IO_L05N_6	AR39		
6	IO_L06P_6	AN34		
6	IO_L06N_6	AP35		
6	IO_L07P_6	AH28	NC	
6	IO_L07N_6	AG28	NC	
6	IO_L08P_6	AR38	NC	
6	IO_L08N_6	AP38	NC	
6	IO_L09P_6	AM34	NC	
6	IO_L09N_6/VREF_6	AM33	NC	
6	IO_L10P_6	AL32	NC	
6	IO_L10N_6	AK32	NC	
6	IO_L11P_6	AP37	NC	
6	IO_L11N_6	AN37	NC	
6	IO_L12P_6	AM35	NC	
6	IO_L12N_6	AN35	NC	
6	IO_L19P_6	AK31		
6	IO_L19N_6	AJ30		
6	IO_L20P_6	AP39		
6	IO_L20N_6	AN39		
6	IO_L21P_6	AK33		
6	IO_L21N_6/VREF_6	AL33		
6	IO_L22P_6	AJ31		
6	IO_L22N_6	AH31		
6	IO_L23P_6	AN38		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	VCCINT	AE18		
NA	VCCINT	AE17		
NA	VCCINT	AE16		
NA	VCCINT	AE15		
NA	VCCINT	AD25		
NA	VCCINT	AD24		
NA	VCCINT	AD16		
NA	VCCINT	AD15		
NA	VCCINT	AC25		
NA	VCCINT	AC15		
NA	VCCINT	AB25		
NA	VCCINT	AB15		
NA	VCCINT	AA25		
NA	VCCINT	AA15		
NA	VCCINT	Y27		
NA	VCCINT	Y26		
NA	VCCINT	Y25		
NA	VCCINT	Y15		
NA	VCCINT	Y14		
NA	VCCINT	Y13		
NA	VCCINT	W25		
NA	VCCINT	W15		
NA	VCCINT	V25		
NA	VCCINT	V15		
NA	VCCINT	U25		
NA	VCCINT	U15		
NA	VCCINT	T25		
NA	VCCINT	T24		
NA	VCCINT	T16		
NA	VCCINT	T15		
NA	VCCINT	R25		
NA	VCCINT	R24		
NA	VCCINT	R23		
NA	VCCINT	R22		
NA	VCCINT	R21		
NA	VCCINT	R20		

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
7	IO_L53N_7	K30	
7	IO_L52P_7	L28	
7	IO_L52N_7	J28	
7	IO_L51P_7/VREF_7	M24	
7	IO_L51N_7	L24	
7	IO_L50P_7	L29	
7	IO_L50N_7	K29	
7	IO_L49P_7	M25	
7	IO_L49N_7	L25	
7	IO_L48P_7	L26	
7	IO_L48N_7	J26	
7	IO_L47P_7	J31	
7	IO_L47N_7	H31	
7	IO_L46P_7	J29	
7	IO_L46N_7	H29	
7	IO_L45P_7/VREF_7	M22	
7	IO_L45N_7	L22	
7	IO_L44P_7	J30	
7	IO_L44N_7	G30	
7	IO_L43P_7	K27	
7	IO_L43N_7	J27	
7	IO_L27P_7/VREF_7	L23	NC
7	IO_L27N_7	K23	NC
7	IO_L25P_7	G31	NC
7	IO_L25N_7	F31	NC
7	IO_L24P_7	F30	
7	IO_L24N_7	E30	
7	IO_L23P_7	K25	
7	IO_L23N_7	J25	
7	IO_L22P_7	H28	
7	IO_L22N_7	G28	
7	IO_L21P_7/VREF_7	H27	
7	IO_L21N_7	G27	
7	IO_L20P_7	K24	
7	IO_L20N_7	J24	
7	IO_L19P_7	E31	
7	IO_L19N_7	D31	
7	IO_L06P_7	F28	

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
11/07/00	1.0	Early access draft.
11/22/00	1.1	Initial Xilinx release. Made the following corrections: CS144 package - Table 5, page 5: • Added missing pin D10 in Bank 1. • Changed dedicated pins A2 and B2 to RSVD (from DXN and DXP). FG256 package - Table 6, page 10: • Changed dedicated pins A3 and A4 to RSVD (from DXN and DXP). FG896 package - Table 11, page 94: • Corrected pin AG1 in Bank 4 to be AG12. FF1152 package - Table 12, page 120: • Corrected pin Y3 in Bank 6 to be Y32.
12/19/00	1.2	Reverse designations were fixed for pins in every package.
01/25/01	1.3	Data sheet divided into four modules (per current style standard). DXN and DXP pin information added for CS144 package (Table 5) and FG256 package (Table 6).
02/07/01	1.4	DXN and DXP pin information was changed back to RSVD for the CS144 package (Table 5) and the FG256 package (Table 6).
04/02/01	1.5	• ALT_VRN and ALT_VRP pin information was added for each package. • Table 8, page 34 – added No Connect designations for the XC2V1500 device in the FG676 package. • Reverted to traditional double-column format.
11/07/01	1.6	• Updated list of devices supported in the FF1152, FF1517, and BF957 packages.
09/26/02	1.7	• Updated Table 3 to reflect devices supported in the BG728 and BF957 packages. • Added mention of LVPECL to pin definition in Table 4.
10/07/02	1.8	• Corrected Table 10 heading to reflect supported devices in the BG728 package.
12/06/02	1.8.1	• Enhanced the description of the PWRDWN_B pin in Table 4.
05/07/03	1.8.2	• Added clarification to Table 4 and all device pinout tables regarding the dual-use nature of pins D0/DIN and BUSY/DOUT during configuration.
06/19/03	1.8.3	• The final GND pin in each of five pinout tables was inadvertently deleted in v1.8.2. This revision restores the deleted GND pins as follows: - Pin C5, Table 5, page 5 (CS144) - Pin A1, Table 6, page 10 (FG256) - Pin A2, Table 10, page 72 (BG728) - Pin A2, Table 12, page 120 (FF1152) - Pin AL30, Table 14, page 198 (BF957)
08/01/03	2.0	All Virtex-II devices and speed grades now Production. See Table 13, Module 3.
03/29/04	2.0.1	Recompiled for backward compatibility with Acrobat 4 and above.
06/24/04	3.3	Added references to, and new package drawings for, Pb-free wire-bond packages CSG, FGG, and BGG. (Revision number advanced to level of complete data sheet.)
03/01/05	3.4	Table 4: Changed Direction for User I/O pins (IO_LXXY_#) from “Input/Output” to “Input/Output/Bidirectional”. Added requirement to V_{BATT} to connect pin to V_{CCAUX} or GND if battery is not used.
11/05/07	3.5	Updated copyright notice and legal disclaimer.