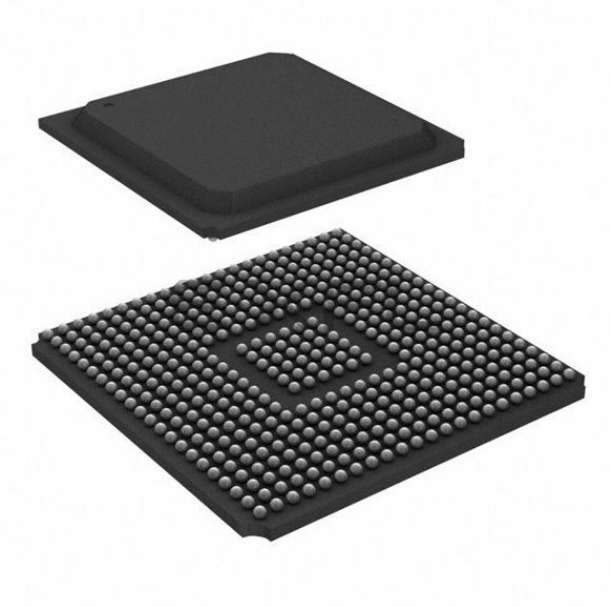
AMD Xilinx - XC2V500-4FG456I Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	768
Number of Logic Elements/Cells	-
Total RAM Bits	589824
Number of I/O	264
Number of Gates	500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v500-4fg456i

Table 6: **Virtex-II Device/Package Combinations and Maximum Number of Available I/Os (Advance Information)**

Package(1,2)	Available I/Os										
	XC2V 40	XC2V 80	XC2V 250	XC2V 500	XC2V 1000	XC2V 1500	XC2V 2000	XC2V 3000	XC2V 4000	XC2V 6000	XC2V 8000
CS144/CSG144	88	92	92	-	-	-	-	-	-	-	-
FG256/FGG256	88	120	172	172	172	-	-	-	-	-	-
FG456/FGG456	-	-	200	264	324	-	-	-	-	-	-
FG676/FGG676	-	-	-	-	-	392	456	484	-	-	-
FF896	-	-	-	-	432	528	624	-	-	-	-
FF1152	-	-	-	-	-	-	-	720	824	824	824
FF1517	-	-	-	-	-	-	-	-	912	1,104	1,108
BG575/BGG575	-	-	-	-	328	392	408	-	-	-	-
BG728/BGG728	-	-	-	-	-	-	-	516	-	-	-
BF957	-	-	-	-	-	-	624	684	684	684	-

Notes:
1. All devices in a particular package are pinout (footprint) compatible. In addition, the FG456/FGG456 and FG676/FGG676 packages are compatible, as are the FF896 and FF1152 packages.
2. Wire-bond packages CS144, FG256, FG456, FG676, BG575, and BG728 are also available in Pb-free versions CSG144, FGG256, FGG456, FGG676, BGG575, and BGG728. See Virtex-II Ordering Examples for details on how to order.

Virtex-II Ordering Examples

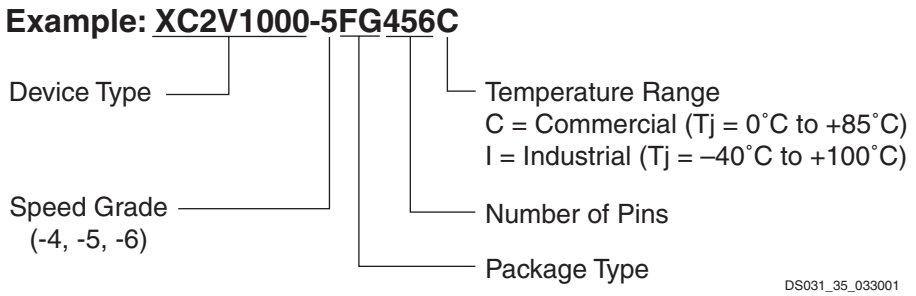


Figure 2: **Virtex-II Ordering Example. Regular Package**

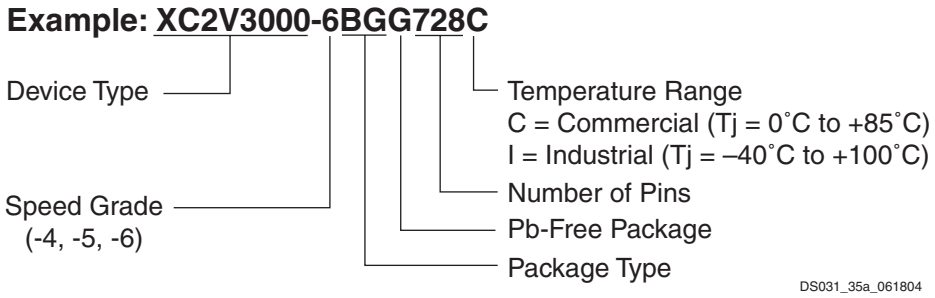


Figure 3: **Virtex-II Ordering Example. Pb-Free Package**

Table 13: **Virtex-II Logic Resources Available in All CLBs**

Device	CLB Array: Row x Column	Number of Slices	Number of LUTs	Max Distributed SelectRAM or Shift Register (bits)	Number of Flip-Flops	Number of Carry-Chains (1)	Number of SOP Chains (1)
XC2V40	8 x 8	256	512	8,192	512	16	16
XC2V80	16 x 8	512	1,024	16,384	1,024	16	32
XC2V250	24 x 16	1,536	3,072	49,152	3,072	32	48
XC2V500	32 x 24	3,072	6,144	98,304	6,144	48	64
XC2V1000	40 x 32	5,120	10,240	163,840	10,240	64	80
XC2V1500	48 x 40	7,680	15,360	245,760	15,360	80	96
XC2V2000	56 x 48	10,752	21,504	344,064	21,504	96	112
XC2V3000	64 x 56	14,336	28,672	458,752	28,672	112	128
XC2V4000	80 x 72	23,040	46,080	737,280	46,080	144	160
XC2V6000	96 x 88	33,792	67,584	1,081,344	67,584	176	192
XC2V8000	112 x 104	46,592	93,184	1,490,944	93,184	208	224

Notes:
1. The carry-chains and SOP chains can be split or cascaded.

18 Kbit Block SelectRAM Resources

Introduction

Virtex-II devices incorporate large amounts of 18 Kbit block SelectRAM. These complement the distributed SelectRAM resources that provide shallow RAM structures implemented in CLBs. Each Virtex-II block SelectRAM is an 18 Kbit true dual-port RAM with two independently clocked and independently controlled synchronous ports that access a common storage area. Both ports are functionally identical. CLK, EN, WE, and SSR polarities are defined through configuration.

Each port has the following types of inputs: Clock and Clock Enable, Write Enable, Set/Reset, and Address, as well as separate Data/parity data inputs (for write) and Data/parity data outputs (for read).

Operation is synchronous; the block SelectRAM behaves like a register. Control, address and data inputs must (and need only) be valid during the set-up time window prior to a rising (or falling, a configuration option) clock edge. Data outputs change as a result of the same clock edge.

Configuration

The Virtex-II block SelectRAM supports various configurations, including single- and dual-port RAM and various data/address aspect ratios. Supported memory configurations for single- and dual-port modes are shown in Table 14.

Table 14: **Dual- and Single-Port Configurations**

16K x 1 bit	2K x 9 bits
8K x 2 bits	1K x 18 bits
4K x 4 bits	512 x 36 bits

Single-Port Configuration

As a single-port RAM, the block SelectRAM has access to the 18 Kbit memory locations in any of the 2K x 9-bit, 1K x 18-bit, or 512 x 36-bit configurations and to 16 Kbit memory locations in any of the 16K x 1-bit, 8K x 2-bit, or 4K x 4-bit configurations. The advantage of the 9-bit, 18-bit and 36-bit widths is the ability to store a parity bit for each eight bits. Parity bits must be generated or checked externally in user logic. In such cases, the width is viewed as 8 + 1, 16 + 2, or 32 + 4. These extra parity bits are stored and behave exactly as the other bits, including the timing parameters. Video applications can use the 9-bit ratio of Virtex-II block SelectRAM memory to advantage.

Each block SelectRAM cell is a fully synchronous memory as illustrated in Figure 29. Input data bus and output data bus widths are identical.

Creating a Design

Creating Virtex-II designs is easy with Xilinx Integrated Synthesis Environment (ISE) development systems, which support advanced design capabilities, including ProActive Timing Closure, integrated logic analysis, and the fastest place and route runtimes in the industry. ISE solutions enable designers to get the performance they need, quickly and easily.

As a result of the ongoing cooperative development efforts between Xilinx and EDA Alliance partners, designers can take advantage of the benefits provided by EDA technologies in the programmable logic design process. Xilinx development systems are available in a number of easy to use configurations, collectively known as the ISE Series.

ISE Alliance

The ISE Alliance solution is designed to plug and play within an existing design environment. Built using industry standard data formats and netlists, these stable, flexible products enable Alliance EDA partners to deliver their best design automation capabilities to Xilinx customers, along with the time to market benefits of ProActive Timing Closure.

ISE Foundation

The ISE Foundation solution delivers the benefits of true HDL-based design in a seamlessly integrated design environment. An intuitive project navigator, as well as powerful HDL design and two HDL synthesis tools, ensure that high-quality results are achieved quickly and easily. The ISE Foundation product includes:

- State Diagram entry using Xilinx StateCAD
- Automatic HDL Testbench generation using Xilinx HDLBencher
- HDL Simulation using ModelSim XE

Design Flow

Virtex-II design flow proceeds as follows:

- Design Entry
- Synthesis
- Implementation
- Verification

Most programmable logic designers iterate through these steps several times in the process of completing a design.

Design Entry

All Xilinx ISE development systems support the mainstream EDA design entry capabilities, ranging from schematic design to advanced HDL design methodologies. Given the high densities of the Virtex-II family, designs are created most efficiently using HDLs. To further improve their time to market, many Xilinx customers employ incremental, modular, and Intellectual Property (IP) design techniques. When properly used, these techniques further accelerate the logic design process.

To enable designers to leverage existing investments in EDA tools, and to ensure high performance design flows, Xilinx jointly develops tools with leading EDA vendors, including:

- Aldec®
- Cadence®
- Exemplar®
- Mentor Graphics®
- Model Technology®
- Synopsys®
- Synplicity®

Complete information on Alliance Series partners and their associated design flows is available at **www.xilinx.com** on the Xilinx Alliance Series web page.

The ISE Foundation product offers schematic entry and HDL design capabilities as part of an integrated design solution - enabling one-stop shopping. These capabilities are powerful, easy to use, and they support the full portfolio of Xilinx programmable logic devices. HDL design capabilities include a color-coded HDL editor with integrated language templates, state diagram entry, and Core generation capabilities.

Synthesis

The ISE Alliance product is engineered to support advanced design flows with the industry's best synthesis tools. Advanced design methodologies include:

- Physical Synthesis
- Incremental synthesis
- RTL floorplanning
- Direct physical mapping

The ISE Foundation product seamlessly integrates synthesis capabilities purchased directly from Exemplar, Synopsys, and Synplicity. In addition, it includes the capabilities of Xilinx Synthesis Technology.

A benefit of having two seamlessly integrated synthesis engines within an ISE design flow is the ability to apply alternative sets of optimization techniques on designs, helping to ensure that designers can meet even the toughest timing requirements.

Design Implementation

The ISE Series development systems include Xilinx timing-driven implementation tools, frequently called “place and route” or “fitting” software. This robust suite of tools enables the creation of an intuitive, flexible, tightly integrated design flow that efficiently bridges “logical” and “physical” design domains. This simplifies the task of defining a design, including its behavior, timing requirements, and optional layout (or floorplanning), as well as simplifying the task of analyzing reports generated during the implementation process.

Configuration

Virtex-II devices are configured by loading application specific configuration data into the internal configuration memory. Configuration is carried out using a subset of the device pins, some of which are dedicated, while others can be re-used as general purpose inputs and outputs once configuration is complete.

Depending on the system design, several configuration modes are supported, selectable via mode pins. The mode pins M2, M1 and M0 are dedicated pins. The M2, M1, and M0 mode pins should be set at a constant DC voltage level, either through pull-up or pull-down resistors, or tied directly to ground or V_{CCAUX}. The mode pins should not be toggled during and after configuration.

An additional pin, HSWAP_EN is used in conjunction with the mode pins to select whether user I/O pins have pull-ups during configuration. By default, HSWAP_EN is tied High (internal pull-up) which shuts off the pull-ups on the user I/O pins during configuration. When HSWAP_EN is tied Low, user I/Os have pull-ups during configuration. Other dedicated pins are CCLK (the configuration clock pin), DONE, PROG_B, and the Boundary-Scan pins: TDI, TDO, TMS, and TCK. Depending on the configuration mode chosen, CCLK can be an output generated by the FPGA, or an input accepting an externally generated clock. The configuration pins and Boundary-Scan pins are independent of the V_{CCO}. The auxiliary power supply (V_{CCAUX}) of 3.3V is used for these pins. All configuration pins are LVTTL 12 mA. (See Virtex-II DC Characteristics in Module 3.)

A persist option is available which can be used to force the configuration pins to retain their configuration function even after device configuration is complete. If the persist option is not selected then the configuration pins with the exception of CCLK, PROG_B, and DONE can be used as user I/O in normal operation. The persist option does not apply to the Boundary-Scan related pins. The persist feature is valuable in applications which employ partial reconfiguration or reconfiguration on the fly.

Configuration Modes

Virtex-II supports the following five configuration modes:

- Slave-Serial Mode
- Master-Serial Mode
- Slave SelectMAP Mode
- Master SelectMAP Mode
- Boundary-Scan (JTAG, IEEE 1532) Mode

A detailed description of configuration modes is provided in the Virtex-II *User Guide*.

Slave-Serial Mode

In slave-serial mode, the FPGA receives configuration data in bit-serial form from a serial PROM or other serial source of configuration data. The CCLK pin on the FPGA is an input in this mode. The serial bitstream must be setup at the DIN input pin a short time before each rising edge of the externally generated CCLK.

Multiple FPGAs can be daisy-chained for configuration from a single source. After a particular FPGA has been configured, the data for the next device is routed internally to the DOUT pin. The data on the DOUT pin changes on the falling edge of CCLK.

Slave-serial mode is selected by applying <111> to the mode pins (M2, M1, M0). A weak pull-up on the mode pins makes slave serial the default mode if the pins are left unconnected.

Master-Serial Mode

In master-serial mode, the CCLK pin is an output pin. It is the Virtex-II FPGA device that drives the configuration clock on the CCLK pin to a Xilinx Serial PROM which in turn feeds bit-serial data to the DIN input. The FPGA accepts this data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the falling CCLK edge.

The interface is identical to slave serial except that an internal oscillator is used to generate the configuration clock (CCLK). A wide range of frequencies can be selected for CCLK which always starts at a slow default frequency. Configuration bits then switch CCLK to a higher frequency for the remainder of the configuration.

Slave SelectMAP Mode

The SelectMAP mode is the fastest configuration option. Byte-wide data is written into the Virtex-II FPGA device with a BUSY flag controlling the flow of data. An external data source provides a byte stream, CCLK, an active Low Chip Select (CS_B) signal and a Write signal (RDWR_B). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low. Data can also be read using the SelectMAP mode. If RDWR_B is asserted, configuration data is read out of the FPGA as part of a readback operation.

After configuration, the pins of the SelectMAP port can be used as additional user I/O. Alternatively, the port can be retained to permit high-speed 8-bit readback using the persist option.

Multiple Virtex-II FPGAs can be configured using the SelectMAP mode, and be made to start-up simultaneously. To configure multiple devices in this way, wire the individual CCLK, Data, RDWR_B, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by deasserting the CS_B pin of each device in turn and writing the appropriate data.

Master SelectMAP Mode

This mode is a master version of the SelectMAP mode. The device is configured byte-wide on a CCLK supplied by the

Date	Version	Revision
07/16/02	2.0	• Updated compatible input standards listed in Table 6.
09/26/02	2.1	• Changed number of resources available to the XC2V40 device in Table 13. • Clarified Power On Reset information under Configuration Sequence.
12/06/02	2.1.1	• Cosmetic edits.
05/07/03	2.1.2	• Added qualification note to Figure 13, page 11. • Corrected sentence in section Input/Output Individual Options, page 4, to read “The optional weak-keeper circuit is connected to each *user I/O pad*.” • Corrected typographical errors in Table 3 for names of HSTL_[x]_DCI_18 standards.
06/19/03	2.2	• Removed Compatible Output Standards and Compatible Input Standards tables. • Added new Table 5, Summary of Voltage Supply Requirements for All Input and Output Standards. This table replaces deleted I/O standards tables. • Added section Rules for Combining I/O Standards in the Same Bank, page 6.
08/01/03	3.0	All Virtex-II devices and speed grades now Production. See Table 13, Module 3.
10/14/03	3.1	• Added section Local Clocking, page 29. • Table 1, page 1: - Added SSTL18_I and SSTL18_II. - Corrected names of 1.8V HSTL_I-IV standards to “HSTL_I-IV_18”. - Corrected Input V_{REF} for HSTL_III-IV_18 from 1.08V to 1.1V. - Changed “N/A” to “N/R” (no requirement). • Table 2, page 2: - Changed “N/A” to “N/R” (no requirement). • Table 3, page 2: - Added SSTL18_I_DCI, SSTL18_II_DCI, LVDS_33_DCI, LVDSEXT_33_DCI, LVDS_25_DCI, and LVDSEXT_25_DCI. - Corrected Input V_{REF} for HSTL_III-IV_18 from 1.08V to 1.1V. • Sections Slave-Serial Mode and Master-Serial Mode, page 36: Changed "rising" to "falling" edge with respect to DOUT. • Added verbiage to section Bitstream Encryption, page 38: “For devices that support this feature, please contact your sales representative for specific ordering part number.”
03/29/04	3.2	• Table 2, page 2, and Table 5, page 7: Removed LVDS_33_DCI and LVDSEXT_33_DCI from tables. • Table 26, page 37: Updated bitstream lengths. • Section BUFGMUX, page 29: Corrected the definition of the "presently selected clock" to be I0 or I1. Corrected signal names in Figure 44 and associated text from CLK0 and CLK1 to I0 and I1. • Recompiled for backward compatibility with Acrobat 4 and above.
06/24/04	3.3	• Table 1, page 1: Added example to Footnote (1) regarding V_{CCO} rules for GTL and GTLP. • Added reference to Pb-free package types in Figure 7, page 6.
03/01/05	3.4	• Reassigned heading hierarchies for better agreement with content. • Table 2: Corrected V_{OD} output voltages. • Table 26: Updated bitstream lengths.
11/05/07	3.5	• Updated copyright statement and legal disclaimer. • Boundary-Scan (JTAG, IEEE 1532) Mode, page 37: Updated IEEE 1149.1 compliance statement.

Table 4: **Quiescent Supply Current**

Symbol	Description	Device	Min	Typical	Max	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC2V40		3	125	mA
		XC2V80		5	125	
		XC2V250		8	150	
		XC2V500		10	200	
		XC2V1000		12	250	
		XC2V1500		15	350	
		XC2V2000		20	400	
		XC2V3000		27	500	
		XC2V4000		35	650	
		XC2V6000		45	800	
		XC2V8000		60	1100	
I_{CCOQ}	Quiescent V_{CCO} supply current(1,2)	XC2V40		1	2	mA
		XC2V80		1	2	
		XC2V250		1	2	
		XC2V500		1	2	
		XC2V1000		1	2	
		XC2V1500		2	4	
		XC2V2000		2	4	
		XC2V3000		2	4	
		XC2V4000		2	4	
		XC2V6000		2	4	
		XC2V8000		2	4	
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current(1,2)	XC2V40		5	25	mA
		XC2V80		5	25	
		XC2V250		5	25	
		XC2V500		5	25	
		XC2V1000		5	25	
		XC2V1500		7.5	50	
		XC2V2000		7.5	50	
		XC2V3000		10	75	
		XC2V4000		10	75	
		XC2V6000		12.5	100	
		XC2V8000		12.5	100	

Notes:
1. With no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
2. If DCI or differential signaling is used, more accurate values can be obtained by using the Power Estimator or XPOWER™.
3. Data are retained even if V_{CCO} drops to 0 V.
4. Values specified for quiescent supply current parameters are Commercial Grade. For Industrial Grade values, multiply Commercial Grade values by 1.25.

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device operation. The actual current consumed depends on the power-on ramp rate of the power supply.

The V_{CCINT}, V_{CCAUX}, and V_{CCO} power supplies shall each ramp on, monotonically, no faster than 200 µs and no slower than 50 ms. Ramp on is defined as: 0 V_{DC} to minimum supply voltages.

Table 5 shows the minimum current required by Virtex-II devices for proper power on and configuration.

Power supplies can be turned on in any sequence.(1)

If any V_{CCO} bank powers up before V_{CCAUX}, then each bank draws up to 300 mA, worst case, until the V_{CCAUX} powers up.(2) This does not harm the device. If the current is limited to the minimum value above, or larger, the device powers on properly after all three supplies have passed through their power-on reset threshold voltages.

Once initialized and configured, use the power calculator to estimate current drain on these supplies.

Notes:
1. If the V_{CCINT} ramp rate is longer than 10 ms, then V_{CCINT} must be applied before V_{CCO} and V_{CCAUX}. The device will not be damaged if this requirement is violated, but configuration will probably fail.
2. The 300 mA is transient current (peak); it eventually disappears even if V_{CCAUX} does not power up.

Table 47: **Sample Window**

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
Sampling Error at Receiver Pins(1)	T_{SAMP}	XC2V40	500	500	550	ps
		XC2V80	500	500	550	ps
		XC2V250	500	500	550	ps
		XC2V500	500	500	550	ps
		XC2V1000	500	500	550	ps
		XC2V1500	500	500	550	ps
		XC2V2000	500	500	550	ps
		XC2V3000	500	500	550	ps
		XC2V4000	500	500	550	ps
		XC2V6000	500	500	550	ps
		XC2V8000		500	550	ps

Notes:
1. This parameter indicates the total sampling error of Virtex-II DDR input registers across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 and CLK180 DCM jitter
   - Worst-case Duty-Cycle Distortion - T_{DCD_CLK180}
   - DCM accuracy (phase offset)
   - DCM phase shift resolution.

   These measurements do not include package or clock tree skew.

Table 48: **Pin-to-Pin Setup/Hold: Source-Synchronous Configuration**

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
Data Input Set-Up and Hold Times Relative to a Forwarded Clock Input Pin, Using DCM and Global Clock Buffer. For situations where clock and data inputs conform to different standards, adjust the setup and hold values accordingly using the values shown in IOB Input Switching Characteristics Standard Adjustments, page 11.						
No Delay Global Clock and IFF with DCM	T_{PSDCM}/ T_{PHDCM}	XC2V40	0.2/0.5	0.2/0.5	0.2/0.5	ns
		XC2V80	0.2/0.5	0.2/0.5	0.2/0.5	ns
		XC2V250	0.2/0.5	0.2/0.5	0.2/0.5	ns
		XC2V500	0.2/0.5	0.2/0.5	0.2/0.5	ns
		XC2V1000	0.2/0.5	0.2/0.5	0.2/0.5	ns
		XC2V1500	0.2/0.5	0.2/0.5	0.2/0.5	ns
		XC2V2000	0.2/0.5	0.2/0.5	0.2/0.5	ns
		XC2V3000	0.2/0.5	0.2/0.5	0.2/0.6	ns
		XC2V4000	0.2/0.5	0.2/0.6	0.2/0.6	ns
		XC2V6000	0.2/0.5	0.2/0.6	0.2/0.6	ns
		XC2V8000		0.2/0.6	0.2/0.7	ns

Notes:
1. IFF = Input Flip-Flop
2. The timing values were measured using the fine-phase adjustment feature of the DCM.
3. The worst-case duty-cycle distortion and DCM jitter on CLK0 and CLK180 is included in these measurements.

CS144/CSG144 Chip-Scale BGA Package

As shown in Table 5, XC2V40, XC2V80, and XC2V250 Virtex-II devices are available in the CS144/CSG144 package. Pins in the XC2V40, XC2V80, and XC2V250 devices are the same except for pin differences in the XC2V40 device, shown in the No Connect column. Following this table are the CS144/CSG144 Chip-Scale BGA Package Specifications (0.80mm pitch).

Table 5: **CS144/CSG144 — XC2V40, XC2V80, and XC2V250**

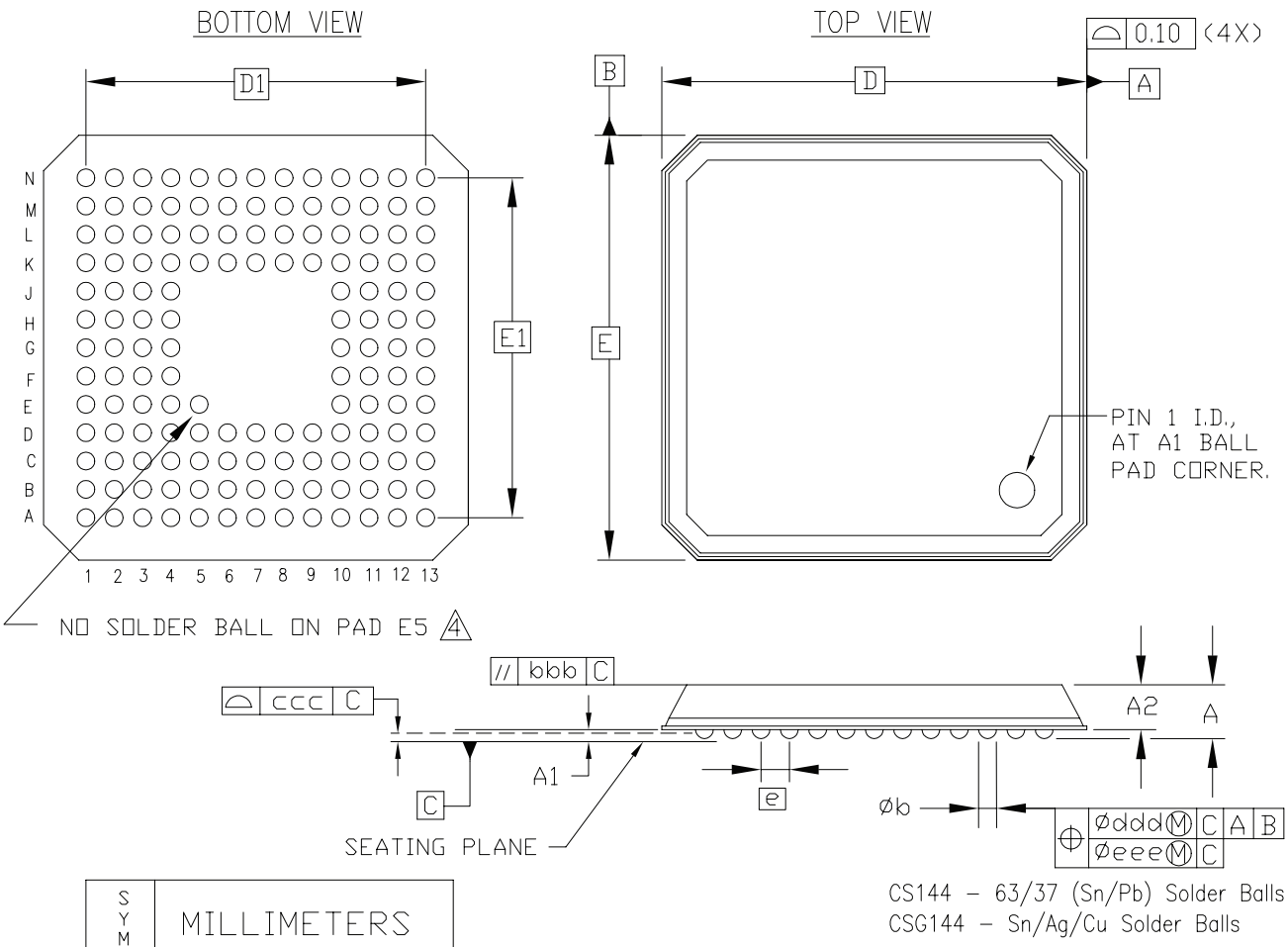
Bank	Pin Description	Pin Number	No Connect in the XC2V40
0	IO_L01N_0	B3	
0	IO_L01P_0	A3	
0	IO_L02N_0	C4	
0	IO_L02P_0	B4	
0	IO_L03N_0/VRP_0	A4	
0	IO_L03P_0/VRN_0	D5	
0	IO_L94N_0/VREF_0	A5	
0	IO_L94P_0	D6	
0	IO_L95N_0/GCLK7P	C6	
0	IO_L95P_0/GCLK6S	B6	
0	IO_L96N_0/GCLK5P	A6	
0	IO_L96P_0/GCLK4S	D7	
1	IO_L96N_1/GCLK3P	A7	
1	IO_L96P_1/GCLK2S	B7	
1	IO_L95N_1/GCLK1P	A8	
1	IO_L95P_1/GCLK0S	B8	
1	IO_L94N_1	C8	
1	IO_L94P_1/VREF_1	D8	
1	IO_L03N_1/VRP_1	C9	
1	IO_L03P_1/VRN_1	D9	
1	IO_L02N_1	A10	
1	IO_L02P_1	B10	
1	IO_L01N_1	C10	
1	IO_L01P_1	D10	
2	IO_L01N_2	C13	
2	IO_L01P_2	D11	
2	IO_L02N_2/VRP_2	D12	
2	IO_L02P_2/VRN_2	D13	
2	IO_L03N_2	E10	
2	IO_L03P_2/VREF_2	E11	
2	IO_L93N_2	E13	NC
2	IO_L93P_2/VREF_2	F11	NC
2	IO_L94N_2	F12	
2	IO_L94P_2	G10	

Table 5: **CS144/CSG144 — XC2V40, XC2V80, and XC2V250**

Bank	Pin Description	Pin Number	No Connect in the XC2V40
NA	CCLK	M13	
NA	PROG_B	B1	
NA	DONE	N12	
NA	M0	N2	
NA	M1	M2	
NA	M2	M3	
NA	TCK	B12	
NA	TDI	C1	
NA	TDO	C11	
NA	TMS	A13	
NA	PWRDWN_B	M12	
NA	HSWAP_EN	A1	
NA	RSVD	A2	
NA	RSVD	B2	
NA	VBATT	A12	
NA	RSVD	B11	
NA	VCCAUX	C2	
NA	VCCAUX	N1	
NA	VCCAUX	N13	
NA	VCCAUX	B13	
NA	VCCINT	H2	
NA	VCCINT	L7	
NA	VCCINT	H13	
NA	VCCINT	C7	
NA	GND	E1	
NA	GND	G2	
NA	GND	J1	
NA	GND	J4	
NA	GND	M5	
NA	GND	L9	
NA	GND	J11	
NA	GND	H10	
NA	GND	F13	
NA	GND	E12	
NA	GND	B9	
NA	GND	C5	

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

CS144/CSG144 Chip-Scale BGA Package Specifications (0.80mm pitch)



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A	–	–	1.20
A_1	0.20	–	–
A_2	0.65	–	–
D/E	12.00 BSC		
D_1/E_1	9.60 BSC		
e	0.80 BSC		
øb	0.40	0.45	0.50
bbb	–	–	0.20
ccc	–	–	0.12
ddd	–	–	0.15
eee	–	–	0.08
M	13		

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MO–216–BAG–2 (DEPOPULATED).
4. PAD 'E5' IS FOR PAD 'A1' CORNER INDICATION.

144–BALL CHIP SCALE BGA (CS144/CSG144)

Figure 1: **CS144/CSG144 Chip-Scale BGA Package Specifications**

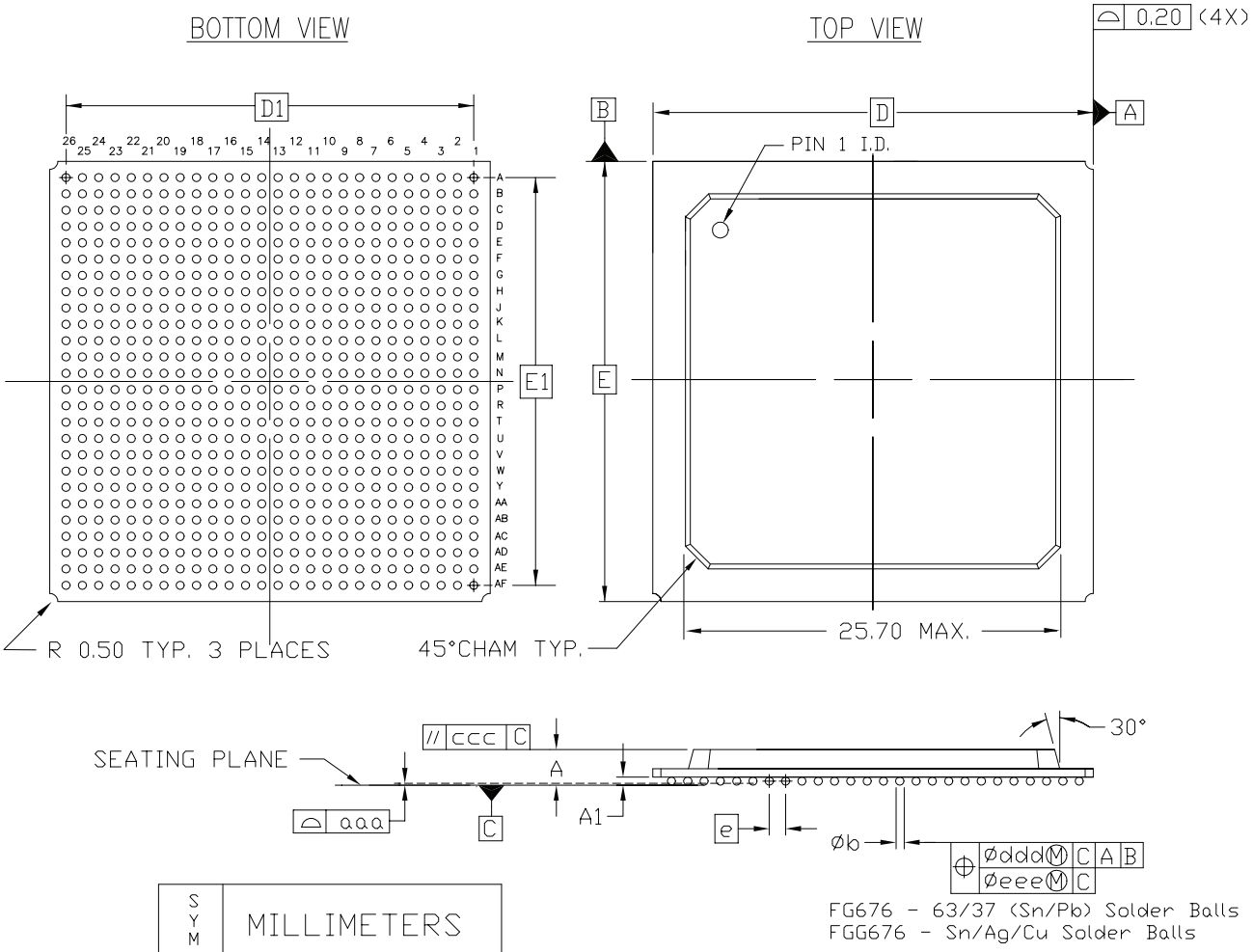
Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
2	IO_L45N_2	H19		
2	IO_L45P_2/VREF_2	H20		
2	IO_L46N_2	H21		
2	IO_L46P_2	H22		
2	IO_L48N_2	J17		
2	IO_L48P_2	J18		
2	IO_L49N_2	J19	NC	
2	IO_L49P_2	J20	NC	
2	IO_L51N_2	J21	NC	
2	IO_L51P_2/VREF_2	J22	NC	
2	IO_L52N_2	K17	NC	
2	IO_L52P_2	K18	NC	
2	IO_L54N_2	K19	NC	
2	IO_L54P_2	K20	NC	
2	IO_L91N_2	K21		
2	IO_L91P_2	K22		
2	IO_L93N_2	L17		
2	IO_L93P_2/VREF_2	L18		
2	IO_L94N_2	L19		
2	IO_L94P_2	L20		
2	IO_L96N_2	L21		
2	IO_L96P_2	L22		
3	IO_L96N_3	M21		
3	IO_L96P_3	M20		
3	IO_L94N_3	M19		
3	IO_L94P_3	M18		
3	IO_L93N_3/VREF_3	M17		
3	IO_L93P_3	N17		
3	IO_L91N_3	N22		
3	IO_L91P_3	N21		
3	IO_L54N_3	N20	NC	
3	IO_L54P_3	N19	NC	
3	IO_L52N_3	N18	NC	

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
6	IO_L52N_6	U1		
6	IO_L54P_6	U7		
6	IO_L54N_6	T7		
6	IO_L67P_6	U4		
6	IO_L67N_6	U3		
6	IO_L69P_6	U6		
6	IO_L69N_6/VREF_6	U5		
6	IO_L70P_6	T5		
6	IO_L70N_6	T6		
6	IO_L72P_6	T8		
6	IO_L72N_6	R8		
6	IO_L73P_6	T2	NC	
6	IO_L73N_6	T1	NC	
6	IO_L75P_6	T4	NC	
6	IO_L75N_6/VREF_6	T3	NC	
6	IO_L76P_6	R6	NC	
6	IO_L76N_6	R5	NC	
6	IO_L78P_6	R4	NC	
6	IO_L78N_6	R3	NC	
6	IO_L91P_6	R2		
6	IO_L91N_6	R1		
6	IO_L93P_6	R7		
6	IO_L93N_6/VREF_6	P7		
6	IO_L94P_6	P6		
6	IO_L94N_6	P5		
6	IO_L96P_6	P4		
6	IO_L96N_6	P3		
7	IO_L96P_7	P1		
7	IO_L96N_7	N1		
7	IO_L94P_7	N4		
7	IO_L94N_7	N5		
7	IO_L93P_7/VREF_7	N6		
7	IO_L93N_7	N7		
7	IO_L91P_7	P8		
7	IO_L91N_7	N8		
7	IO_L78P_7	M1	NC	

FG676/FGG676 Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A	—	2.25	2.60
A_1	0.40	0.50	0.60
D/E	27.00 BSC		
D_1/E_1	25.00 REF		
e	1.00 BSC		
Øb	0.50	0.60	0.70
aaa	—	—	0.20
ccc	—	—	0.35
ddd	—	—	0.30
eee	—	—	0.10
M	26		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-AAL-1

676-BALL FINE PITCH BGA (FG676/FGG676)

Figure 4: **FG676/FGG676 Fine-Pitch BGA Package Specifications**

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
0	IO_L95P_0/GCLK6S	G16		
0	IO_L96N_0/GCLK5P	C17		
0	IO_L96P_0/GCLK4S	C16		
1	IO_L96N_1/GCLK3P	C15		
1	IO_L96P_1/GCLK2S	C14		
1	IO_L95N_1/GCLK1P	F15		
1	IO_L95P_1/GCLK0S	F14		
1	IO_L94N_1	B15		
1	IO_L94P_1/VREF_1	B14		
1	IO_L93N_1	D14		
1	IO_L93P_1	D15		
1	IO_L92N_1	G15		
1	IO_L92P_1	H15		
1	IO_L91N_1	A14		
1	IO_L91P_1/VREF_1	A13		
1	IO_L78N_1	E14	NC	NC
1	IO_L78P_1	E15	NC	NC
1	IO_L77N_1	J15	NC	NC
1	IO_L77P_1	J14	NC	NC
1	IO_L76N_1	B12	NC	NC
1	IO_L76P_1	B13	NC	NC
1	IO_L75N_1/VREF_1	D13	NC	NC
1	IO_L75P_1	E13	NC	NC
1	IO_L74N_1	H14	NC	NC
1	IO_L74P_1	H13	NC	NC
1	IO_L73N_1	A11	NC	NC
1	IO_L73P_1	A12	NC	NC
1	IO_L72N_1	C11	NC	
1	IO_L72P_1	C12	NC	
1	IO_L71N_1	F13	NC	
1	IO_L71P_1	F12	NC	
1	IO_L70N_1	B10	NC	
1	IO_L70P_1	B11	NC	
1	IO_L69N_1/VREF_1	D12	NC	
1	IO_L69P_1	D11	NC	
1	IO_L68N_1	G13	NC	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
5	VCCO_5	AP19	
5	VCCO_5	AL28	
5	VCCO_5	AK20	
5	VCCO_5	AD23	
5	VCCO_5	AD22	
5	VCCO_5	AD21	
5	VCCO_5	AD20	
5	VCCO_5	AC22	
5	VCCO_5	AC21	
5	VCCO_5	AC20	
5	VCCO_5	AC19	
5	VCCO_5	AC18	
6	VCCO_6	AH31	
6	VCCO_6	AE34	
6	VCCO_6	AC24	
6	VCCO_6	AB24	
6	VCCO_6	AB23	
6	VCCO_6	AA24	
6	VCCO_6	AA23	
6	VCCO_6	Y30	
6	VCCO_6	Y24	
6	VCCO_6	Y23	
6	VCCO_6	W34	
6	VCCO_6	W23	
6	VCCO_6	V23	
7	VCCO_7	U23	
7	VCCO_7	T34	
7	VCCO_7	T23	
7	VCCO_7	R30	
7	VCCO_7	R24	
7	VCCO_7	R23	
7	VCCO_7	P24	
7	VCCO_7	P23	
7	VCCO_7	N24	
7	VCCO_7	N23	
7	VCCO_7	M24	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
NA	GND	V19	
NA	GND	V18	
NA	GND	V17	
NA	GND	V16	
NA	GND	V15	
NA	GND	V14	
NA	GND	U21	
NA	GND	U20	
NA	GND	U19	
NA	GND	U18	
NA	GND	U17	
NA	GND	U16	
NA	GND	U15	
NA	GND	U14	
NA	GND	T26	
NA	GND	T21	
NA	GND	T20	
NA	GND	T19	
NA	GND	T18	
NA	GND	T17	
NA	GND	T16	
NA	GND	T15	
NA	GND	T14	
NA	GND	T9	
NA	GND	R33	
NA	GND	R21	
NA	GND	R20	
NA	GND	R19	
NA	GND	R18	
NA	GND	R17	
NA	GND	R16	
NA	GND	R15	
NA	GND	R14	
NA	GND	R2	
NA	GND	P28	
NA	GND	P21	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
5	IO_L79N_5	AV24		
5	IO_L79P_5	AV23		
5	IO_L78N_5	AP23		
5	IO_L78P_5	AP22		
5	IO_L77N_5	AJ21		
5	IO_L77P_5	AJ22		
5	IO_L76N_5	AU24		
5	IO_L76P_5	AU23		
5	IO_L75N_5/VREF_5	AT25		
5	IO_L75P_5	AT24		
5	IO_L74N_5	AH21		
5	IO_L74P_5	AH22		
5	IO_L73N_5	AW26		
5	IO_L73P_5	AW25		
5	IO_L72N_5	AR25		
5	IO_L72P_5	AR24		
5	IO_L71N_5	AN23		
5	IO_L71P_5	AN24		
5	IO_L70N_5	AU25		
5	IO_L70P_5	AV25		
5	IO_L69N_5/VREF_5	AL24		
5	IO_L69P_5	AL23		
5	IO_L68N_5	AK23		
5	IO_L68P_5	AK24		
5	IO_L67N_5	AU27		
5	IO_L67P_5	AU26		
5	IO_L60N_5	AP25		
5	IO_L60P_5	AP24		
5	IO_L59N_5	AM24		
5	IO_L59P_5	AM25		
5	IO_L58N_5	AW28		
5	IO_L58P_5	AW27		
5	IO_L57N_5/VREF_5	AT27		
5	IO_L57P_5	AT26		
5	IO_L56N_5	AH23		
5	IO_L56P_5	AH24		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
5	IO_L55N_5	AV28		
5	IO_L55P_5	AV27		
5	IO_L54N_5	AP27		
5	IO_L54P_5	AP26		
5	IO_L53N_5	AN25		
5	IO_L53P_5	AN26		
5	IO_L52N_5	AU29		
5	IO_L52P_5	AU28		
5	IO_L51N_5/VREF_5	AR28		
5	IO_L51P_5	AR27		
5	IO_L50N_5	AJ24		
5	IO_L50P_5	AJ25		
5	IO_L49N_5	AW30		
5	IO_L49P_5	AW29		
5	IO_L36N_5	AT29	NC	
5	IO_L36P_5	AT28	NC	
5	IO_L35N_5	AK25	NC	
5	IO_L35P_5	AL26	NC	
5	IO_L34N_5	AV31	NC	
5	IO_L34P_5	AV30	NC	
5	IO_L33N_5/VREF_5	AP29	NC	
5	IO_L33P_5	AP28	NC	
5	IO_L32N_5	AK26	NC	
5	IO_L32P_5	AJ26	NC	
5	IO_L31N_5	AW32	NC	
5	IO_L31P_5	AW31	NC	
5	IO_L30N_5	AM27		
5	IO_L30P_5	AM26		
5	IO_L29N_5	AN28		
5	IO_L29P_5	AN29		
5	IO_L28N_5	AU31		
5	IO_L28P_5	AU30		
5	IO_L27N_5/VREF_5	AT31		
5	IO_L27P_5	AT30		
5	IO_L26N_5	AH25		
5	IO_L26P_5	AH26		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
5	IO_L01N_5/RDWR_B	AU36		
5	IO_L01P_5/CS_B	AV36		
6	IO_L01P_6	AJ27		
6	IO_L01N_6	AH27		
6	IO_L02P_6/VRN_6	AT38		
6	IO_L02N_6/VRP_6	AR37		
6	IO_L03P_6	AP36		
6	IO_L03N_6/VREF_6	AR36		
6	IO_L04P_6	AJ28		
6	IO_L04N_6	AH29		
6	IO_L05P_6	AT39		
6	IO_L05N_6	AR39		
6	IO_L06P_6	AN34		
6	IO_L06N_6	AP35		
6	IO_L07P_6	AH28	NC	
6	IO_L07N_6	AG28	NC	
6	IO_L08P_6	AR38	NC	
6	IO_L08N_6	AP38	NC	
6	IO_L09P_6	AM34	NC	
6	IO_L09N_6/VREF_6	AM33	NC	
6	IO_L10P_6	AL32	NC	
6	IO_L10N_6	AK32	NC	
6	IO_L11P_6	AP37	NC	
6	IO_L11N_6	AN37	NC	
6	IO_L12P_6	AM35	NC	
6	IO_L12N_6	AN35	NC	
6	IO_L19P_6	AK31		
6	IO_L19N_6	AJ30		
6	IO_L20P_6	AP39		
6	IO_L20N_6	AN39		
6	IO_L21P_6	AK33		
6	IO_L21N_6/VREF_6	AL33		
6	IO_L22P_6	AJ31		
6	IO_L22N_6	AH31		
6	IO_L23P_6	AN38		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
6	IO_L95N_6	AA38		
6	IO_L96P_6	AA35		
6	IO_L96N_6	AA34		
7	IO_L96P_7	W34		
7	IO_L96N_7	Y34		
7	IO_L95P_7	W32		
7	IO_L95N_7	V32		
7	IO_L94P_7	W37		
7	IO_L94N_7	Y37		
7	IO_L93P_7/VREF_7	W35		
7	IO_L93N_7	Y35		
7	IO_L92P_7	W31		
7	IO_L92N_7	V31		
7	IO_L91P_7	V39		
7	IO_L91N_7	W39		
7	IO_L84P_7	V36		
7	IO_L84N_7	W36		
7	IO_L83P_7	W30		
7	IO_L83N_7	V30		
7	IO_L82P_7	V38		
7	IO_L82N_7	W38		
7	IO_L81P_7/VREF_7	V33		
7	IO_L81N_7	W33		
7	IO_L80P_7	W29		
7	IO_L80N_7	V29		
7	IO_L79P_7	T39		
7	IO_L79N_7	U39		
7	IO_L78P_7	U35		
7	IO_L78N_7	V35		
7	IO_L77P_7	W28		
7	IO_L77N_7	V28		
7	IO_L76P_7	U37		
7	IO_L76N_7	U38		
7	IO_L75P_7/VREF_7	U34		
7	IO_L75N_7	V34		