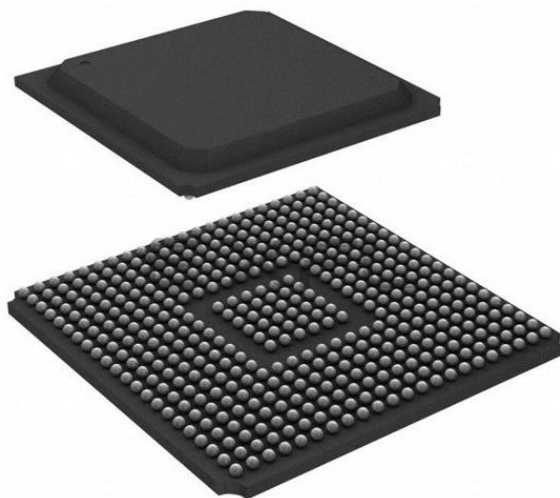




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	768
Number of Logic Elements/Cells	-
Total RAM Bits	589824
Number of I/O	264
Number of Gates	500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v500-4fgg456c

Sum of Products

Each Virtex-II slice has a dedicated OR gate named ORCY, ORing together outputs from the slices carryout and the ORCY from an adjacent slice. The ORCY gate with the dedicated Sum of Products (SOP) chain are designed for implementing

large, flexible SOP chains. One input of each ORCY is connected through the fast SOP chain to the output of the previous ORCY in the same slice row. The second input is connected to the output of the top MUXCY in the same slice, as shown in Figure 25.

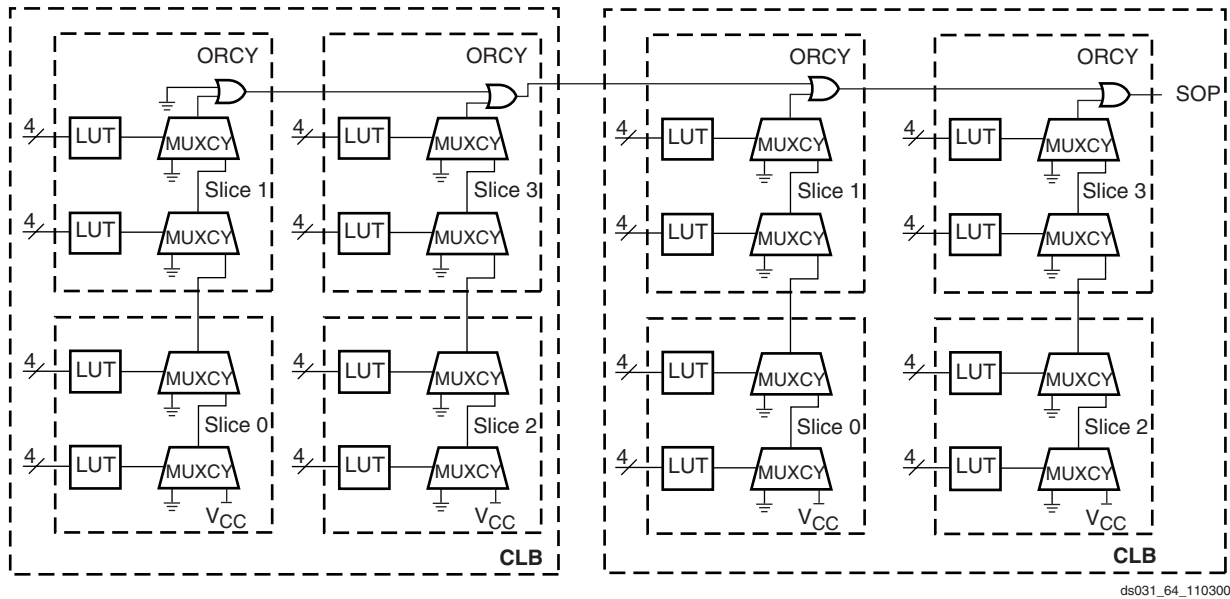


Figure 25: Horizontal Cascade Chain

LUTs and MUXCYs can implement large AND gates or other combinatorial logic functions. Figure 26 illustrates

LUT and MUXCY resources configured as a 16-input AND gate.

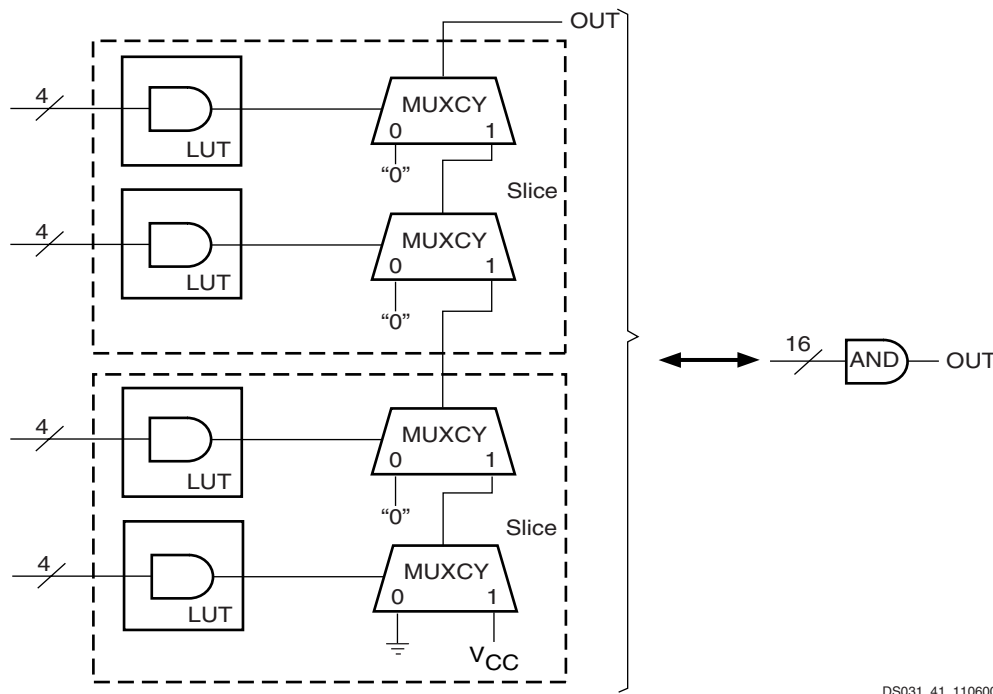


Figure 26: Wide-Input AND Gate (16 Inputs)

Table 5: Minimum Power On Current Required for Virtex-II Devices

	Device (mA)							
	XC2V40, XC2V80, XC2V250, XC2V500	XC2V1000	XC2V1500	XC2V2000	XC2V3000	XC2V4000	XC2V6000	XC2V8000
$I_{CCINTMIN}$	200	250	350	400	500	650	800	1100
$I_{CCAUXMIN}$	100	100	100	100	100	100	100	100
I_{CCOMIN}	50	50	100	100	100	100	100	100

Notes:

- Values specified for power on current parameters are Commercial Grade. For Industrial Grade values, multiply Commercial Grade values by 1.25.
- I_{CCOMIN} values listed here apply to the entire device (all banks).

General Power Supply Requirements

Proper decoupling of all FPGA power supplies is essential. Consult Xilinx Application Note [XAPP623](#) for detailed information on power distribution system design.

V_{CCAUX} powers critical resources in the FPGA. Thus, V_{CCAUX} is especially susceptible to power supply noise.

Changes in V_{CCAUX} voltage outside of 200 mV peak to peak should take place at a rate no faster than 10 mV per millisecond. Techniques to help reduce jitter and period distortion are provided in Xilinx Answer Record 13756, available at [www.support.xilinx.com](#).

V_{CCAUX} can share a power plane with 3.3V V_{CCO} , but only if V_{CCO} does not have excessive noise. Using simultaneously switching output (SSO) limits are essential for keeping power supply noise to a minimum. Refer to [XAPP689](#), "Managing Ground Bounce in Large FPGAs," to determine the number of simultaneously switching outputs allowed per bank at the package level.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 6: DC Input and Output Levels

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTL ⁽¹⁾	-0.5	0.8	2.0	3.6	0.4	2.4	24	-24
LVC MOS33	-0.5	0.8	2.0	3.6	0.4	$V_{CCO} - 0.4$	24	-24
LVC MOS25	-0.5	0.7	1.7	2.7	0.4	$V_{CCO} - 0.4$	24	-24
LVC MOS18	-0.5	35% V_{CCO}	65% V_{CCO}	1.95	0.4	$V_{CCO} - 0.4$	16	-16
LVC MOS15	-0.5	35% V_{CCO}	65% V_{CCO}	1.7	0.4	$V_{CCO} - 0.4$	16	-16
PCI33_3	-0.5	30% V_{CCO}	50% V_{CCO}	$V_{CCO} + 0.5$	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
PCI66_3	-0.5	30% V_{CCO}	50% V_{CCO}	$V_{CCO} + 0.5$	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
PCI-X	-0.5	Note 2	Note 2	Note 2	Note 2	Note 2	Note 2	Note 2
GTLP	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCO} + 0.5$	0.6	n/a	36	n/a
GTL	-0.5	$V_{REF} - 0.05$	$V_{REF} + 0.05$	$V_{CCO} + 0.5$	0.4	n/a	40	n/a
HSTL I	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCO} + 0.5$	0.4	$V_{CCO} - 0.4$	8	-8
HSTL II	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCO} + 0.5$	0.4	$V_{CCO} - 0.4$	16	-16
HSTL III	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCO} + 0.5$	0.4	$V_{CCO} - 0.4$	24	-8
HSTL IV	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCO} + 0.5$	0.4	$V_{CCO} - 0.4$	48	-8

Extended LVDS DC Specifications (LVDSEXT_33 & LVDSEXT_25)

Table 9: Extended LVDS DC Specifications

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}			3.3 or 2.5		V
Output High voltage for Q and $\overline{Q}$	V_{OH}	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals			1.785	V
Output Low voltage for Q and $\overline{Q}$	V_{OL}	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	0.705			V
Differential output voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{ODIFF}	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	440		820	mV
Output common-mode voltage	V_{OCM}	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	1.125	1.200	1.375	V
Differential input voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{IDIFF}	Common-mode input voltage = 1.25 V	100	350	N/A	mV
Input common-mode voltage	V_{ICM}	Differential input voltage = ± 350 mV	0.2	1.25	$V_{CCO} - 0.5$	V

LVPECL DC Specifications

These values are valid when driving a $100\ \Omega$ differential load only, i.e., a $100\ \Omega$ resistor between the two receiver pins. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower

common-mode ranges. Table 10 summarizes the DC output specifications of LVPECL. For more information on using LVPECL, see the *Virtex-II User Guide*.

Table 10: LVPECL DC Specifications

DC Parameter	Min	Max	Min	Max	Min	Max	Units
V_{CCO}	3.0		3.3		3.6		V
V_{OH}	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{OL}	0.96	1.27	1.06	1.43	1.30	1.57	V
V_{IH}	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	0.86	2.125	0.86	2.125	0.86	2.125	V
Differential Input Voltage	0.3	–	0.3	–	0.3	–	V

Virtex-II Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, With DCM

Table 34: Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, With DCM

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
LVTTL Global Clock Input to Output delay using Output flip-flop, 12 mA, Fast Slew Rate, <i>with</i> DCM. For data <i>output</i> with different standards, adjust the delays with the values shown in IOB Output Switching Characteristics Standard Adjustments, page 14.						
Global Clock and OFF with DCM	T _{ICKOFFDCM}	XC2V40	1.10	1.28	1.48	ns
		XC2V80	1.10	1.28	1.48	ns
		XC2V250	1.10	1.28	1.48	ns
		XC2V500	1.10	1.28	1.48	ns
		XC2V1000	1.10	1.28	1.48	ns
		XC2V1500	1.10	1.28	1.48	ns
		XC2V2000	1.10	1.28	1.48	ns
		XC2V3000	1.19	1.38	1.59	ns
		XC2V4000	1.19	1.38	1.59	ns
		XC2V6000	1.64	1.88	2.17	ns
		XC2V8000		1.88	2.17	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with test setup shown in **Figure 1**. For other I/O standards, see **Table 19**.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *Without* DCM

Table 35: Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *Without* DCM

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
LVTTL Global Clock Input to Output Delay using Output flip-flop, 12 mA, Fast Slew Rate, <i>without</i> DCM. For data <i>output</i> with different standards, adjust the delays with the values shown in <i>IOB Output Switching Characteristics Standard Adjustments</i> , page 14.						
Global Clock and OFF without DCM	T _{ICKOF}	XC2V40	3.46	3.58	3.69	ns
		XC2V80	3.62	3.58	3.69	ns
		XC2V250	3.79	3.88	4.47	ns
		XC2V500	3.85	3.88	4.47	ns
		XC2V1000	4.02	4.28	4.62	ns
		XC2V1500	4.16	4.28	4.62	ns
		XC2V2000	4.30	4.43	5.10	ns
		XC2V3000	4.49	4.64	5.34	ns
		XC2V4000	4.82	4.99	5.74	ns
		XC2V6000	5.19	5.38	5.93	ns
		XC2V8000		6.09	7.00	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with test setup shown in [Figure 1](#). For other I/O standards, see [Table 19](#).

Table 6: FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
3	IO_L96N_3	J16		
3	IO_L96P_3	J15		
3	IO_L94N_3	J14		
3	IO_L94P_3	J13		
3	IO_L93N_3/VREF_3	K16	NC	
3	IO_L93P_3	K15	NC	
3	IO_L91N_3	K14	NC	
3	IO_L91P_3	K13	NC	
3	IO_L45N_3/VREF_3	K12	NC	NC
3	IO_L45P_3	L12	NC	NC
3	IO_L43N_3	L16	NC	NC
3	IO_L43P_3	L15	NC	NC
3	IO_L06N_3	L14	NC	
3	IO_L06P_3	L13	NC	
3	IO_L04N_3	M16	NC	
3	IO_L04P_3	M15	NC	
3	IO_L03N_3/VREF_3	M14		
3	IO_L03P_3	M13		
3	IO_L02N_3/VRP_3	N15		
3	IO_L02P_3/VRN_3	N14		
3	IO_L01N_3	N16		
3	IO_L01P_3	P16		
4	IO_L01N_4/BUSY/DOUT ⁽¹⁾	T14		
4	IO_L01P_4/INIT_B	T13		
4	IO_L02N_4/D0/DIN ⁽¹⁾	P13		
4	IO_L02P_4/D1	R13		
4	IO_L03N_4/D2/ALT_VRP_4	N12		
4	IO_L03P_4/D3/ALT_VRN_4	P12		
4	IO_L04N_4/VREF_4	R12	NC	NC
4	IO_L04P_4	T12	NC	NC
4	IO_L05N_4/VRP_4	N11	NC	NC
4	IO_L05P_4/VRN_4	P11	NC	NC

Table 6: FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
5	IO_L01P_5/CS_B	T3		
6	IO_L01P_6	P1		
6	IO_L01N_6	N1		
6	IO_L02P_6/VRN_6	N3		
6	IO_L02N_6/VRP_6	N2		
6	IO_L03P_6	M4		
6	IO_L03N_6/VREF_6	M3		
6	IO_L04P_6	M2	NC	
6	IO_L04N_6	M1	NC	
6	IO_L06P_6	L4	NC	
6	IO_L06N_6	L3	NC	
6	IO_L43P_6	L2	NC	NC
6	IO_L43N_6	L1	NC	NC
6	IO_L45P_6	L5	NC	NC
6	IO_L45N_6/VREF_6	K5	NC	NC
6	IO_L91P_6	K4	NC	
6	IO_L91N_6	K3	NC	
6	IO_L93P_6	K2	NC	
6	IO_L93N_6/VREF_6	K1	NC	
6	IO_L94P_6	J4		
6	IO_L94N_6	J3		
6	IO_L96P_6	J2		
6	IO_L96N_6	J1		
7	IO_L96P_7	H1		
7	IO_L96N_7	H2		
7	IO_L94P_7	H3		
7	IO_L94N_7	H4		
7	IO_L93P_7/VREF_7	G1	NC	
7	IO_L93N_7	G2	NC	
7	IO_L91P_7	G3	NC	
7	IO_L91N_7	G4	NC	
7	IO_L45P_7/VREF_7	G5	NC	NC

Table 7: FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
0	IO_L93N_0	B10		
0	IO_L93P_0	A10		
0	IO_L94N_0/VREF_0	E11		
0	IO_L94P_0	F11		
0	IO_L95N_0/GCLK7P	D11		
0	IO_L95P_0/GCLK6S	C11		
0	IO_L96N_0/GCLK5P	B11		
0	IO_L96P_0/GCLK4S	A11		
1	IO_L96N_1/GCLK3P	F12		
1	IO_L96P_1/GCLK2S	F13		
1	IO_L95N_1/GCLK1P	E12		
1	IO_L95P_1/GCLK0S	D12		
1	IO_L94N_1	C12		
1	IO_L94P_1/VREF_1	B12		
1	IO_L93N_1	A13		
1	IO_L93P_1	B13		
1	IO_L92N_1	C13		
1	IO_L92P_1	D13		
1	IO_L91N_1	E13		
1	IO_L91P_1/VREF_1	E14		
1	IO_L54N_1	A14	NC	
1	IO_L54P_1	B14	NC	
1	IO_L52N_1	C14	NC	
1	IO_L52P_1	D14	NC	
1	IO_L51N_1/VREF_1	A15	NC	
1	IO_L51P_1	B15	NC	
1	IO_L49N_1	C15	NC	
1	IO_L49P_1	D15	NC	
1	IO_L24N_1	F14	NC	NC
1	IO_L24P_1	E15	NC	NC
1	IO_L22N_1	A16	NC	NC
1	IO_L22P_1	B16	NC	NC
1	IO_L21N_1/VREF_1	C16	NC	NC

Table 7: FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
3	IO_L52P_3	P18	NC	
3	IO_L51N_3/VREF_3	P22	NC	
3	IO_L51P_3	P21	NC	
3	IO_L49N_3	P20	NC	
3	IO_L49P_3	P19	NC	
3	IO_L48N_3	R22		
3	IO_L48P_3	R21		
3	IO_L46N_3	R20		
3	IO_L46P_3	R19		
3	IO_L45N_3/VREF_3	R18		
3	IO_L45P_3	P17		
3	IO_L43N_3	T22		
3	IO_L43P_3	T21		
3	IO_L24N_3	T20	NC	NC
3	IO_L24P_3	T19	NC	NC
3	IO_L22N_3	U22	NC	NC
3	IO_L22P_3	U21	NC	NC
3	IO_L21N_3/VREF_3	U20	NC	NC
3	IO_L21P_3	U19	NC	NC
3	IO_L19N_3	T18	NC	NC
3	IO_L19P_3	U18	NC	NC
3	IO_L06N_3	V22		
3	IO_L06P_3	V21		
3	IO_L04N_3	V20		
3	IO_L04P_3	V19		
3	IO_L03N_3/VREF_3	W22		
3	IO_L03P_3	W21		
3	IO_L02N_3/VRP_3	Y22		
3	IO_L02P_3/VRN_3	Y21		
3	IO_L01N_3	W20		
3	IO_L01P_3	AA20		
4	IO_L01N_4/BUSY/DOUT ⁽¹⁾	AB19		
4	IO_L01P_4/INIT_B	AA19		

Table 7: FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
NA	VCCINT	R16		
NA	VCCINT	R7		
NA	VCCINT	H16		
NA	VCCINT	H7		
NA	VCCINT	G16		
NA	VCCINT	G15		
NA	VCCINT	G8		
NA	VCCINT	G7		
NA	VCCINT	F17		
NA	VCCINT	F6		
NA	GND	AB22		
NA	GND	AB1		
NA	GND	AA21		
NA	GND	AA2		
NA	GND	Y20		
NA	GND	Y3		
NA	GND	W19		
NA	GND	W4		
NA	GND	P14		
NA	GND	P13		
NA	GND	P12		
NA	GND	P11		
NA	GND	P10		
NA	GND	P9		
NA	GND	N14		
NA	GND	N13		
NA	GND	N12		
NA	GND	N11		
NA	GND	N10		
NA	GND	N9		
NA	GND	M14		
NA	GND	M13		
NA	GND	M12		
NA	GND	M11		

Table 9: BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
0	IO_L69P_0/VREF_0	B9	NC	
0	IO_L70N_0	F10	NC	
0	IO_L70P_0	E10	NC	
0	IO_L72N_0	A10	NC	
0	IO_L72P_0	A11	NC	
0	IO_L73N_0	C10	NC	NC
0	IO_L73P_0	B10	NC	NC
0	IO_L91N_0/VREF_0	D11		
0	IO_L91P_0	C11		
0	IO_L92N_0	G11		
0	IO_L92P_0	E11		
0	IO_L93N_0	C12		
0	IO_L93P_0	B12		
0	IO_L94N_0/VREF_0	E12		
0	IO_L94P_0	D12		
0	IO_L95N_0/GCLK7P	G12		
0	IO_L95P_0/GCLK6S	F12		
0	IO_L96N_0/GCLK5P	H11		
0	IO_L96P_0/GCLK4S	H12		
1	IO_L96N_1/GCLK3P	A13		
1	IO_L96P_1/GCLK2S	A14		
1	IO_L95N_1/GCLK1P	B13		
1	IO_L95P_1/GCLK0S	C13		
1	IO_L94N_1	D13		
1	IO_L94P_1/VREF_1	E13		
1	IO_L93N_1	F13		
1	IO_L93P_1	G13		
1	IO_L92N_1	H13		
1	IO_L92P_1	H14		
1	IO_L91N_1	C14		
1	IO_L91P_1/VREF_1	D14		
1	IO_L73N_1	E14	NC	NC
1	IO_L73P_1	G14	NC	NC
1	IO_L72N_1	A15	NC	
1	IO_L72P_1	A16	NC	

Table 9: BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
2	IO_L01P_2	D23		
2	IO_L02N_2/VRP_2	E21		
2	IO_L02P_2/VRN_2	E22		
2	IO_L03N_2	F21		
2	IO_L03P_2/VREF_2	F20		
2	IO_L04N_2	G20		
2	IO_L04P_2	G19		
2	IO_L06N_2	H18		
2	IO_L06P_2	J17		
2	IO_L19N_2	D24		
2	IO_L19P_2	E23		
2	IO_L21N_2	E24		
2	IO_L21P_2/VREF_2	F24		
2	IO_L22N_2	F23		
2	IO_L22P_2	G23		
2	IO_L24N_2	G21		
2	IO_L24P_2	G22		
2	IO_L43N_2	H19		
2	IO_L43P_2	H20		
2	IO_L45N_2	J18		
2	IO_L45P_2/VREF_2	J19		
2	IO_L46N_2	K17		
2	IO_L46P_2	K18		
2	IO_L48N_2	H23		
2	IO_L48P_2	H24		
2	IO_L49N_2	H21		
2	IO_L49P_2	H22		
2	IO_L51N_2	J24		
2	IO_L51P_2/VREF_2	K24		
2	IO_L52N_2	J22		
2	IO_L52P_2	J23		
2	IO_L54N_2	J20		
2	IO_L54P_2	J21		
2	IO_L67N_2	K19	NC	
2	IO_L67P_2	K20	NC	
2	IO_L69N_2	L17	NC	

Table 11: FF896 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
7	IO_L52P_7	J29		
7	IO_L52N_7	K29		
7	IO_L51P_7/VREF_7	K27		
7	IO_L51N_7	J27		
7	IO_L50P_7	L24		
7	IO_L50N_7	K24		
7	IO_L49P_7	H27		
7	IO_L49N_7	J28		
7	IO_L48P_7	H26		
7	IO_L48N_7	J26		
7	IO_L47P_7	K25		
7	IO_L47N_7	J25		
7	IO_L46P_7	H28		
7	IO_L46N_7	H29		
7	IO_L45P_7/VREF_7	G28		
7	IO_L45N_7	F28		
7	IO_L44P_7	L23		
7	IO_L44N_7	K23		
7	IO_L43P_7	F30		
7	IO_L43N_7	G30		
7	IO_L24P_7	F26		
7	IO_L24N_7	G27		
7	IO_L23P_7	J24		
7	IO_L23N_7	H24		
7	IO_L22P_7	F29		
7	IO_L22N_7	G29		
7	IO_L21P_7/VREF_7	G26		
7	IO_L21N_7	G25		
7	IO_L20P_7	H25		
7	IO_L20N_7	G24		
7	IO_L19P_7	D30		
7	IO_L19N_7	E30		
7	IO_L06P_7	E27		
7	IO_L06N_7	F27		
7	IO_L05P_7	J23		
7	IO_L05N_7	H22		
7	IO_L04P_7	C29		

Table 11: FF896 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
2	VCCO_2	L10		
2	VCCO_2	L9		
2	VCCO_2	K9		
2	VCCO_2	E2		
3	VCCO_3	AF2		
3	VCCO_3	AA9		
3	VCCO_3	Y10		
3	VCCO_3	Y9		
3	VCCO_3	W10		
3	VCCO_3	W9		
3	VCCO_3	V10		
3	VCCO_3	V9		
3	VCCO_3	V3		
3	VCCO_3	U10		
3	VCCO_3	T10		
4	VCCO_4	AJ5		
4	VCCO_4	AH13		
4	VCCO_4	AB13		
4	VCCO_4	AB12		
4	VCCO_4	AB11		
4	VCCO_4	AB10		
4	VCCO_4	AA15		
4	VCCO_4	AA14		
4	VCCO_4	AA13		
4	VCCO_4	AA12		
4	VCCO_4	AA11		
5	VCCO_5	AJ26		
5	VCCO_5	AH18		
5	VCCO_5	AB21		
5	VCCO_5	AB20		
5	VCCO_5	AB19		
5	VCCO_5	AB18		
5	VCCO_5	AA20		
5	VCCO_5	AA19		
5	VCCO_5	AA18		
5	VCCO_5	AA17		
5	VCCO_5	AA16		

Table 11: FF896 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
NA	GND	AC1		
NA	GND	AA28		
NA	GND	AA3		
NA	GND	W26		
NA	GND	W19		
NA	GND	W18		
NA	GND	W17		
NA	GND	W16		
NA	GND	W15		
NA	GND	W14		
NA	GND	W13		
NA	GND	W12		
NA	GND	W5		
NA	GND	V19		
NA	GND	V18		
NA	GND	V17		
NA	GND	V16		
NA	GND	V15		
NA	GND	V14		
NA	GND	V13		
NA	GND	V12		
NA	GND	U24		
NA	GND	U19		
NA	GND	U18		
NA	GND	U17		
NA	GND	U16		
NA	GND	U15		
NA	GND	U14		
NA	GND	U13		
NA	GND	U12		
NA	GND	U7		
NA	GND	T19		
NA	GND	T18		
NA	GND	T17		
NA	GND	T16		
NA	GND	T15		
NA	GND	T14		

device shown in the No Connect column. Following this table are the **FF1152 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)**.

Table 12: FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
0	IO_L01N_0	D29	
0	IO_L01P_0	C29	
0	IO_L02N_0	H26	
0	IO_L02P_0	G26	
0	IO_L03N_0/VRP_0	E28	
0	IO_L03P_0/VRN_0	E27	
0	IO_L04N_0/VREF_0	F25	
0	IO_L04P_0	F26	
0	IO_L05N_0	H25	
0	IO_L05P_0	H24	
0	IO_L06N_0	E26	
0	IO_L06P_0	F27	
0	IO_L19N_0	B32	
0	IO_L19P_0	C33	
0	IO_L20N_0	J24	
0	IO_L20P_0	J23	
0	IO_L21N_0	C27	
0	IO_L21P_0/VREF_0	C28	
0	IO_L22N_0	B30	
0	IO_L22P_0	B31	
0	IO_L23N_0	K23	
0	IO_L23P_0	K22	
0	IO_L24N_0	C26	
0	IO_L24P_0	D27	
0	IO_L25N_0	A30	
0	IO_L25P_0	A31	
0	IO_L26N_0	G24	
0	IO_L26P_0	G25	
0	IO_L27N_0	E25	
0	IO_L27P_0/VREF_0	E24	
0	IO_L28N_0	D25	
0	IO_L28P_0	D26	
0	IO_L29N_0	H23	
0	IO_L29P_0	H22	

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
5	IO_L55N_5	AV28		
5	IO_L55P_5	AV27		
5	IO_L54N_5	AP27		
5	IO_L54P_5	AP26		
5	IO_L53N_5	AN25		
5	IO_L53P_5	AN26		
5	IO_L52N_5	AU29		
5	IO_L52P_5	AU28		
5	IO_L51N_5/VREF_5	AR28		
5	IO_L51P_5	AR27		
5	IO_L50N_5	AJ24		
5	IO_L50P_5	AJ25		
5	IO_L49N_5	AW30		
5	IO_L49P_5	AW29		
5	IO_L36N_5	AT29	NC	
5	IO_L36P_5	AT28	NC	
5	IO_L35N_5	AK25	NC	
5	IO_L35P_5	AL26	NC	
5	IO_L34N_5	AV31	NC	
5	IO_L34P_5	AV30	NC	
5	IO_L33N_5/VREF_5	AP29	NC	
5	IO_L33P_5	AP28	NC	
5	IO_L32N_5	AK26	NC	
5	IO_L32P_5	AJ26	NC	
5	IO_L31N_5	AW32	NC	
5	IO_L31P_5	AW31	NC	
5	IO_L30N_5	AM27		
5	IO_L30P_5	AM26		
5	IO_L29N_5	AN28		
5	IO_L29P_5	AN29		
5	IO_L28N_5	AU31		
5	IO_L28P_5	AU30		
5	IO_L27N_5/VREF_5	AT31		
5	IO_L27P_5	AT30		
5	IO_L26N_5	AH25		
5	IO_L26P_5	AH26		

Table 14: BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000

Bank	Pin Description	Pin Number	No Connect in XC2V2000
0	IO_L49N_0	C23	
0	IO_L49P_0	C22	
0	IO_L50N_0	E22	
0	IO_L50P_0	E21	
0	IO_L51N_0	F21	
0	IO_L51P_0/VREF_0	F20	
0	IO_L52N_0	A24	
0	IO_L52P_0	A23	
0	IO_L53N_0	E20	
0	IO_L53P_0	E19	
0	IO_L54N_0	B22	
0	IO_L54P_0	B21	
0	IO_L67N_0	D21	
0	IO_L67P_0	D20	
0	IO_L68N_0	J20	
0	IO_L68P_0	J19	
0	IO_L69N_0	F19	
0	IO_L69P_0/VREF_0	F18	
0	IO_L70N_0	A22	
0	IO_L70P_0	A21	
0	IO_L71N_0	H19	
0	IO_L71P_0	H17	
0	IO_L72N_0	C21	
0	IO_L72P_0	C20	
0	IO_L73N_0	B20	
0	IO_L73P_0	B19	
0	IO_L74N_0	G18	
0	IO_L74P_0	G17	
0	IO_L75N_0	E18	
0	IO_L75P_0/VREF_0	D17	
0	IO_L76N_0	A20	
0	IO_L76P_0	A19	
0	IO_L77N_0	D19	
0	IO_L77P_0	D18	
0	IO_L78N_0	C19	
0	IO_L78P_0	C17	
0	IO_L91N_0/VREF_0	K18	
0	IO_L91P_0	J18	

Table 14: BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000

Bank	Pin Description	Pin Number	No Connect in XC2V2000
6	IO_L67P_6	AB30	
6	IO_L67N_6	AA30	
6	IO_L68P_6	W26	
6	IO_L68N_6	V26	
6	IO_L69P_6	AB31	
6	IO_L69N_6/VREF_6	AA31	
6	IO_L70P_6	AA29	
6	IO_L70N_6	Y29	
6	IO_L71P_6	Y24	
6	IO_L71N_6	W24	
6	IO_L72P_6	V25	
6	IO_L72N_6	U25	
6	IO_L73P_6	Y28	
6	IO_L73N_6	W28	
6	IO_L74P_6	W23	
6	IO_L74N_6	V23	
6	IO_L75P_6	Y30	
6	IO_L75N_6/VREF_6	W30	
6	IO_L76P_6	Y31	
6	IO_L76N_6	W31	
6	IO_L77P_6	V27	
6	IO_L77N_6	U27	
6	IO_L78P_6	W29	
6	IO_L78N_6	U29	
6	IO_L91P_6	U23	
6	IO_L91N_6	T23	
6	IO_L92P_6	U26	
6	IO_L92N_6	T26	
6	IO_L93P_6	V28	
6	IO_L93N_6/VREF_6	U28	
6	IO_L94P_6	U24	
6	IO_L94N_6	T24	
6	IO_L95P_6	V30	
6	IO_L95N_6	U30	
6	IO_L96P_6	V31	
6	IO_L96N_6	U31	
7	IO_L96P_7	T27	

Table 14: BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000

Bank	Pin Description	Pin Number	No Connect in XC2V2000
7	IO_L06N_7	E28	
7	IO_L05P_7	K22	
7	IO_L05N_7	K21	
7	IO_L04P_7	F29	
7	IO_L04N_7	E29	
7	IO_L03P_7/VREF_7	H26	
7	IO_L03N_7	H25	
7	IO_L02P_7/VRN_7	G26	
7	IO_L02N_7/VRP_7	F27	
7	IO_L01P_7	D30	
7	IO_L01N_7	D29	
0	VCCO_0	C18	
0	VCCO_0	C25	
0	VCCO_0	F22	
0	VCCO_0	H18	
0	VCCO_0	L17	
0	VCCO_0	L18	
0	VCCO_0	L19	
0	VCCO_0	L20	
0	VCCO_0	M17	
0	VCCO_0	M18	
0	VCCO_0	M19	
1	VCCO_1	C7	
1	VCCO_1	C14	
1	VCCO_1	F10	
1	VCCO_1	H14	
1	VCCO_1	L12	
1	VCCO_1	L13	
1	VCCO_1	L14	
1	VCCO_1	L15	
1	VCCO_1	M13	
1	VCCO_1	M14	
1	VCCO_1	M15	
2	VCCO_2	G3	
2	VCCO_2	K6	
2	VCCO_2	M11	
2	VCCO_2	N11	