# AMD Xilinx - XC2V500-5FGG256C Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 768 |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 589824 |
| Number of I/O | 172 |
| Number of Gates | 500000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 256-BGA |
| Supplier Device Package | 256-FBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc2v500-5fgg256c |

Each block SelectRAM cell is a fully synchronous memory, as illustrated in Figure 30. The two ports have independent inputs and outputs and are independently clocked.

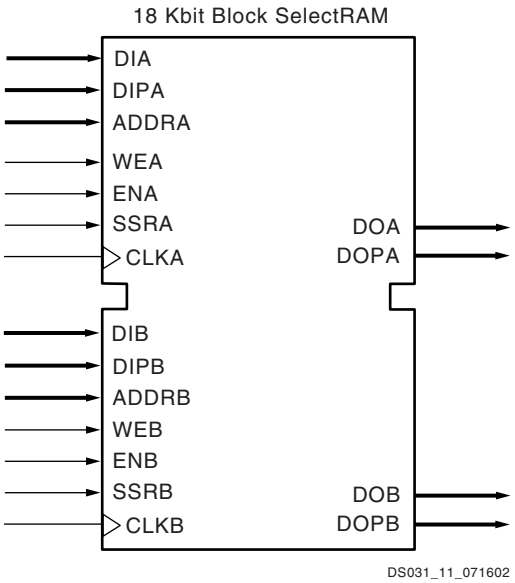



*Figure 30:* **18 Kbit Block SelectRAM in Dual-Port Mode**

### Port Aspect Ratios

Table 16 shows the depth and the width aspect ratios for the 18 Kbit block SelectRAM. Virtex-II block SelectRAM also includes dedicated routing resources to provide an efficient interface with CLBs, block SelectRAM, and multipliers.

*Table 16:* **18 Kbit Block SelectRAM Port Aspect Ratio**

| Width | Depth | Address Bus | Data Bus | Parity Bus |
|---|---|---|---|---|
| 1 | 16,384 | ADDR[13:0] | DATA[0] | N/A |
| 2 | 8,192 | ADDR[12:0] | DATA[1:0] | N/A |
| 4 | 4,096 | ADDR[11:0] | DATA[3:0] | N/A |
| 9 | 2,048 | ADDR[10:0] | DATA[7:0] | Parity[0] |
| 18 | 1,024 | ADDR[9:0] | DATA[15:0] | Parity[1:0] |
| 36 | 512 | ADDR[8:0] | DATA[31:0] | Parity[3:0] |

### *Read/Write Operations*

The Virtex-II block SelectRAM read operation is fully synchronous. An address is presented, and the read operation is enabled by control signals WEA and WEB in addition to ENA or ENB. Then, depending on clock polarity, a rising or falling clock edge causes the stored data to be loaded into output registers.

The write operation is also fully synchronous. Data and address are presented, and the write operation is enabled by control signals WEA or WEB in addition to ENA or ENB. Then, again depending on the clock input mode, a rising or falling clock edge causes the data to be loaded into the memory cell addressed.

A write operation performs a simultaneous read operation. Three different options are available, selected by configuration:

1. **"WRITE_FIRST"**

   The "WRITE_FIRST" option is a transparent mode. The same clock edge that writes the data input (DI) into the memory also transfers DI into the output registers DO as shown in Figure 31.

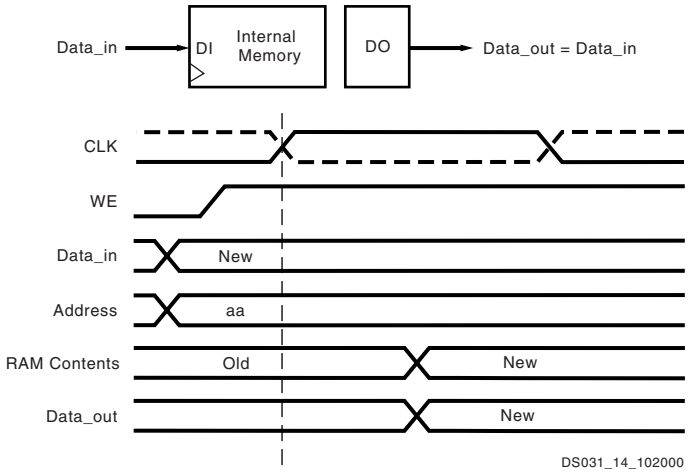



*Figure 31:* **WRITE_FIRST Mode**

2. **"READ_FIRST"**

   The "READ_FIRST" option is a read-before-write mode.

   The same clock edge that writes data input (DI) into the memory also transfers the prior content of the memory cell addressed into the data output registers DO, as shown in Figure 32.

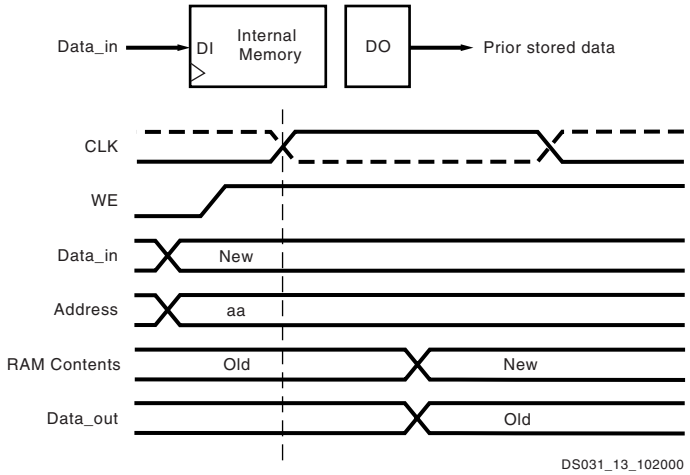



*Figure 32:* **READ_FIRST Mode**

The Virtex-II implementation process is comprised of Synthesis, translation, mapping, place and route, and configuration file generation. While the tools can be run individually, many designers choose to run the entire implementation process with the click of a button. To assist those who prefer to script their design flows, Xilinx provides Xflow, an automated single command line process.

### *Design Verification*

In addition to conventional design verification using static timing analysis or simulation techniques, Xilinx offers powerful in-circuit debugging techniques using ChipScope ILA (Integrated Logic Analysis). The reconfigurable nature of Xilinx FPGAs means that designs can be verified in real time without the need for extensive sets of software simulation vectors.

For simulation, the system extracts post-layout timing information from the design database, and back-annotates this information into the netlist for use by the simulator. The back annotation features a variety of patented Xilinx techniques, resulting in the industry's most powerful simulation flows. Alternatively, timing-critical portions of a design can be verified using the Xilinx static timing analyzer or a third party static timing analysis tool like Synopsys Prime Time™, by exporting timing data in the STAMP data format.

For in-circuit debugging, ChipScope ILA enables designers to analyze the real-time behavior of a device while operating at full system speeds. Logic analysis commands and captured data are transferred between the ChipScope software and ILA cores within the Virtex-II FPGA, using industry standard JTAG protocols. These JTAG transactions are driven over an optional download cable (MultiLINX or JTAG), connecting the Virtex device in the target system to a PC or workstation.

ChipScope ILA was designed to look and feel like a logic analyzer, making it easy to begin debugging a design immediately. Modifications to the desired logic analysis can be downloaded directly into the system in a matter of minutes.

## Other Unique Features of Virtex-II Design Flow

Xilinx design flows feature a number of unique capabilities. Among these are efficient incremental HDL design flows; a robust capability that is enabled by Xilinx exclusive hierarchical floorplanning capabilities. Another powerful design capability only available in the Xilinx design flow is "Modular Design", part of the Xilinx suite of team design tools, which enables autonomous design, implementation, and verification of design modules.

### *Incremental Synthesis*

Xilinx unique hierarchical floorplanning capabilities enable designers to create a programmable logic design by isolating design changes within one hierarchical "logic block", and perform synthesis, verification and implementation processes on that specific logic block. By preserving the logic in unchanged portions of a design, Xilinx incremental design makes the high-density design process more efficient.

Xilinx hierarchical floorplanning capabilities can be specified using the high-level floorplanner or a preferred RTL floorplanner (see the Xilinx web site for a list of supported EDA partners). When used in conjunction with one of the EDA partners' floorplanners, higher performance results can be achieved, as many synthesis tools use this more predictable detailed physical implementation information to establish more aggressive and accurate timing estimates when performing their logic optimizations.

### *Modular Design*

Xilinx innovative modular design capabilities take the incremental design process one step further by enabling the designer to delegate responsibility for completing the design, synthesis, verification, and implementation of a hierarchical "logic block" to an arbitrary number of designers - assigning a specific region within the target FPGA for exclusive use by each of the team members.

This team design capability enables an autonomous approach to design modules, changing the hand-off point to the lead designer or integrator from "my module works in simulation" to "my module works in the FPGA". This unique design methodology also leverages the Xilinx hierarchical floorplanning capabilities and enables the Xilinx (or EDA partner) floorplanner to manage the efficient implementation of very high-density FPGAs.

Virtex-II FPGA device. Timing is similar to the Slave Serial-MAP mode except that CCLK is supplied by the Virtex-II FPGA.

### *Boundary-Scan (JTAG, IEEE 1532) Mode*

In Boundary-Scan mode, dedicated pins are used for configuring the Virtex-II device. The configuration is done entirely through the IEEE 1149.1 Test Access Port (TAP). Virtex-II device configuration using Boundary-Scan is compatible with the IEEE 1149.1-1993 standard and the new IEEE 1532 standard for In-System Configurable (ISC) devices. The IEEE 1532 standard is backward compliant with the IEEE 1149.1-1993 TAP and state machine. The IEEE Standard 1532 for In-System Configurable (ISC) devices is intended to be programmed, reprogrammed, or tested on the board via a physical and logical protocol.

Configuration through the Boundary-Scan port is always available, independent of the mode selection. Selecting the Boundary-Scan mode simply turns off the other modes.

*Table 25:* **Virtex-II Configuration Mode Pin Settings**

| Configuration Mode(1) | M2 | M1 | M0 | CCLK Direction | Data Width | Serial $D_{OUT}$(2) |
|---|---|---|---|---|---|---|
| Master Serial | 0 | 0 | 0 | Out | 1 | Yes |
| Slave Serial | 1 | 1 | 1 | In | 1 | Yes |
| Master SelectMAP | 0 | 1 | 1 | Out | 8 | No |
| Slave SelectMAP | 1 | 1 | 0 | In | 8 | No |
| Boundary-Scan | 1 | 0 | 1 | N/A | 1 | No |

**Notes:**
1. The HSWAP_EN pin controls the pull-ups. Setting M2, M1, and M0 selects the configuration mode, while the HSWAP_EN pin controls whether or not the pull-ups are used.
2. Daisy chaining is possible only in modes where Serial $D_{OUT}$ is used. For example, in SelectMAP modes, the first device does NOT support daisy chaining of downstream devices.

Table 26 lists the total number of bits required to configure each device.

*Table 26:* **Virtex-II Bitstream Lengths**

| Device | # of Configuration Bits |
|---|---|
| XC2V40 | 338,976 |
| XC2V80 | 598,816 |
| XC2V250 | 1,593,632 |
| XC2V500 | 2,560,544 |
| XC2V1000 | 4,082,592 |
| XC2V1500 | 5,170,208 |
| XC2V2000 | 6,812,960 |
| XC2V3000 | 10,494,368 |
| XC2V4000 | 15,659,936 |
| XC2V6000 | 21,849,504 |
| XC2V8000 | 26,194,208 |

## Configuration Sequence

The configuration of Virtex-II devices is a three-phase process after Power On Reset or POR. POR occurs when $V_{CCINT}$ is greater than 1.2V, $V_{CCAUX}$ is greater than 2.5V, and $V_{CCO}$ (bank 4) is greater than 1.5V. Once the POR voltages have been reached, the three-phase process begins.

First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process.

Configuration is automatically initiated on power-up unless it is delayed by the user. The INIT_B pin can be held Low using an open-drain driver. An open-drain is required since INIT_B is a bidirectional open-drain pin that is held Low by a Virtex-II FPGA device while the configuration memory is being cleared. Extending the time that the pin is Low causes the configuration sequencer to wait. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

The configuration process can also be initiated by asserting the PROG_B pin. The end of the memory-clearing phase is signaled by the INIT_B pin going High, and the completion of the entire process is signaled by the DONE pin going High. The Global Set/Reset (GSR) signal is pulsed after the last frame of configuration data is written but before the start-up sequence. The GSR signal resets all flip-flops on the device.

The default start-up sequence is that one CCLK cycle after DONE goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary. One CCLK cycle later, the Global Write Enable (GWE) signal is released. This permits the internal storage ele-

# Virtex-II Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

## Global Clock Setup and Hold for LVTTL Standard, *With* DCM

*Table 36:* **Global Clock Setup and Hold for LVTTL Standard, *With* DCM**

| Description | Symbol | Device | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -6 | -5 | -4 | |
| Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard.<br>For data input with different standards, adjust the setup time delay by the values shown in IOB Input Switching Characteristics Standard Adjustments, page 11. | | | | | | |
| No Delay<br>Global Clock and IFF with DCM | $T_{PSDCM}/T_{PHDCM}$ | XC2V40 | 1.60/–0.90 | 1.60/–0.90 | 1.84/–0.76 | ns |
| | | XC2V80 | 1.60/–0.90 | 1.60/–0.90 | 1.84/–0.76 | ns |
| | | XC2V250 | 1.60/–0.90 | 1.60/–0.90 | 1.84/–0.76 | ns |
| | | XC2V500 | 1.60/–0.90 | 1.60/–0.90 | 1.84/–0.76 | ns |
| | | XC2V1000 | 1.60/–0.90 | 1.60/–0.90 | 1.84/–0.76 | ns |
| | | XC2V1500 | 1.60/–0.90 | 1.60/–0.90 | 1.84/–0.76 | ns |
| | | XC2V2000 | 1.70/–0.90 | 1.70/–0.90 | 1.96/–0.76 | ns |
| | | XC2V3000 | 1.70/–0.90 | 1.70/–0.90 | 1.96/–0.76 | ns |
| | | XC2V4000 | 1.70/–0.90 | 1.70/–0.90 | 1.96/–0.76 | ns |
| | | XC2V6000 | 1.70/–0.90 | 1.70/–0.90 | 1.96/–0.76 | ns |
| | | XC2V8000 | | 1.70/–0.90 | 1.96/–0.76 | ns |

**Notes:**
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.

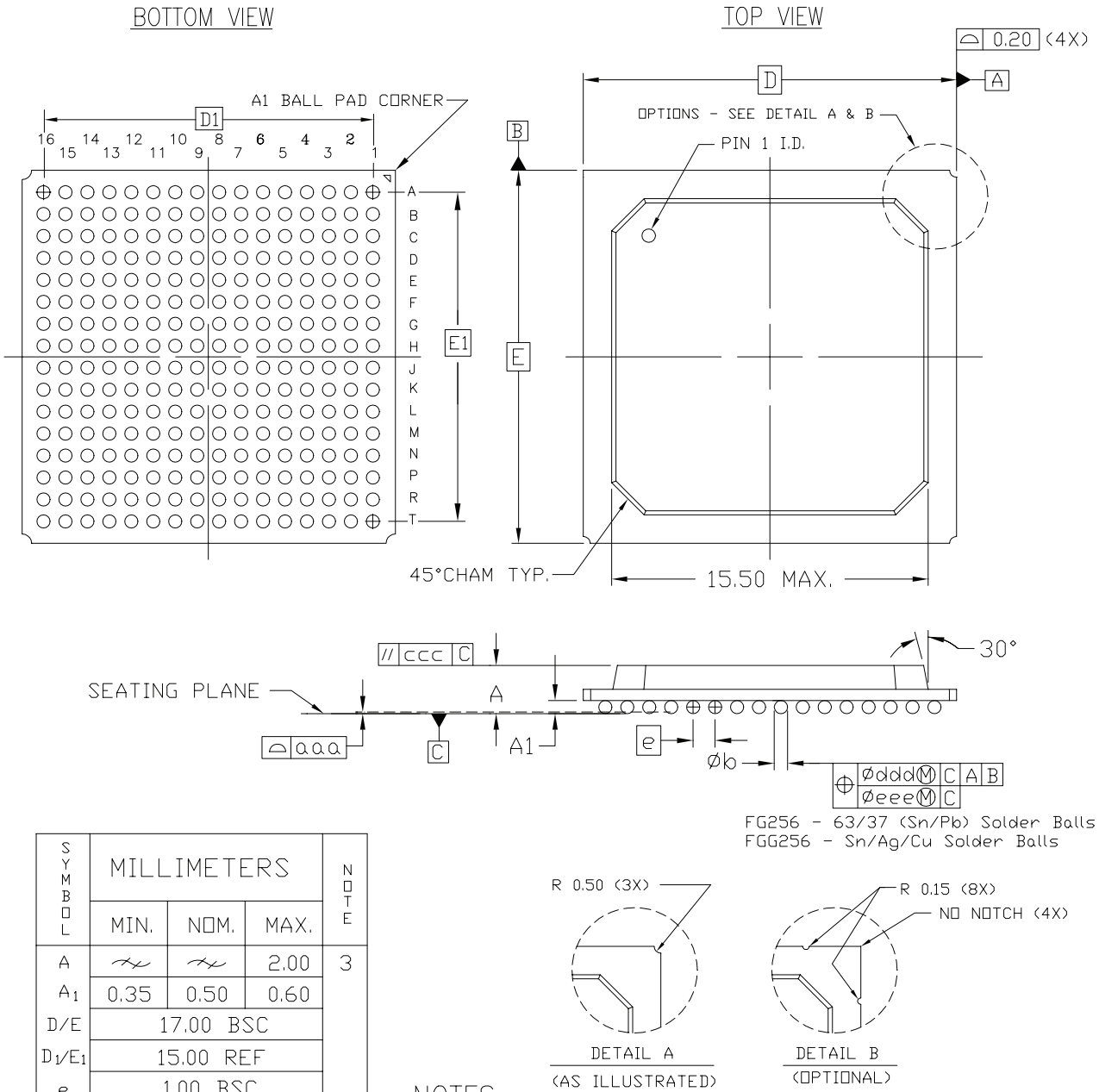
*Table 6:* **FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

| Bank | Pin Description | Pin Number | No Connect in XC2V40 | No Connect in XC2V80 |
|---|---|---|---|---|
| 4 | IO_L91N_4/VREF_4 | R11 | NC | NC |
| 4 | IO_L91P_4 | T11 | NC | NC |
| 4 | IO_L92N_4 | M11 | NC | NC |
| 4 | IO_L92P_4 | M10 | NC | NC |
| 4 | IO_L93N_4 | N10 | NC | NC |
| 4 | IO_L93P_4 | P10 | NC | NC |
| 4 | IO_L94N_4/VREF_4 | R10 | | |
| 4 | IO_L94P_4 | T10 | | |
| 4 | IO_L95N_4/GCLK3S | N9 | | |
| 4 | IO_L95P_4/GCLK2P | P9 | | |
| 4 | IO_L96N_4/GCLK1S | R9 | | |
| 4 | IO_L96P_4/GCLK0P | T9 | | |
| | | | | |
| 5 | IO_L96N_5/GCLK7S | T8 | | |
| 5 | IO_L96P_5/GCLK6P | R8 | | |
| 5 | IO_L95N_5/GCLK5S | P8 | | |
| 5 | IO_L95P_5/GCLK4P | N8 | | |
| 5 | IO_L94N_5 | T7 | | |
| 5 | IO_L94P_5/VREF_5 | R7 | | |
| 5 | IO_L93N_5 | P7 | NC | NC |
| 5 | IO_L93P_5 | N7 | NC | NC |
| 5 | IO_L92N_5 | M7 | NC | NC |
| 5 | IO_L92P_5 | M6 | NC | NC |
| 5 | IO_L91N_5 | T6 | NC | NC |
| 5 | IO_L91P_5/VREF_5 | R6 | NC | NC |
| 5 | IO_L05N_5/VRP_5 | P6 | NC | NC |
| 5 | IO_L05P_5/VRN_5 | N6 | NC | NC |
| 5 | IO_L04N_5 | T5 | NC | NC |
| 5 | IO_L04P_5/VREF_5 | R5 | NC | NC |
| 5 | IO_L03N_5/D4/ALT_VRP_5 | P5 | | |
| 5 | IO_L03P_5/D5/ALT_VRN_5 | N5 | | |
| 5 | IO_L02N_5/D6 | R4 | | |
| 5 | IO_L02P_5/D7 | P4 | | |
| 5 | IO_L01N_5/RDWR_B | T4 | | |

*Table 6:* **FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

| Bank | Pin Description | Pin Number | No Connect in XC2V40 | No Connect in XC2V80 |
|---|---|---|---|---|
| 5 | IO_L01P_5/CS_B | T3 | | |
| | | | | |
| 6 | IO_L01P_6 | P1 | | |
| 6 | IO_L01N_6 | N1 | | |
| 6 | IO_L02P_6/VRN_6 | N3 | | |
| 6 | IO_L02N_6/VRP_6 | N2 | | |
| 6 | IO_L03P_6 | M4 | | |
| 6 | IO_L03N_6/VREF_6 | M3 | | |
| 6 | IO_L04P_6 | M2 | NC | |
| 6 | IO_L04N_6 | M1 | NC | |
| 6 | IO_L06P_6 | L4 | NC | |
| 6 | IO_L06N_6 | L3 | NC | |
| 6 | IO_L43P_6 | L2 | NC | NC |
| 6 | IO_L43N_6 | L1 | NC | NC |
| 6 | IO_L45P_6 | L5 | NC | NC |
| 6 | IO_L45N_6/VREF_6 | K5 | NC | NC |
| 6 | IO_L91P_6 | K4 | NC | |
| 6 | IO_L91N_6 | K3 | NC | |
| 6 | IO_L93P_6 | K2 | NC | |
| 6 | IO_L93N_6/VREF_6 | K1 | NC | |
| 6 | IO_L94P_6 | J4 | | |
| 6 | IO_L94N_6 | J3 | | |
| 6 | IO_L96P_6 | J2 | | |
| 6 | IO_L96N_6 | J1 | | |
| | | | | |
| 7 | IO_L96P_7 | H1 | | |
| 7 | IO_L96N_7 | H2 | | |
| 7 | IO_L94P_7 | H3 | | |
| 7 | IO_L94N_7 | H4 | | |
| 7 | IO_L93P_7/VREF_7 | G1 | NC | |
| 7 | IO_L93N_7 | G2 | NC | |
| 7 | IO_L91P_7 | G3 | NC | |
| 7 | IO_L91N_7 | G4 | NC | |
| 7 | IO_L45P_7/VREF_7 | G5 | NC | NC |

## FG256/FGG256 Fine-Pitch BGA Package Specifications (1.00mm pitch)




| SYMBOL | MILLIMETERS | | | NOTE |
|---|---|---|---|---|
| | MIN. | NOM. | MAX. | |
| A | | | 2.00 | 3 |
| $A_1$ | 0.35 | 0.50 | 0.60 | |
| D/E | 17.00 BSC | | | |
| $D_1/E_1$ | 15.00 REF | | | |
| e | 1.00 BSC | | | |
| øb | 0.50 | 0.60 | 0.70 | |
| aaa | | | 0.20 | |
| ccc | | | 0.35 | |
| ddd | | | 0.30 | |
| eee | | | 0.10 | |
| M | 16 | | | 2 |

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994.
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. NOMINAL DIMENSION IS TYPICALLY 1.60-1.73mm
4. CONFORMS TO JEDEC MS-034-AAF-1

256-BALL FINE PITCH BGA (FG256/FGG256)

*Figure 2:* **FG256/FGG256 Fine-Pitch BGA Package Specifications**

*Table 7:* **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

| Bank | Pin Description | Pin Number | No Connect in XC2V250 | No Connect in XC2V500 |
|---|---|---|---|---|
| 0 | IO_L93N_0 | B10 | | |
| 0 | IO_L93P_0 | A10 | | |
| 0 | IO_L94N_0/VREF_0 | E11 | | |
| 0 | IO_L94P_0 | F11 | | |
| 0 | IO_L95N_0/GCLK7P | D11 | | |
| 0 | IO_L95P_0/GCLK6S | C11 | | |
| 0 | IO_L96N_0/GCLK5P | B11 | | |
| 0 | IO_L96P_0/GCLK4S | A11 | | |
| | | | | |
| 1 | IO_L96N_1/GCLK3P | F12 | | |
| 1 | IO_L96P_1/GCLK2S | F13 | | |
| 1 | IO_L95N_1/GCLK1P | E12 | | |
| 1 | IO_L95P_1/GCLK0S | D12 | | |
| 1 | IO_L94N_1 | C12 | | |
| 1 | IO_L94P_1/VREF_1 | B12 | | |
| 1 | IO_L93N_1 | A13 | | |
| 1 | IO_L93P_1 | B13 | | |
| 1 | IO_L92N_1 | C13 | | |
| 1 | IO_L92P_1 | D13 | | |
| 1 | IO_L91N_1 | E13 | | |
| 1 | IO_L91P_1/VREF_1 | E14 | | |
| 1 | IO_L54N_1 | A14 | NC | |
| 1 | IO_L54P_1 | B14 | NC | |
| 1 | IO_L52N_1 | C14 | NC | |
| 1 | IO_L52P_1 | D14 | NC | |
| 1 | IO_L51N_1/VREF_1 | A15 | NC | |
| 1 | IO_L51P_1 | B15 | NC | |
| 1 | IO_L49N_1 | C15 | NC | |
| 1 | IO_L49P_1 | D15 | NC | |
| 1 | IO_L24N_1 | F14 | NC | NC |
| 1 | IO_L24P_1 | E15 | NC | NC |
| 1 | IO_L22N_1 | A16 | NC | NC |
| 1 | IO_L22P_1 | B16 | NC | NC |
| 1 | IO_L21N_1/VREF_1 | C16 | NC | NC |

*Table 7:* **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

| Bank | Pin Description | Pin Number | No Connect in XC2V250 | No Connect in XC2V500 |
|---|---|---|---|---|
| 2 | IO_L45N_2 | H19 | | |
| 2 | IO_L45P_2/VREF_2 | H20 | | |
| 2 | IO_L46N_2 | H21 | | |
| 2 | IO_L46P_2 | H22 | | |
| 2 | IO_L48N_2 | J17 | | |
| 2 | IO_L48P_2 | J18 | | |
| 2 | IO_L49N_2 | J19 | NC | |
| 2 | IO_L49P_2 | J20 | NC | |
| 2 | IO_L51N_2 | J21 | NC | |
| 2 | IO_L51P_2/VREF_2 | J22 | NC | |
| 2 | IO_L52N_2 | K17 | NC | |
| 2 | IO_L52P_2 | K18 | NC | |
| 2 | IO_L54N_2 | K19 | NC | |
| 2 | IO_L54P_2 | K20 | NC | |
| 2 | IO_L91N_2 | K21 | | |
| 2 | IO_L91P_2 | K22 | | |
| 2 | IO_L93N_2 | L17 | | |
| 2 | IO_L93P_2/VREF_2 | L18 | | |
| 2 | IO_L94N_2 | L19 | | |
| 2 | IO_L94P_2 | L20 | | |
| 2 | IO_L96N_2 | L21 | | |
| 2 | IO_L96P_2 | L22 | | |
| | | | | |
| 3 | IO_L96N_3 | M21 | | |
| 3 | IO_L96P_3 | M20 | | |
| 3 | IO_L94N_3 | M19 | | |
| 3 | IO_L94P_3 | M18 | | |
| 3 | IO_L93N_3/VREF_3 | M17 | | |
| 3 | IO_L93P_3 | N17 | | |
| 3 | IO_L91N_3 | N22 | | |
| 3 | IO_L91P_3 | N21 | | |
| 3 | IO_L54N_3 | N20 | NC | |
| 3 | IO_L54P_3 | N19 | NC | |
| 3 | IO_L52N_3 | N18 | NC | |

*Table 7:* **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

| Bank | Pin Description | Pin Number | No Connect in XC2V250 | No Connect in XC2V500 |
|---|---|---|---|---|
| 4 | IO_L95N_4/GCLK3S | W12 | | |
| 4 | IO_L95P_4/GCLK2P | Y12 | | |
| 4 | IO_L96N_4/GCLK1S | AA12 | | |
| 4 | IO_L96P_4/GCLK0P | AB12 | | |
| | | | | |
| 5 | IO_L96N_5/GCLK7S | AA11 | | |
| 5 | IO_L96P_5/GCLK6P | Y11 | | |
| 5 | IO_L95N_5/GCLK5S | W11 | | |
| 5 | IO_L95P_5/GCLK4P | V11 | | |
| 5 | IO_L94N_5 | U11 | | |
| 5 | IO_L94P_5/VREF_5 | U10 | | |
| 5 | IO_L93N_5 | AB10 | | |
| 5 | IO_L93P_5 | AA10 | | |
| 5 | IO_L92N_5 | Y10 | | |
| 5 | IO_L92P_5 | W10 | | |
| 5 | IO_L91N_5 | V10 | | |
| 5 | IO_L91P_5/VREF_5 | V9 | | |
| 5 | IO_L54N_5 | AB9 | NC | |
| 5 | IO_L54P_5 | AA9 | NC | |
| 5 | IO_L52N_5 | Y9 | NC | |
| 5 | IO_L52P_5 | W9 | NC | |
| 5 | IO_L51N_5/VREF_5 | AB8 | NC | |
| 5 | IO_L51P_5 | AA8 | NC | |
| 5 | IO_L49N_5 | Y8 | NC | |
| 5 | IO_L49P_5 | W8 | NC | |
| 5 | IO_L24N_5 | U9 | NC | NC |
| 5 | IO_L24P_5 | V8 | NC | NC |
| 5 | IO_L22N_5 | AB7 | NC | NC |
| 5 | IO_L22P_5 | AA7 | NC | NC |
| 5 | IO_L21N_5/VREF_5 | Y7 | NC | NC |
| 5 | IO_L21P_5 | W7 | NC | NC |
| 5 | IO_L19N_5 | AB6 | NC | NC |
| 5 | IO_L19P_5 | AA6 | NC | NC |
| 5 | IO_L06N_5 | Y6 | | |

*Table 8:* **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

| Bank | Pin Description | Pin Number | No Connect in XC2V1500 | No Connect in XC2V2000 |
|---|---|---|---|---|
| NA | VCCINT | H19 | | |
| NA | VCCINT | H8 | | |
| NA | GND | AF26 | | |
| NA | GND | AF1 | | |
| NA | GND | AE25 | | |
| NA | GND | AE14 | | |
| NA | GND | AE13 | | |
| NA | GND | AE2 | | |
| NA | GND | AD24 | | |
| NA | GND | AD3 | | |
| NA | GND | AC23 | | |
| NA | GND | AC4 | | |
| NA | GND | AB22 | | |
| NA | GND | AB5 | | |
| NA | GND | AA21 | | |
| NA | GND | AA6 | | |
| NA | GND | U17 | | |
| NA | GND | U16 | | |
| NA | GND | U15 | | |
| NA | GND | U14 | | |
| NA | GND | U13 | | |
| NA | GND | U12 | | |
| NA | GND | U11 | | |
| NA | GND | U10 | | |
| NA | GND | T17 | | |
| NA | GND | T16 | | |
| NA | GND | T15 | | |
| NA | GND | T14 | | |
| NA | GND | T13 | | |
| NA | GND | T12 | | |
| NA | GND | T11 | | |
| NA | GND | T10 | | |
| NA | GND | R17 | | |
| NA | GND | R16 | | |
| NA | GND | R15 | | |
| NA | GND | R14 | | |
| NA | GND | R13 | | |

*Table 9:* **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

| Bank | Pin Description | Pin Number | No Connect in XC2V1000 | No Connect in XC2V1500 |
|---|---|---|---|---|
| 6 | IO_L91N_6 | P4 | | |
| 6 | IO_L93P_6 | N4 | | |
| 6 | IO_L93N_6/VREF_6 | N3 | | |
| 6 | IO_L94P_6 | N6 | | |
| 6 | IO_L94N_6 | N5 | | |
| 6 | IO_L96P_6 | N8 | | |
| 6 | IO_L96N_6 | N7 | | |
| | | | | |
| 7 | IO_L96P_7 | N2 | | |
| 7 | IO_L96N_7 | M1 | | |
| 7 | IO_L94P_7 | M2 | | |
| 7 | IO_L94N_7 | M3 | | |
| 7 | IO_L93P_7/VREF_7 | M4 | | |
| 7 | IO_L93N_7 | M5 | | |
| 7 | IO_L91P_7 | M6 | | |
| 7 | IO_L91N_7 | M7 | | |
| 7 | IO_L73P_7 | M8 | NC | NC |
| 7 | IO_L73N_7 | L8 | NC | NC |
| 7 | IO_L72P_7 | L1 | NC | |
| 7 | IO_L72N_7 | K1 | NC | |
| 7 | IO_L70P_7 | K2 | NC | |
| 7 | IO_L70N_7 | K3 | NC | |
| 7 | IO_L69P_7/VREF_7 | L3 | NC | |
| 7 | IO_L69N_7 | L4 | NC | |
| 7 | IO_L67P_7 | L5 | NC | |
| 7 | IO_L67N_7 | L7 | NC | |
| 7 | IO_L54P_7 | J1 | | |
| 7 | IO_L54N_7 | H1 | | |
| 7 | IO_L52P_7 | J2 | | |
| 7 | IO_L52N_7 | J3 | | |
| 7 | IO_L51P_7/VREF_7 | J4 | | |
| 7 | IO_L51N_7 | J5 | | |
| 7 | IO_L49P_7 | K5 | | |
| 7 | IO_L49N_7 | K6 | | |
| 7 | IO_L48P_7 | F1 | | |
| 7 | IO_L48N_7 | F2 | | |

*Table 10:* **BG728 BGA — XC2V3000**

| Bank | Pin Description | Pin Number |
|---|---|---|
| 2 | IO_L19P_2 | F26 |
| 2 | IO_L21N_2 | F27 |
| 2 | IO_L21P_2/VREF_2 | G27 |
| 2 | IO_L22N_2 | G23 |
| 2 | IO_L22P_2 | H23 |
| 2 | IO_L24N_2 | G25 |
| 2 | IO_L24P_2 | G26 |
| 2 | IO_L25N_2 | H21 |
| 2 | IO_L25P_2 | J21 |
| 2 | IO_L27N_2 | H22 |
| 2 | IO_L27P_2/VREF_2 | J22 |
| 2 | IO_L28N_2 | H24 |
| 2 | IO_L28P_2 | H25 |
| 2 | IO_L30N_2 | H27 |
| 2 | IO_L30P_2 | J27 |
| 2 | IO_L43N_2 | J23 |
| 2 | IO_L43P_2 | J24 |
| 2 | IO_L45N_2 | J25 |
| 2 | IO_L45P_2/VREF_2 | J26 |
| 2 | IO_L46N_2 | K20 |
| 2 | IO_L46P_2 | K21 |
| 2 | IO_L48N_2 | K22 |
| 2 | IO_L48P_2 | K23 |
| 2 | IO_L49N_2 | K24 |
| 2 | IO_L49P_2 | K25 |
| 2 | IO_L51N_2 | K26 |
| 2 | IO_L51P_2/VREF_2 | K27 |
| 2 | IO_L52N_2 | L20 |
| 2 | IO_L52P_2 | M20 |
| 2 | IO_L54N_2 | L21 |
| 2 | IO_L54P_2 | L22 |
| 2 | IO_L67N_2 | L24 |
| 2 | IO_L67P_2 | L25 |
| 2 | IO_L69N_2 | L26 |
| 2 | IO_L69P_2/VREF_2 | L27 |
| 2 | IO_L70N_2 | M19 |

*Table 11:* **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

| Bank | Pin Description | Pin Number | No Connect in the XC2V1000 | No Connect in the XC2V1500 |
|---|---|---|---|---|
| NA | GND | T13 | | |
| NA | GND | T12 | | |
| NA | GND | R19 | | |
| NA | GND | R18 | | |
| NA | GND | R17 | | |
| NA | GND | R16 | | |
| NA | GND | R15 | | |
| NA | GND | R14 | | |
| NA | GND | R13 | | |
| NA | GND | R12 | | |
| NA | GND | P24 | | |
| NA | GND | P19 | | |
| NA | GND | P18 | | |
| NA | GND | P17 | | |
| NA | GND | P16 | | |
| NA | GND | P15 | | |
| NA | GND | P14 | | |
| NA | GND | P13 | | |
| NA | GND | P12 | | |
| NA | GND | P7 | | |
| NA | GND | N19 | | |
| NA | GND | N18 | | |
| NA | GND | N17 | | |
| NA | GND | N16 | | |
| NA | GND | N15 | | |
| NA | GND | N14 | | |
| NA | GND | N13 | | |
| NA | GND | N12 | | |
| NA | GND | M26 | | |
| NA | GND | M19 | | |
| NA | GND | M18 | | |
| NA | GND | M17 | | |
| NA | GND | M16 | | |
| NA | GND | M15 | | |
| NA | GND | M14 | | |
| NA | GND | M13 | | |
| NA | GND | M12 | | |

*Table 12:* **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

| Bank | Pin Description | Pin Number | No Connect in the XC2V3000 |
|---|---|---|---|
| 3 | IO_L83P_3 | Y4 | NC |
| 3 | IO_L82N_3 | W11 | NC |
| 3 | IO_L82P_3 | V11 | NC |
| 3 | IO_L81N_3/VREF_3 | W8 | NC |
| 3 | IO_L81P_3 | Y8 | NC |
| 3 | IO_L80N_3 | W2 | NC |
| 3 | IO_L80P_3 | Y1 | NC |
| 3 | IO_L79N_3 | AA3 | NC |
| 3 | IO_L79P_3 | AB3 | NC |
| 3 | IO_L78N_3 | Y6 | |
| 3 | IO_L78P_3 | AA6 | |
| 3 | IO_L77N_3 | AA4 | |
| 3 | IO_L77P_3 | AB4 | |
| 3 | IO_L76N_3 | Y7 | |
| 3 | IO_L76P_3 | AA8 | |
| 3 | IO_L75N_3/VREF_3 | Y10 | |
| 3 | IO_L75P_3 | AA10 | |
| 3 | IO_L74N_3 | AA1 | |
| 3 | IO_L74P_3 | AB1 | |
| 3 | IO_L73N_3 | AA5 | |
| 3 | IO_L73P_3 | AB5 | |
| 3 | IO_L72N_3 | AA9 | |
| 3 | IO_L72P_3 | Y9 | |
| 3 | IO_L71N_3 | AA2 | |
| 3 | IO_L71P_3 | AB2 | |
| 3 | IO_L70N_3 | AB6 | |
| 3 | IO_L70P_3 | AC6 | |
| 3 | IO_L69N_3/VREF_3 | AD1 | |
| 3 | IO_L69P_3 | AC1 | |
| 3 | IO_L68N_3 | AC3 | |
| 3 | IO_L68P_3 | AD3 | |
| 3 | IO_L67N_3 | AC4 | |
| 3 | IO_L67P_3 | AD4 | |
| 3 | IO_L54N_3 | AB7 | |
| 3 | IO_L54P_3 | AC7 | |
| 3 | IO_L53N_3 | AC2 | |

*Table 12:* **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

| Bank | Pin Description | Pin Number | No Connect in the XC2V3000 |
|---|---|---|---|
| 4 | IO_L67N_4 | AN12 | |
| 4 | IO_L67P_4 | AN11 | |
| 4 | IO_L68N_4 | AE14 | |
| 4 | IO_L68P_4 | AE15 | |
| 4 | IO_L69N_4 | AJ13 | |
| 4 | IO_L69P_4/VREF_4 | AJ14 | |
| 4 | IO_L70N_4 | AL13 | |
| 4 | IO_L70P_4 | AL12 | |
| 4 | IO_L71N_4 | AF14 | |
| 4 | IO_L71P_4 | AF15 | |
| 4 | IO_L72N_4 | AM13 | |
| 4 | IO_L72P_4 | AM12 | |
| 4 | IO_L73N_4 | AP12 | |
| 4 | IO_L73P_4 | AP11 | |
| 4 | IO_L74N_4 | AG15 | |
| 4 | IO_L74P_4 | AG16 | |
| 4 | IO_L75N_4 | AN14 | |
| 4 | IO_L75P_4/VREF_4 | AN13 | |
| 4 | IO_L76N_4 | AP14 | |
| 4 | IO_L76P_4 | AP13 | |
| 4 | IO_L77N_4 | AD16 | |
| 4 | IO_L77P_4 | AD17 | |
| 4 | IO_L78N_4 | AK14 | |
| 4 | IO_L78P_4 | AK13 | |
| 4 | IO_L79N_4 | AN16 | NC |
| 4 | IO_L79P_4 | AP15 | NC |
| 4 | IO_L80N_4 | AE16 | NC |
| 4 | IO_L80P_4 | AE17 | NC |
| 4 | IO_L81N_4 | AH15 | NC |
| 4 | IO_L81P_4/VREF_4 | AJ15 | NC |
| 4 | IO_L82N_4 | AP17 | NC |
| 4 | IO_L82P_4 | AN17 | NC |
| 4 | IO_L83N_4 | AH17 | NC |
| 4 | IO_L83P_4 | AH16 | NC |
| 4 | IO_L84N_4 | AL15 | NC |
| 4 | IO_L84P_4 | AL14 | NC |

*Table 12:* **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

| Bank | Pin Description | Pin Number | No Connect in the XC2V3000 |
|---|---|---|---|
| NA | GND | V19 | |
| NA | GND | V18 | |
| NA | GND | V17 | |
| NA | GND | V16 | |
| NA | GND | V15 | |
| NA | GND | V14 | |
| NA | GND | U21 | |
| NA | GND | U20 | |
| NA | GND | U19 | |
| NA | GND | U18 | |
| NA | GND | U17 | |
| NA | GND | U16 | |
| NA | GND | U15 | |
| NA | GND | U14 | |
| NA | GND | T26 | |
| NA | GND | T21 | |
| NA | GND | T20 | |
| NA | GND | T19 | |
| NA | GND | T18 | |
| NA | GND | T17 | |
| NA | GND | T16 | |
| NA | GND | T15 | |
| NA | GND | T14 | |
| NA | GND | T9 | |
| NA | GND | R33 | |
| NA | GND | R21 | |
| NA | GND | R20 | |
| NA | GND | R19 | |
| NA | GND | R18 | |
| NA | GND | R17 | |
| NA | GND | R16 | |
| NA | GND | R15 | |
| NA | GND | R14 | |
| NA | GND | R2 | |
| NA | GND | P28 | |
| NA | GND | P21 | |

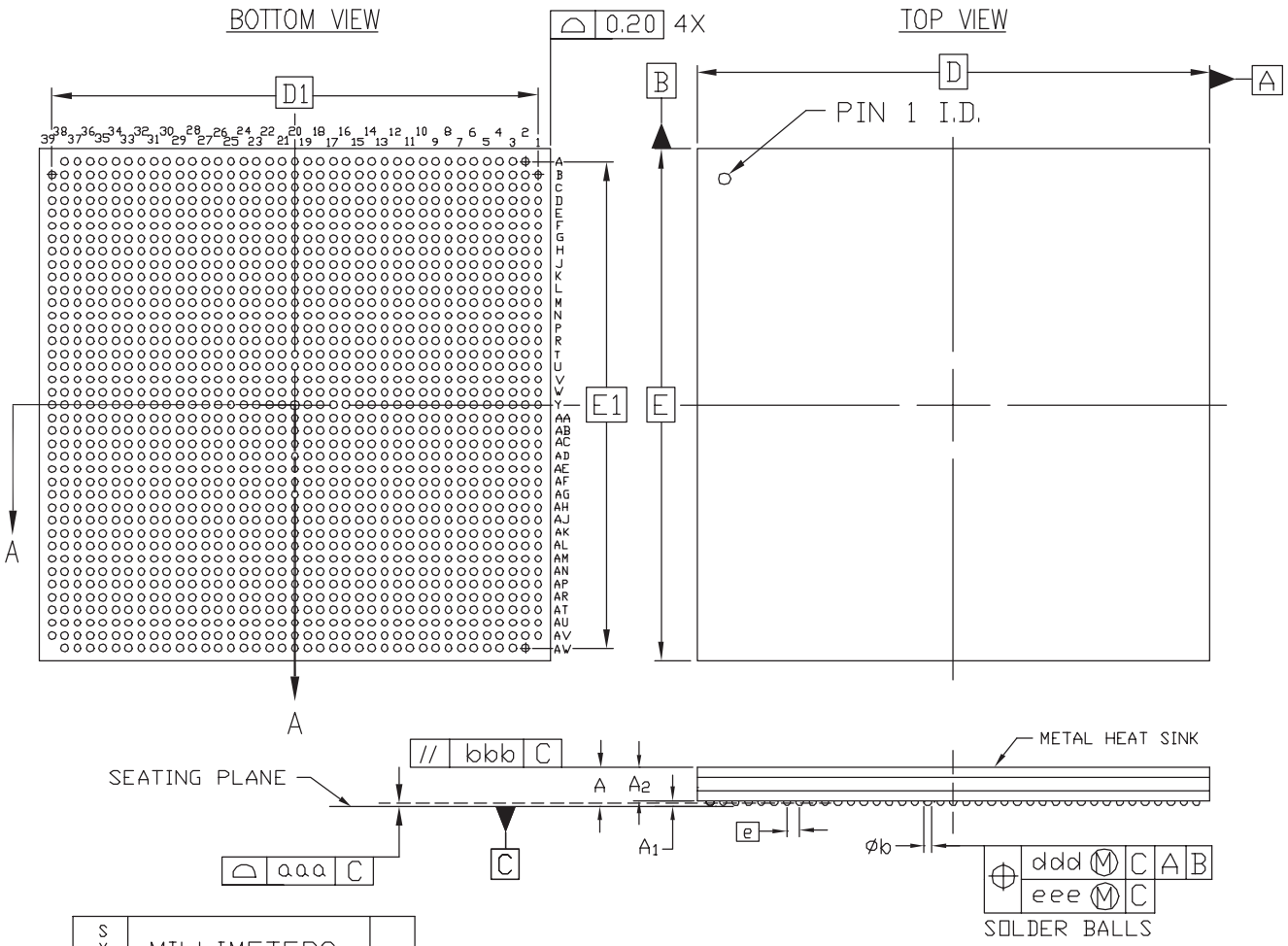
*Table 13:* **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

| Bank | Pin Description | Pin Number | No Connect in the XC2V4000 | No Connect in the XC2V6000 |
|---|---|---|---|---|
| 1 | IO_L69N_1/VREF_1 | E15 | | |
| 1 | IO_L69P_1 | E16 | | |
| 1 | IO_L68N_1 | K17 | | |
| 1 | IO_L68P_1 | K16 | | |
| 1 | IO_L67N_1 | C15 | | |
| 1 | IO_L67P_1 | B15 | | |
| 1 | IO_L60N_1 | F15 | | |
| 1 | IO_L60P_1 | F16 | | |
| 1 | IO_L59N_1 | H16 | | |
| 1 | IO_L59P_1 | H15 | | |
| 1 | IO_L58N_1 | C13 | | |
| 1 | IO_L58P_1 | C14 | | |
| 1 | IO_L57N_1/VREF_1 | D13 | | |
| 1 | IO_L57P_1 | D14 | | |
| 1 | IO_L56N_1 | M17 | | |
| 1 | IO_L56P_1 | M16 | | |
| 1 | IO_L55N_1 | A12 | | |
| 1 | IO_L55P_1 | A13 | | |
| 1 | IO_L54N_1 | B12 | | |
| 1 | IO_L54P_1 | B13 | | |
| 1 | IO_L53N_1 | G15 | | |
| 1 | IO_L53P_1 | G14 | | |
| 1 | IO_L52N_1 | C11 | | |
| 1 | IO_L52P_1 | C12 | | |
| 1 | IO_L51N_1/VREF_1 | F13 | | |
| 1 | IO_L51P_1 | F14 | | |
| 1 | IO_L50N_1 | L16 | | |
| 1 | IO_L50P_1 | L15 | | |
| 1 | IO_L49N_1 | A10 | | |
| 1 | IO_L49P_1 | A11 | | |
| 1 | IO_L36N_1 | E12 | NC | |
| 1 | IO_L36P_1 | E13 | NC | |
| 1 | IO_L35N_1 | K15 | NC | |
| 1 | IO_L35P_1 | J14 | NC | |
| 1 | IO_L34N_1 | B9 | NC | |
| 1 | IO_L34P_1 | B10 | NC | |

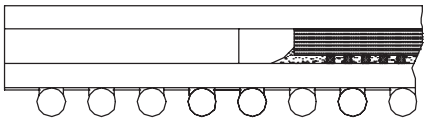
*Table 13:* **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

| Bank | Pin Description | Pin Number | No Connect in the XC2V4000 | No Connect in the XC2V6000 |
|---|---|---|---|---|
| 5 | IO_L01N_5/RDWR_B | AU36 | | |
| 5 | IO_L01P_5/CS_B | AV36 | | |
| | | | | |
| 6 | IO_L01P_6 | AJ27 | | |
| 6 | IO_L01N_6 | AH27 | | |
| 6 | IO_L02P_6/VRN_6 | AT38 | | |
| 6 | IO_L02N_6/VRP_6 | AR37 | | |
| 6 | IO_L03P_6 | AP36 | | |
| 6 | IO_L03N_6/VREF_6 | AR36 | | |
| 6 | IO_L04P_6 | AJ28 | | |
| 6 | IO_L04N_6 | AH29 | | |
| 6 | IO_L05P_6 | AT39 | | |
| 6 | IO_L05N_6 | AR39 | | |
| 6 | IO_L06P_6 | AN34 | | |
| 6 | IO_L06N_6 | AP35 | | |
| 6 | IO_L07P_6 | AH28 | NC | |
| 6 | IO_L07N_6 | AG28 | NC | |
| 6 | IO_L08P_6 | AR38 | NC | |
| 6 | IO_L08N_6 | AP38 | NC | |
| 6 | IO_L09P_6 | AM34 | NC | |
| 6 | IO_L09N_6/VREF_6 | AM33 | NC | |
| 6 | IO_L10P_6 | AL32 | NC | |
| 6 | IO_L10N_6 | AK32 | NC | |
| 6 | IO_L11P_6 | AP37 | NC | |
| 6 | IO_L11N_6 | AN37 | NC | |
| 6 | IO_L12P_6 | AM35 | NC | |
| 6 | IO_L12N_6 | AN35 | NC | |
| 6 | IO_L19P_6 | AK31 | | |
| 6 | IO_L19N_6 | AJ30 | | |
| 6 | IO_L20P_6 | AP39 | | |
| 6 | IO_L20N_6 | AN39 | | |
| 6 | IO_L21P_6 | AK33 | | |
| 6 | IO_L21N_6/VREF_6 | AL33 | | |
| 6 | IO_L22P_6 | AJ31 | | |
| 6 | IO_L22N_6 | AH31 | | |
| 6 | IO_L23P_6 | AN38 | | |

## FF1517 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)




| SYMBOL | MILLIMETERS | | | NOTE |
|---|---|---|---|---|
| | MIN. | NOM. | MAX. | |
| A | | 3.20 | 3.40 | |
| $A_1$ | 0.40 | 0.50 | 0.60 | |
| $A_2$ | | | 2.80 | |
| D/E | 40.00 BASIC | | | |
| $D_1/E_1$ | 38.00 REF | | | |
| e | 1.00 BASIC | | | |
| øb | 0.50 | 0.60 | 0.70 | |
| aaa | | | 0.20 | |
| bbb | | | 0.25 | |
| ddd | | | 0.25 | |
| eee | | | 0.10 | |
| M | | 39 | | 2 |



SECTION A–A
(NOT TO SCALE)

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAU–1 (DEPOPULATED)

*Figure 9:* **FF1517 Flip-Chip Fine-Pitch BGA Package Specifications**