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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	768
Number of Logic Elements/Cells	-
Total RAM Bits	589824
Number of I/O	172
Number of Gates	500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v500-5fgg256i

Table 4: **LVTTL and LVCMOS Programmable Currents (Sink and Source)**

SelectI/O-Ultra	Programmable Current (Worst-Case Guaranteed Minimum)						
LVTTL	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA
LVCMOS33	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA
LVCMOS25	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA
LVCMOS18	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	n/a
LVCMOS15	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	n/a

Figure 6 shows the SSTL2, SSTL3, and HSTL configurations. HSTL can sink current up to 48 mA. (HSTL IV)

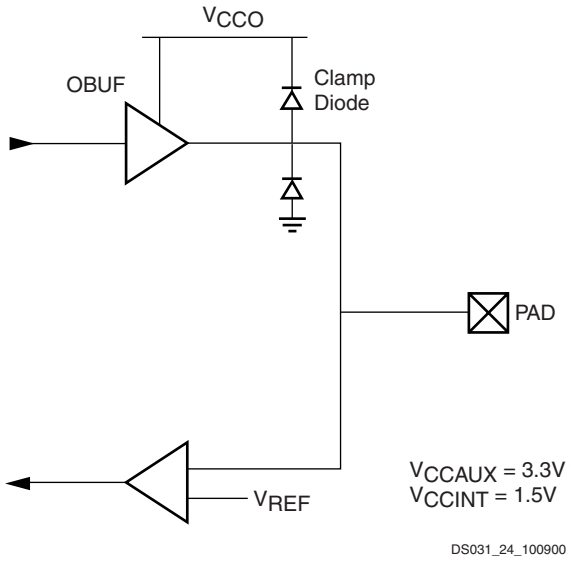


Figure 6: **SSTL or HSTL SelectI/O-Ultra Standards**

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. Virtex-II uses two memory cells to control the configuration of an I/O as an input. This is to reduce the probability of an I/O configured as an input from flipping to an output when subjected to a single event upset (SEU) in space applications.

Prior to configuration, all outputs not involved in configuration are forced into their high-impedance state. The pull-down resistors and the weak-keeper circuits are inactive. The dedicated pin HSWAP_EN controls the pull-up resistors prior to configuration. By default, HSWAP_EN is set high, which disables the pull-up resistors on user I/O pins. When HSWAP_EN is set low, the pull-up resistors are activated on user I/O pins.

All Virtex-II IOBs support IEEE 1149.1 compatible Boundary-Scan testing.

Input Path

The Virtex-II IOB input path routes input signals directly to internal logic and / or through an optional input flip-flop or latch, or through the DDR input registers. An optional delay element at the D-input of the storage element eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the Virtex-II device, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signaling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, V_{REF}. The need to supply V_{REF} imposes constraints on which standards can be used in the same bank. See I/O banking description.

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output and / or the 3-state signal can be routed to the buffer directly from the internal logic or through an output / 3-state flip-flop or latch, or through the DDR output / 3-state registers.

Each output driver can be individually programmed for a wide range of low-voltage signaling standards. In most signaling standards, the output High voltage depends on an externally supplied V_{CCO} voltage. The need to supply V_{CCO} imposes constraints on which standards can be used in the same bank. See I/O banking description.

I/O Banking

Some of the I/O standards described above require V_{CCO} and V_{REF} voltages. These voltages are externally supplied and connected to device pins that serve groups of IOB blocks, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from dividing each edge of the FPGA into two banks, as shown in Figure 7 and Figure 8. Each bank has multiple V_{CCO} pins, all of which must be connected to the same voltage. This voltage is determined by the output standards in use.

Routing

DCM Locations/Organization

Virtex-II DCMs are placed on the top and bottom of each block RAM and multiplier column. The number of DCMs depends on the device size, as shown in Table 24.

Table 24: **DCM Organization**

Device	Columns	DCMs
XC2V40	2	4
XC2V80	2	4
XC2V250	4	8
XC2V500	4	8
XC2V1000	4	8
XC2V1500	4	8
XC2V2000	4	8
XC2V3000	6	12
XC2V4000	6	12
XC2V6000	6	12
XC2V8000	6	12

Active Interconnect Technology

Local and global Virtex-II routing resources are optimized for speed and timing predictability, as well as to facilitate IP cores implementation. Virtex-II Active Interconnect Technology is a fully buffered programmable routing matrix. All routing resources are segmented to offer the advantages of a hierarchical solution. Virtex-II logic features like CLBs, IOBs, block RAM, multipliers, and DCMs are all connected to an identical switch matrix for access to global routing resources, as shown in Figure 47.

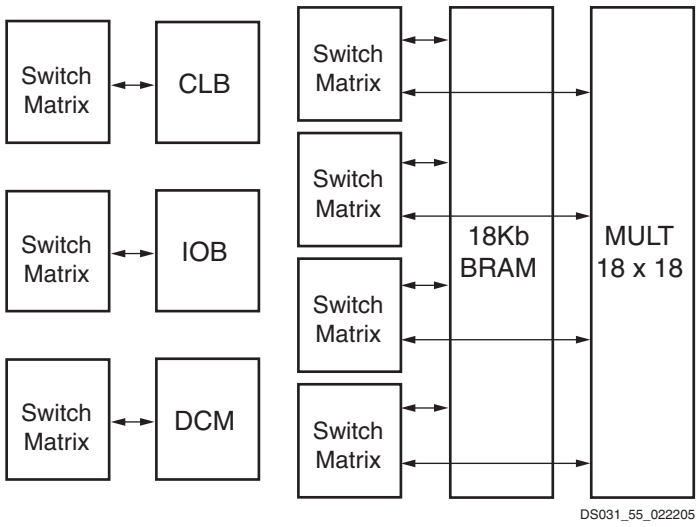


Figure 47: **Active Interconnect Technology**

Each Virtex-II device can be represented as an array of switch matrixes with logic blocks attached, as illustrated in Figure 48.

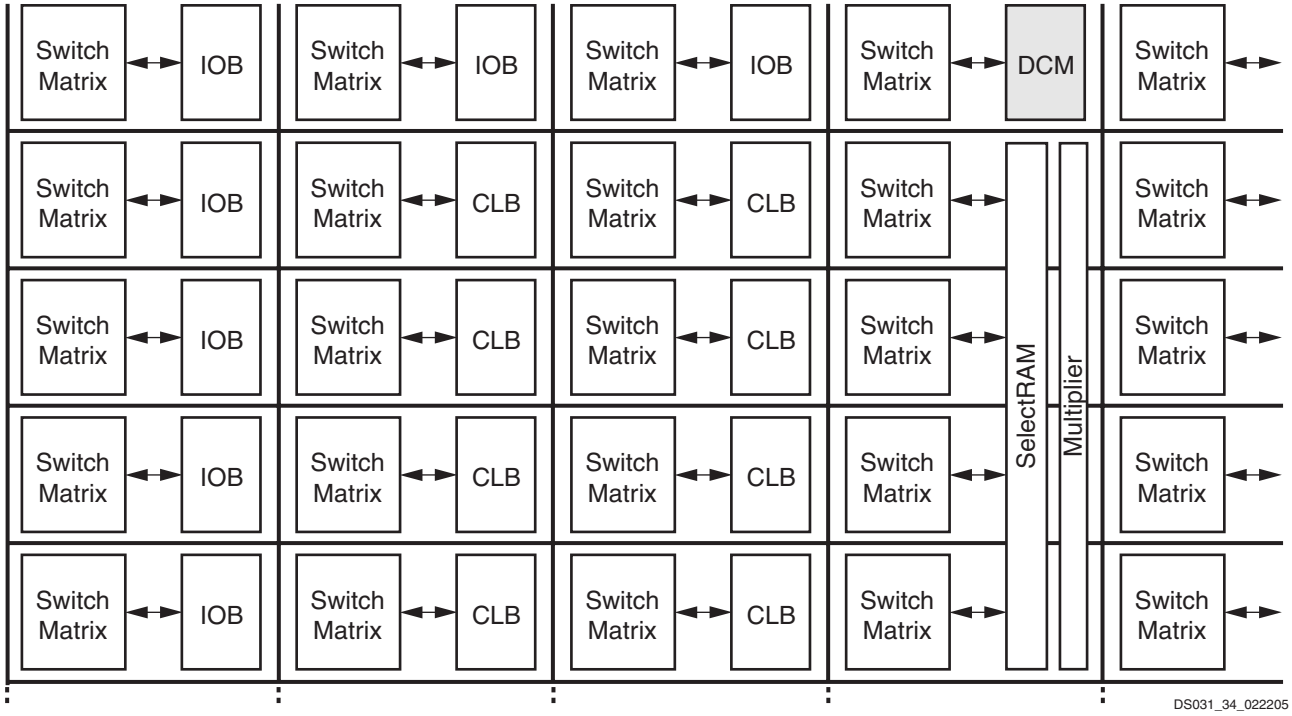


Figure 48: **Routing Resources**

Virtex-II FPGA device. Timing is similar to the Slave Serial-MAP mode except that CCLK is supplied by the Virtex-II FPGA.

Boundary-Scan (JTAG, IEEE 1532) Mode

In Boundary-Scan mode, dedicated pins are used for configuring the Virtex-II device. The configuration is done entirely through the IEEE 1149.1 Test Access Port (TAP). Virtex-II device configuration using Boundary-Scan is compatible with the IEEE 1149.1-1993 standard and the new IEEE 1532 standard for In-System Configurable (ISC) devices. The IEEE 1532 standard is backward compliant with the IEEE 1149.1-1993 TAP and state machine. The IEEE Standard 1532 for In-System Configurable (ISC) devices is intended to be programmed, reprogrammed, or tested on the board via a physical and logical protocol.

Configuration through the Boundary-Scan port is always available, independent of the mode selection. Selecting the Boundary-Scan mode simply turns off the other modes.

Table 25: **Virtex-II Configuration Mode Pin Settings**

Configuration Mode(1)	M2	M1	M0	CCLK Direction	Data Width	Serial D_{OUT}(2)
Master Serial	0	0	0	Out	1	Yes
Slave Serial	1	1	1	In	1	Yes
Master SelectMAP	0	1	1	Out	8	No
Slave SelectMAP	1	1	0	In	8	No
Boundary-Scan	1	0	1	N/A	1	No

Notes:
1. The HSWAP_EN pin controls the pull-ups. Setting M2, M1, and M0 selects the configuration mode, while the HSWAP_EN pin controls whether or not the pull-ups are used.
2. Daisy chaining is possible only in modes where Serial D_{OUT} is used. For example, in SelectMAP modes, the first device does NOT support daisy chaining of downstream devices.

Table 26 lists the total number of bits required to configure each device.

Table 26: **Virtex-II Bitstream Lengths**

Device	# of Configuration Bits
XC2V40	338,976
XC2V80	598,816
XC2V250	1,593,632
XC2V500	2,560,544
XC2V1000	4,082,592
XC2V1500	5,170,208
XC2V2000	6,812,960
XC2V3000	10,494,368
XC2V4000	15,659,936
XC2V6000	21,849,504
XC2V8000	26,194,208

Configuration Sequence

The configuration of Virtex-II devices is a three-phase process after Power On Reset or POR. POR occurs when V_{CCINT} is greater than 1.2V, V_{CCAUX} is greater than 2.5V, and V_{CCO} (bank 4) is greater than 1.5V. Once the POR voltages have been reached, the three-phase process begins.

First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process.

Configuration is automatically initiated on power-up unless it is delayed by the user. The INIT_B pin can be held Low using an open-drain driver. An open-drain is required since INIT_B is a bidirectional open-drain pin that is held Low by a Virtex-II FPGA device while the configuration memory is being cleared. Extending the time that the pin is Low causes the configuration sequencer to wait. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

The configuration process can also be initiated by asserting the PROG_B pin. The end of the memory-clearing phase is signaled by the INIT_B pin going High, and the completion of the entire process is signaled by the DONE pin going High. The Global Set/Reset (GSR) signal is pulsed after the last frame of configuration data is written but before the start-up sequence. The GSR signal resets all flip-flops on the device.

The default start-up sequence is that one CCLK cycle after DONE goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary. One CCLK cycle later, the Global Write Enable (GWE) signal is released. This permits the internal storage ele-

Notice of Disclaimer

Virtex-II Data Sheet

The Virtex-II Data Sheet contains the following modules:

- Virtex-II Platform FPGAs: Introduction and Overview (Module 1)
- Virtex-II Platform FPGAs: Functional Description (Module 2)
- Virtex-II Platform FPGAs: DC and Switching Characteristics (Module 3)
- Virtex-II Platform FPGAs: Pinout Information (Module 4)

IOB Output Switching Characteristics Standard Adjustments

Table 17 gives all standard-specific adjustments for output delays terminating at pads, based on standard capacitive load, C_{REF}. Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

Table 17: **IOB Output Switching Characteristics Standard Adjustments**

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-6	-5	-4	
LVTTL (Low-Voltage Transistor-Transistor Logic), Slow, 2 mA	LVTTL_S2	T_{OLVTTL_S2}	9.42	9.71	10.68	ns
LVTTL, Slow, 4 mA	LVTTL_S4	T_{OLVTTL_S4}	5.77	5.95	6.55	ns
LVTTL, Slow, 6 mA	LVTTL_S6	T_{OLVTTL_S6}	4.11	4.24	4.66	ns
LVTTL, Slow, 8 mA	LVTTL_S8	T_{OLVTTL_S8}	2.87	2.96	3.26	ns
LVTTL, Slow, 12 mA	LVTTL_S12	T_{OLVTTL_S12}	2.32	2.39	2.63	ns
LVTTL, Slow, 16 mA	LVTTL_S16	T_{OLVTTL_S16}	1.70	1.75	1.93	ns
LVTTL, Slow, 24 mA	LVTTL_S24	T_{OLVTTL_S24}	1.26	1.30	1.43	ns
LVTTL, Fast, 2 mA	LVTTL_F2	T_{OLVTTL_F2}	6.52	6.72	7.39	ns
LVTTL, Fast, 4 mA	LVTTL_F4	T_{OLVTTL_F4}	2.80	2.88	3.17	ns
LVTTL, Fast, 6 mA	LVTTL_F6	T_{OLVTTL_F6}	1.57	1.62	1.78	ns
LVTTL, Fast, 8 mA	LVTTL_F8	T_{OLVTTL_F8}	0.46	0.48	0.52	ns
LVTTL, Fast, 12 mA	LVTTL_F12	T_{OLVTTL_F12}	0.00	0.00	0.00	ns
LVTTL, Fast, 16 mA	LVTTL_F16	T_{OLVTTL_F16}	–0.13	–0.14	–0.15	ns
LVTTL, Fast, 24 mA	LVTTL_F24	T_{OLVTTL_F24}	–0.22	–0.23	–0.26	ns
LVCMOS (Low-Voltage CMOS), 3.3V, Slow, 2 mA	LVCMOS33_S2	$T_{OLVCMOS33\_S2}$	7.67	7.91	8.70	ns
LVCMOS, 3.3V, Slow, 4 mA	LVCMOS33_S4	$T_{OLVCMOS33\_S4}$	4.37	4.50	4.95	ns
LVCMOS, 3.3V, Slow, 6 mA	LVCMOS33_S6	$T_{OLVCMOS33\_S6}$	3.34	3.44	3.78	ns
LVCMOS, 3.3V, Slow, 8 mA	LVCMOS33_S8	$T_{OLVCMOS33\_S8}$	2.29	2.36	2.60	ns
LVCMOS, 3.3V, Slow, 12 mA	LVCMOS33_S12	$T_{OLVCMOS33\_S12}$	1.91	1.97	2.16	ns
LVCMOS, 3.3V, Slow, 16 mA	LVCMOS33_S16	$T_{OLVCMOS33\_S16}$	1.24	1.27	1.40	ns
LVCMOS, 3.3V, Slow, 24 mA	LVCMOS33_S24	$T_{OLVCMOS33\_S24}$	1.18	1.22	1.34	ns
LVCMOS, 3.3V, Fast, 2 mA	LVCMOS33_F2	$T_{OLVCMOS33\_F2}$	5.82	6.00	6.60	ns
LVCMOS, 3.3V, Fast, 4 mA	LVCMOS33_F4	$T_{OLVCMOS33\_F4}$	2.48	2.55	2.81	ns
LVCMOS, 3.3V, Fast, 6 mA	LVCMOS33_F6	$T_{OLVCMOS33\_F6}$	1.28	1.31	1.45	ns
LVCMOS, 3.3V, Fast, 8 mA	LVCMOS33_F8	$T_{OLVCMOS33\_F8}$	0.48	0.49	0.54	ns
LVCMOS, 3.3V, Fast, 12 mA	LVCMOS33_F12	$T_{OLVCMOS33\_F12}$	0.27	0.28	0.31	ns
LVCMOS, 3.3V, Fast, 16 mA	LVCMOS33_F16	$T_{OLVCMOS33\_F16}$	–0.14	–0.14	–0.15	ns
LVCMOS, 3.3V, Fast, 24 mA	LVCMOS33_F24	$T_{OLVCMOS33\_F24}$	–0.21	–0.21	–0.23	ns
LVCMOS, 2.5V, Slow, 2 mA	LVCMOS25_S2	$T_{OLVCMOS25\_S2}$	9.11	9.39	10.33	ns
LVCMOS, 2.5V, Slow, 4 mA	LVCMOS25_S4	$T_{OLVCMOS25\_S4}$	5.00	5.16	5.67	ns
LVCMOS, 2.5V, Slow, 6 mA	LVCMOS25_S6	$T_{OLVCMOS25\_S6}$	4.53	4.67	5.13	ns
LVCMOS, 2.5V, Slow, 8 mA	LVCMOS25_S8	$T_{OLVCMOS25\_S8}$	3.86	3.98	4.38	ns
LVCMOS, 2.5V, Slow, 12 mA	LVCMOS25_S12	$T_{OLVCMOS25\_S12}$	2.84	2.93	3.22	ns
LVCMOS, 2.5V, Slow, 16 mA	LVCMOS25_S16	$T_{OLVCMOS25\_S16}$	2.36	2.43	2.67	ns
LVCMOS, 2.5V, Slow, 24 mA	LVCMOS25_S24	$T_{OLVCMOS25\_S24}$	2.00	2.06	2.27	ns
LVCMOS, 2.5V, Fast, 2 mA	LVCMOS25_F2	$T_{OLVCMOS25\_F2}$	4.06	4.18	4.60	ns
LVCMOS, 2.5V, Fast, 4 mA	LVCMOS25_F4	$T_{OLVCMOS25\_F4}$	1.15	1.18	1.30	ns
LVCMOS, 2.5V, Fast, 6 mA	LVCMOS25_F6	$T_{OLVCMOS25\_F6}$	0.72	0.74	0.81	ns
LVCMOS, 2.5V, Fast, 8 mA	LVCMOS25_F8	$T_{OLVCMOS25\_F8}$	0.33	0.34	0.37	ns
LVCMOS, 2.5V, Fast, 12 mA	LVCMOS25_F12	$T_{OLVCMOS25\_F12}$	0.02	0.02	0.03	ns

Clock Distribution Switching Characteristics

Table 20: **Clock Distribution Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Global Clock Buffer I input to O output	T_{GIO}	0.47	0.52	0.59	ns, Max
Global Clock Buffer S input Setup/Hold to I1 an I2 inputs	T_{GSI}/T_{GIS}	0.55/ 0	0.61/ 0	0.70/ 0	ns, Max

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used (see Figure 16 in Module 2). The values listed below are worst-case. Precise values are provided by the timing analyzer.

Table 21: **CLB Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Combinatorial Delays					
4-input function: F/G inputs to X/Y outputs	T_{ILO}	0.35	0.39	0.44	ns, Max
5-input function: F/G inputs to F5 output	T_{IF5}	0.57	0.63	0.72	ns, Max
5-input function: F/G inputs to X output	T_{IF5X}	0.76	0.83	0.95	ns, Max
FXINA or FXINB inputs to Y output via MUXFX	T_{IFXY}	0.36	0.39	0.45	ns, Max
FXINA input to FX output via MUXFX	T_{INAFX}	0.26	0.28	0.32	ns, Max
FXINB input to FX output via MUXFX	T_{INBFX}	0.26	0.28	0.32	ns, Max
SOPIN input to SOPOUT output via ORCY	T_{SOPSOP}	0.35	0.38	0.44	ns, Max
Incremental delay routing through transparent latch to XQ/YQ outputs	T_{IFNCTL}	0.41	0.45	0.51	ns, Max
Sequential Delays					
FF Clock CLK to XQ/YQ outputs	T_{CKO}	0.45	0.50	0.57	ns, Max
Latch Clock CLK to XQ/YQ outputs	T_{CKLO}	0.54	0.59	0.68	ns, Max
Setup and Hold Times Before/After Clock CLK					
BX/BY inputs	T_{DICK}/T_{CKDI}	0.30/–0.07	0.33/–0.08	0.37/–0.09	ns, Min
DY inputs	T_{DYCK}/T_{CKDY}	0.30/–0.07	0.33/–0.08	0.37/–0.09	ns, Min
DX inputs	T_{DXCK}/T_{CKDX}	0.30/–0.07	0.33/–0.08	0.37/–0.09	ns, Min
CE input	T_{CECK}/T_{CKCE}	0.19/–0.06	0.21/–0.07	0.24/–0.08	ns, Min
SR/BY inputs (synchronous)	T_{SRCK}/T_{SCKR}	0.21/–0.02	0.23/–0.03	0.26/–0.03	ns, Min
Clock CLK					
Minimum Pulse Width, High	T_{CH}	0.61	0.67	0.77	ns, Min
Minimum Pulse Width, Low	T_{CL}	0.61	0.67	0.77	ns, Min
Set/Reset					
Minimum Pulse Width, SR/BY inputs (asynchronous)	T_{RPW}	0.61	0.67	0.77	ns, Min
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	T_{RQ}	1.06	1.17	1.34	ns, Max
Toggle Frequency (MHz) (for export control)	F_{TOG}	820	750	650	MHz

FG256/FGG256 Fine-Pitch BGA Package

As shown in Table 6, XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000 Virtex-II devices are available in the FG256/FGG256 fine-pitch BGA package. The pins in the XC2V250, XC2V500, and XC2V1000 devices are same. The No Connect columns show pin differences for the XC2V40 and XC2V80 devices. Following this table are the FG256/FGG256 Fine-Pitch BGA Package Specifications (1.00mm pitch).

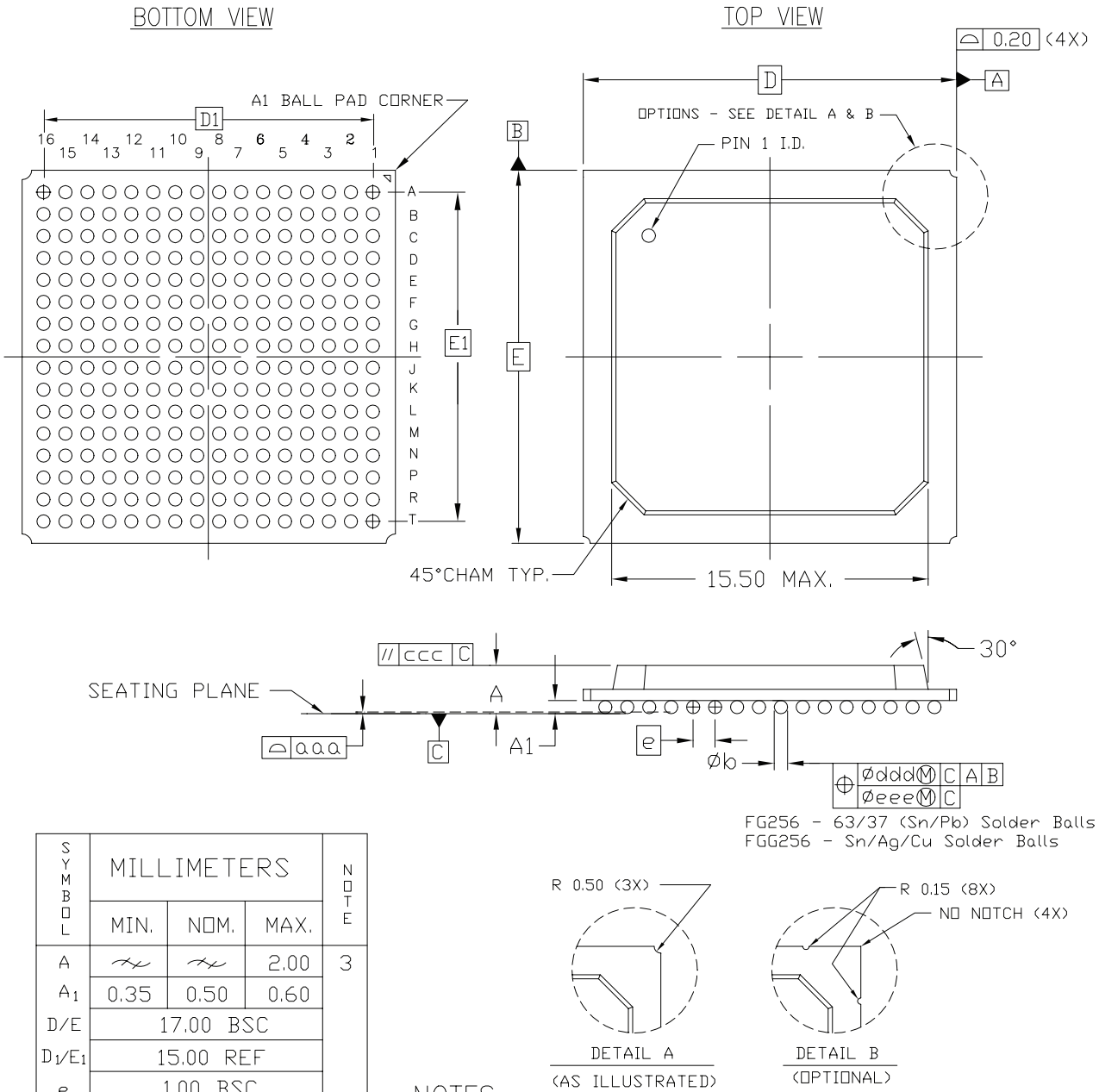
Table 6: **FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
0	IO_L01N_0	C4		
0	IO_L01P_0	B4		
0	IO_L02N_0	D5		
0	IO_L02P_0	C5		
0	IO_L03N_0/VRP_0	B5		
0	IO_L03P_0/VRN_0	A5		
0	IO_L04N_0/VREF_0	D6	NC	NC
0	IO_L04P_0	C6	NC	NC
0	IO_L05N_0	B6	NC	NC
0	IO_L05P_0	A6	NC	NC
0	IO_L92N_0	E6	NC	NC
0	IO_L92P_0	E7	NC	NC
0	IO_L93N_0	D7	NC	NC
0	IO_L93P_0	C7	NC	NC
0	IO_L94N_0/VREF_0	B7		
0	IO_L94P_0	A7		
0	IO_L95N_0/GCLK7P	D8		
0	IO_L95P_0/GCLK6S	C8		
0	IO_L96N_0/GCLK5P	B8		
0	IO_L96P_0/GCLK4S	A8		
1	IO_L96N_1/GCLK3P	A9		
1	IO_L96P_1/GCLK2S	B9		
1	IO_L95N_1/GCLK1P	C9		
1	IO_L95P_1/GCLK0S	D9		
1	IO_L94N_1	A10		
1	IO_L94P_1/VREF_1	B10		
1	IO_L93N_1	C10	NC	NC
1	IO_L93P_1	D10	NC	NC
1	IO_L92N_1	E10	NC	NC

Table 6: **FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
1	IO_L92P_1	E11	NC	NC
1	IO_L05N_1	A11	NC	NC
1	IO_L05P_1	B11	NC	NC
1	IO_L04N_1	C11	NC	NC
1	IO_L04P_1/VREF_1	D11	NC	NC
1	IO_L03N_1/VRP_1	A12		
1	IO_L03P_1/VRN_1	B12		
1	IO_L02N_1	C12		
1	IO_L02P_1	D12		
1	IO_L01N_1	B13		
1	IO_L01P_1	C13		
2	IO_L01N_2	C16		
2	IO_L01P_2	D16		
2	IO_L02N_2/VRP_2	D14		
2	IO_L02P_2/VRN_2	D15		
2	IO_L03N_2	E13		
2	IO_L03P_2/VREF_2	E14		
2	IO_L04N_2	E15	NC	
2	IO_L04P_2	E16	NC	
2	IO_L06N_2	F13	NC	
2	IO_L06P_2	F14	NC	
2	IO_L43N_2	F15	NC	NC
2	IO_L43P_2	F16	NC	NC
2	IO_L45N_2	F12	NC	NC
2	IO_L45P_2/VREF_2	G12	NC	NC
2	IO_L91N_2	G13	NC	
2	IO_L91P_2	G14	NC	
2	IO_L93N_2	G15	NC	
2	IO_L93P_2/VREF_2	G16	NC	
2	IO_L94N_2	H13		
2	IO_L94P_2	H14		
2	IO_L96N_2	H15		
2	IO_L96P_2	H16		

FG256/FGG256 Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A			2.00	3
A_1	0.35	0.50	0.60	
D/E	17.00 BSC			
D_1/E_1	15.00 REF			
e	1.00 BSC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.35	
ddd			0.30	
eee			0.10	
M	16			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994.
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. NOMINAL DIMENSION IS TYPICALLY 1.60-1.73mm
4. CONFORMS TO JEDEC MS-034-AAF-1

256-BALL FINE PITCH BGA (FG256/FGG256)

Figure 2: **FG256/FGG256 Fine-Pitch BGA Package Specifications**

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
4	IO_L95N_4/GCLK3S	W12		
4	IO_L95P_4/GCLK2P	Y12		
4	IO_L96N_4/GCLK1S	AA12		
4	IO_L96P_4/GCLK0P	AB12		
5	IO_L96N_5/GCLK7S	AA11		
5	IO_L96P_5/GCLK6P	Y11		
5	IO_L95N_5/GCLK5S	W11		
5	IO_L95P_5/GCLK4P	V11		
5	IO_L94N_5	U11		
5	IO_L94P_5/VREF_5	U10		
5	IO_L93N_5	AB10		
5	IO_L93P_5	AA10		
5	IO_L92N_5	Y10		
5	IO_L92P_5	W10		
5	IO_L91N_5	V10		
5	IO_L91P_5/VREF_5	V9		
5	IO_L54N_5	AB9	NC	
5	IO_L54P_5	AA9	NC	
5	IO_L52N_5	Y9	NC	
5	IO_L52P_5	W9	NC	
5	IO_L51N_5/VREF_5	AB8	NC	
5	IO_L51P_5	AA8	NC	
5	IO_L49N_5	Y8	NC	
5	IO_L49P_5	W8	NC	
5	IO_L24N_5	U9	NC	NC
5	IO_L24P_5	V8	NC	NC
5	IO_L22N_5	AB7	NC	NC
5	IO_L22P_5	AA7	NC	NC
5	IO_L21N_5/VREF_5	Y7	NC	NC
5	IO_L21P_5	W7	NC	NC
5	IO_L19N_5	AB6	NC	NC
5	IO_L19P_5	AA6	NC	NC
5	IO_L06N_5	Y6		

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
5	IO_L06P_5	W6		
5	IO_L05N_5/VRP_5	V7		
5	IO_L05P_5/VRN_5	V6		
5	IO_L04N_5	AB5		
5	IO_L04P_5/VREF_5	AA5		
5	IO_L03N_5/D4/ALT_VRP_5	Y5		
5	IO_L03P_5/D5/ALT_VRN_5	W5		
5	IO_L02N_5/D6	AB4		
5	IO_L02P_5/D7	AA4		
5	IO_L01N_5/RDWR_B	Y4		
5	IO_L01P_5/CS_B	AA3		
6	IO_L01P_6	V5		
6	IO_L01N_6	U5		
6	IO_L02P_6/VRN_6	Y2		
6	IO_L02N_6/VRP_6	Y1		
6	IO_L03P_6	V4		
6	IO_L03N_6/VREF_6	V3		
6	IO_L04P_6	W2		
6	IO_L04N_6	W1		
6	IO_L06P_6	U4		
6	IO_L06N_6	U3		
6	IO_L19P_6	V2	NC	NC
6	IO_L19N_6	V1	NC	NC
6	IO_L21P_6	U2	NC	NC
6	IO_L21N_6/VREF_6	U1	NC	NC
6	IO_L22P_6	T5	NC	NC
6	IO_L22N_6	R5	NC	NC
6	IO_L24P_6	T4	NC	NC
6	IO_L24N_6	T3	NC	NC
6	IO_L43P_6	T2		
6	IO_L43N_6	T1		
6	IO_L45P_6	R4		
6	IO_L45N_6/VREF_6	R3		

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
5	IO_L02P_5/D7	AC6		
5	IO_L01N_5/RDWR_B	AB6		
5	IO_L01P_5/CS_B	AC5		
6	IO_L01P_6	AF2		
6	IO_L01N_6	AE1		
6	IO_L02P_6/VRN_6	AB4		
6	IO_L02N_6/VRP_6	AB3		
6	IO_L03P_6	AD2		
6	IO_L03N_6/VREF_6	AD1		
6	IO_L04P_6	AC2		
6	IO_L04N_6	AC1		
6	IO_L06P_6	AB2		
6	IO_L06N_6	AB1		
6	IO_L19P_6	AA4		
6	IO_L19N_6	AA3		
6	IO_L21P_6	Y6		
6	IO_L21N_6/VREF_6	Y5		
6	IO_L22P_6	W6		
6	IO_L22N_6	W7		
6	IO_L24P_6	AA2		
6	IO_L24N_6	AA1		
6	IO_L25P_6	Y4	NC	NC
6	IO_L25N_6	Y3	NC	NC
6	IO_L43P_6	W5		
6	IO_L43N_6	W4		
6	IO_L45P_6	W2		
6	IO_L45N_6/VREF_6	W3		
6	IO_L46P_6	Y1		
6	IO_L46N_6	W1		
6	IO_L48P_6	V6		
6	IO_L48N_6	V7		
6	IO_L49P_6	V5		
6	IO_L49N_6	V4		
6	IO_L51P_6	V3		
6	IO_L51N_6/VREF_6	V2		
6	IO_L52P_6	V1		

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
NA	VCCAUX	P26
NA	VCCAUX	P2
NA	VCCAUX	C26
NA	VCCAUX	C2
NA	VCCAUX	B14
NA	VCCINT	V18
NA	VCCINT	V14
NA	VCCINT	V10
NA	VCCINT	U17
NA	VCCINT	U16
NA	VCCINT	U15
NA	VCCINT	U14
NA	VCCINT	U13
NA	VCCINT	U12
NA	VCCINT	U11
NA	VCCINT	T17
NA	VCCINT	T11
NA	VCCINT	R17
NA	VCCINT	R11
NA	VCCINT	P18
NA	VCCINT	P17
NA	VCCINT	P11
NA	VCCINT	P10
NA	VCCINT	N17
NA	VCCINT	N11
NA	VCCINT	M17
NA	VCCINT	M11
NA	VCCINT	L17
NA	VCCINT	L16
NA	VCCINT	L15
NA	VCCINT	L14
NA	VCCINT	L13
NA	VCCINT	L12
NA	VCCINT	L11
NA	VCCINT	K18
NA	VCCINT	K14

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
3	IO_L73P_3	W4	NC	NC
3	IO_L72N_3	W7	NC	
3	IO_L72P_3	V7	NC	
3	IO_L71N_3	V5	NC	
3	IO_L71P_3	W6	NC	
3	IO_L70N_3	W3	NC	
3	IO_L70P_3	Y3	NC	
3	IO_L69N_3/VREF_3	V8	NC	
3	IO_L69P_3	W8	NC	
3	IO_L68N_3	AA1	NC	
3	IO_L68P_3	AB1	NC	
3	IO_L67N_3	Y4	NC	
3	IO_L67P_3	AA4	NC	
3	IO_L54N_3	AA6		
3	IO_L54P_3	Y6		
3	IO_L53N_3	AA2		
3	IO_L53P_3	AB2		
3	IO_L52N_3	Y5		
3	IO_L52P_3	AA5		
3	IO_L51N_3/VREF_3	Y8		
3	IO_L51P_3	AA8		
3	IO_L50N_3	AC2		
3	IO_L50P_3	AD2		
3	IO_L49N_3	Y7		
3	IO_L49P_3	AA7		
3	IO_L48N_3	AC6		
3	IO_L48P_3	AB6		
3	IO_L47N_3	AD1		
3	IO_L47P_3	AE1		
3	IO_L46N_3	AB3		
3	IO_L46P_3	AC3		
3	IO_L45N_3/VREF_3	AB7		
3	IO_L45P_3	AC7		
3	IO_L44N_3	AB4		
3	IO_L44P_3	AC4		
3	IO_L43N_3	AB5		
3	IO_L43P_3	AC5		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
3	IO_L24N_3	AC8		
3	IO_L24P_3	AB8		
3	IO_L23N_3	AE2		
3	IO_L23P_3	AF3		
3	IO_L22N_3	AD3		
3	IO_L22P_3	AE3		
3	IO_L21N_3/VREF_3	AD6		
3	IO_L21P_3	AD7		
3	IO_L20N_3	AF1		
3	IO_L20P_3	AG1		
3	IO_L19N_3	AD4		
3	IO_L19P_3	AE4		
3	IO_L06N_3	AD8		
3	IO_L06P_3	AE7		
3	IO_L05N_3	AG2		
3	IO_L05P_3	AH2		
3	IO_L04N_3	AD5		
3	IO_L04P_3	AE5		
3	IO_L03N_3/VREF_3	AC9		
3	IO_L03P_3	AD9		
3	IO_L02N_3/VRP_3	AH1		
3	IO_L02P_3/VRN_3	AJ1		
3	IO_L01N_3	AF4		
3	IO_L01P_3	AG3		
4	IO_L01N_4/BUSY/DOUT(1)	AK2		
4	IO_L01P_4/INIT_B	AJ3		
4	IO_L02N_4/D0/DIN(1)	AE8		
4	IO_L02P_4/D1	AF9		
4	IO_L03N_4/D2/ALT_VRP_4	AH5		
4	IO_L03P_4/D3/ALT_VRN_4	AH6		
4	IO_L04N_4/VREF_4	AJ4		
4	IO_L04P_4	AK4		
4	IO_L05N_4/VRP_4	AC10		
4	IO_L05P_4/VRN_4	AC11		
4	IO_L06N_4	AH7		
4	IO_L06P_4	AG6		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
6	IO_L68N_6	Y26	NC	
6	IO_L69P_6	AA30	NC	
6	IO_L69N_6/VREF_6	Y30	NC	
6	IO_L70P_6	W24	NC	
6	IO_L70N_6	V24	NC	
6	IO_L71P_6	Y27	NC	
6	IO_L71N_6	W27	NC	
6	IO_L72P_6	W28	NC	
6	IO_L72N_6	Y28	NC	
6	IO_L73P_6	V25	NC	NC
6	IO_L73N_6	U25	NC	NC
6	IO_L74P_6	V26	NC	NC
6	IO_L74N_6	V27	NC	NC
6	IO_L75P_6	Y29	NC	NC
6	IO_L75N_6/VREF_6	W29	NC	NC
6	IO_L76P_6	U22	NC	NC
6	IO_L76N_6	T22	NC	NC
6	IO_L77P_6	U26	NC	NC
6	IO_L77N_6	T26	NC	NC
6	IO_L78P_6	V30	NC	NC
6	IO_L78N_6	W30	NC	NC
6	IO_L91P_6	U23		
6	IO_L91N_6	T23		
6	IO_L92P_6	U27		
6	IO_L92N_6	T27		
6	IO_L93P_6	V29		
6	IO_L93N_6/VREF_6	U29		
6	IO_L94P_6	T24		
6	IO_L94N_6	T25		
6	IO_L95P_6	U28		
6	IO_L95N_6	T28		
6	IO_L96P_6	T30		
6	IO_L96N_6	U30		
7	IO_L96P_7	P28		
7	IO_L96N_7	R28		
7	IO_L95P_7	R25		

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
3	IO_L23P_3	AJ3	
3	IO_L22N_3	AF7	
3	IO_L22P_3	AG7	
3	IO_L21N_3/VREF_3	AL1	
3	IO_L21P_3	AK1	
3	IO_L20N_3	AH2	
3	IO_L20P_3	AJ2	
3	IO_L19N_3	AJ4	
3	IO_L19P_3	AK4	
3	IO_L06N_3	AE10	
3	IO_L06P_3	AD10	
3	IO_L05N_3	AK2	
3	IO_L05P_3	AL2	
3	IO_L04N_3	AH6	
3	IO_L04P_3	AJ5	
3	IO_L03N_3/VREF_3	AE11	
3	IO_L03P_3	AF11	
3	IO_L02N_3/VRP_3	AK3	
3	IO_L02P_3/VRN_3	AL3	
3	IO_L01N_3	AF10	
3	IO_L01P_3	AG9	
4	IO_L01N_4/BUSY/DOUT(1)	AM4	
4	IO_L01P_4/INIT_B	AL5	
4	IO_L02N_4/D0/DIN(1)	AG10	
4	IO_L02P_4/D1	AH11	
4	IO_L03N_4/D2/ALT_VRP_4	AK7	
4	IO_L03P_4/D3/ALT_VRN_4	AK8	
4	IO_L04N_4/VREF_4	AL6	
4	IO_L04P_4	AM6	
4	IO_L05N_4/VRP_4	AK9	
4	IO_L05P_4/VRN_4	AJ8	
4	IO_L06N_4	AM8	
4	IO_L06P_4	AM7	
4	IO_L19N_4	AN3	
4	IO_L19P_4	AM2	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
2	VCCO_2	R11	
2	VCCO_2	R5	
2	VCCO_2	P12	
2	VCCO_2	P11	
2	VCCO_2	N12	
2	VCCO_2	N11	
2	VCCO_2	M11	
2	VCCO_2	K1	
2	VCCO_2	G4	
3	VCCO_3	AH4	
3	VCCO_3	AE1	
3	VCCO_3	AC11	
3	VCCO_3	AB12	
3	VCCO_3	AB11	
3	VCCO_3	AA12	
3	VCCO_3	AA11	
3	VCCO_3	Y12	
3	VCCO_3	Y11	
3	VCCO_3	Y5	
3	VCCO_3	W12	
3	VCCO_3	W1	
3	VCCO_3	V12	
4	VCCO_4	AP16	
4	VCCO_4	AP10	
4	VCCO_4	AL7	
4	VCCO_4	AK15	
4	VCCO_4	AD15	
4	VCCO_4	AD14	
4	VCCO_4	AD13	
4	VCCO_4	AD12	
4	VCCO_4	AC17	
4	VCCO_4	AC16	
4	VCCO_4	AC15	
4	VCCO_4	AC14	
4	VCCO_4	AC13	
5	VCCO_5	AP25	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
0	IO_L76P_0	C24		
0	IO_L77N_0	K22		
0	IO_L77P_0	K21		
0	IO_L78N_0	E22		
0	IO_L78P_0	E23		
0	IO_L79N_0	B23		
0	IO_L79P_0	B24		
0	IO_L80N_0	J22		
0	IO_L80P_0	J21		
0	IO_L81N_0	G21		
0	IO_L81P_0/VREF_0	G22		
0	IO_L82N_0	A23		
0	IO_L82P_0	A24		
0	IO_L83N_0	H22		
0	IO_L83P_0	H21		
0	IO_L84N_0	F21		
0	IO_L84P_0	F22		
0	IO_L91N_0/VREF_0	B21		
0	IO_L91P_0	B22		
0	IO_L92N_0	L20		
0	IO_L92P_0	M20		
0	IO_L93N_0	E21		
0	IO_L93P_0	D22		
0	IO_L94N_0/VREF_0	A21		
0	IO_L94P_0	A22		
0	IO_L95N_0/GCLK7P	H20		
0	IO_L95P_0/GCLK6S	J20		
0	IO_L96N_0/GCLK5P	C21		
0	IO_L96P_0/GCLK4S	D21		
1	IO_L96N_1/GCLK3P	F19		
1	IO_L96P_1/GCLK2S	F20		
1	IO_L95N_1/GCLK1P	H19		
1	IO_L95P_1/GCLK0S	H18		
1	IO_L94N_1	C19		
1	IO_L94P_1/VREF_1	C20		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
2	IO_L09P_2/VREF_2	H7	NC	
2	IO_L10N_2	G3	NC	
2	IO_L10P_2	F3	NC	
2	IO_L11N_2	J8	NC	
2	IO_L11P_2	K8	NC	
2	IO_L12N_2	H5	NC	
2	IO_L12P_2	G5	NC	
2	IO_L19N_2	G1		
2	IO_L19P_2	F1		
2	IO_L20N_2	K9		
2	IO_L20P_2	L10		
2	IO_L21N_2	K7		
2	IO_L21P_2/VREF_2	J7		
2	IO_L22N_2	H2		
2	IO_L22P_2	G2		
2	IO_L23N_2	L9		
2	IO_L23P_2	M9		
2	IO_L24N_2	H4		
2	IO_L24P_2	G4		
2	IO_L25N_2	J3		
2	IO_L25P_2	H3		
2	IO_L26N_2	M10		
2	IO_L26P_2	N10		
2	IO_L27N_2	K6		
2	IO_L27P_2/VREF_2	J6		
2	IO_L28N_2	K5		
2	IO_L28P_2	J5		
2	IO_L29N_2	N11		
2	IO_L29P_2	P11		
2	IO_L30N_2	M7		
2	IO_L30P_2	L7		
2	IO_L31N_2	J1	NC	
2	IO_L31P_2	H1	NC	
2	IO_L32N_2	L8	NC	
2	IO_L32P_2	M8	NC	
2	IO_L33N_2	K4	NC	