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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	8448
Number of Logic Elements/Cells	-
Total RAM Bits	2654208
Number of I/O	684
Number of Gates	6000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	957-BBGA, FCBGA
Supplier Device Package	957-FCBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v6000-4bf957c

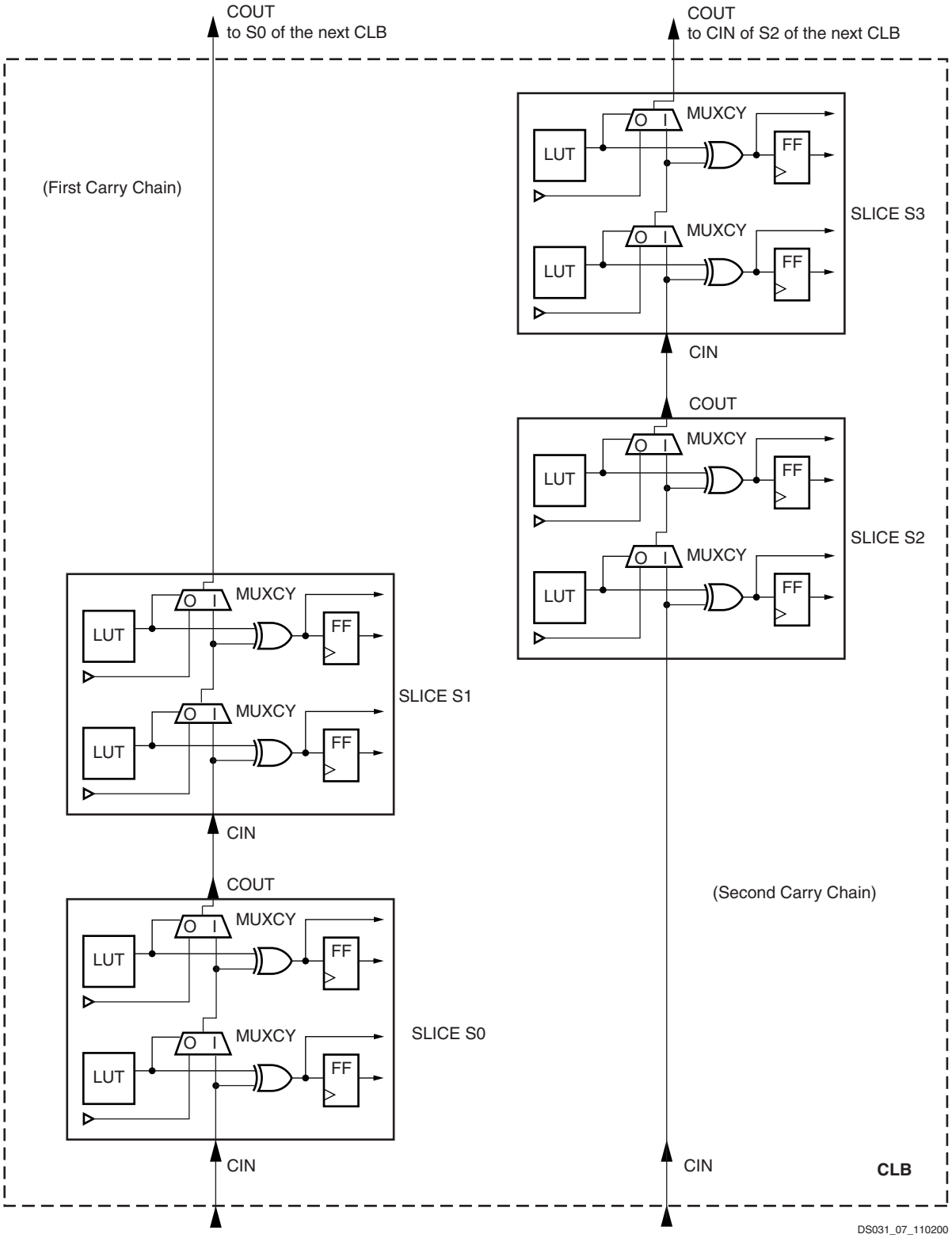

Figure 24: **Fast Carry Logic Path**

3. "NO_CHANGE"

The "NO_CHANGE" option maintains the content of the output registers, regardless of the write operation. The clock edge during the write mode has no effect on the content of the data output register DO. When the port is configured as "NO_CHANGE", only a read operation loads a new value in the output register DO, as shown in Figure 33.

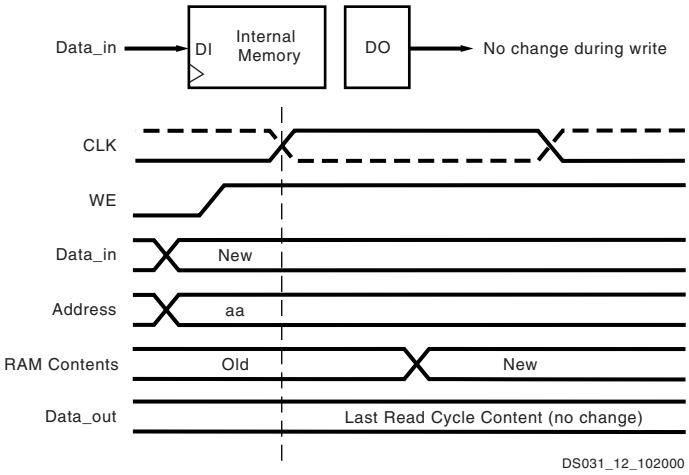

Figure 33: **NO_CHANGE Mode**

Control Pins and Attributes

Virtex-II SelectRAM memory has two independent ports with the control signals described in Table 17. All control inputs including the clock have an optional inversion.

Table 17: **Control Functions**

Control Signal	Function
CLK	Read and Write Clock
EN	Enable affects Read, Write, Set, Reset
WE	Write Enable
SSR	Set DO register to SRVAL (attribute)

Initial memory content is determined by the INIT_xx attributes. Separate attributes determine the output register value after device configuration (INIT) and SSR is asserted (SRVAL). Both attributes (INIT_B and SRVAL) are available for each port when a block SelectRAM resource is configured as dual-port RAM.

Locations

Virtex-II SelectRAM memory blocks are located in either four or six columns. The number of blocks per column depends of the device array size and is equivalent to the number of CLBs in a column divided by four. Column locations are shown in Table 18.

Table 18: **SelectRAM Memory Floor Plan**

Device	Columns	SelectRAM Blocks	
		Per Column	Total
XC2V40	2	2	4
XC2V80	2	4	8
XC2V250	4	6	24
XC2V500	4	8	32
XC2V1000	4	10	40
XC2V1500	4	12	48
XC2V2000	4	14	56
XC2V3000	6	16	96
XC2V4000	6	20	120
XC2V6000	6	24	144
XC2V8000	6	28	168

Extended LVDS DC Specifications (LVDSEXT_33 & LVDSEXT_25)

Table 9: **Extended LVDS DC Specifications**

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}			3.3 or 2.5		V
Output High voltage for Q and $\overline{Q}$	V_{OH}	R_T = 100 Ω across Q and $\overline{Q}$ signals			1.785	V
Output Low voltage for Q and $\overline{Q}$	V_{OL}	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.705			V
Differential output voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{ODIFF}	R_T = 100 Ω across Q and $\overline{Q}$ signals	440		820	mV
Output common-mode voltage	V_{OCM}	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.200	1.375	V
Differential input voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{IDIFF}	Common-mode input voltage = 1.25 V	100	350	N/A	mV
Input common-mode voltage	V_{ICM}	Differential input voltage = ±350 mV	0.2	1.25	V_{CCO} – 0.5	V

LVPECL DC Specifications

These values are valid when driving a 100 Ω differential load only, i.e., a 100 Ω resistor between the two receiver pins. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. Table 10 summarizes the DC output specifications of LVPECL. For more information on using LVPECL, see the *Virtex-II User Guide*.

Table 10: **LVPECL DC Specifications**

DC Parameter	Min	Max	Min	Max	Min	Max	Units
V_{CCO}	3.0		3.3		3.6		V
V_{OH}	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{OL}	0.96	1.27	1.06	1.43	1.30	1.57	V
V_{IH}	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	0.86	2.125	0.86	2.125	0.86	2.125	V
Differential Input Voltage	0.3	–	0.3	–	0.3	–	V

Virtex-II Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Setup and Hold for LVTTL Standard, *With* DCM

Table 36: **Global Clock Setup and Hold for LVTTL Standard, *With* DCM**

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in IOB Input Switching Characteristics Standard Adjustments, page 11.						
No Delay Global Clock and IFF with DCM	T_{PSDCM}/T_{PHDCM}	XC2V40	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		XC2V80	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		XC2V250	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		XC2V500	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		XC2V1000	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		XC2V1500	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		XC2V2000	1.70/–0.90	1.70/–0.90	1.96/–0.76	ns
		XC2V3000	1.70/–0.90	1.70/–0.90	1.96/–0.76	ns
		XC2V4000	1.70/–0.90	1.70/–0.90	1.96/–0.76	ns
		XC2V6000	1.70/–0.90	1.70/–0.90	1.96/–0.76	ns
		XC2V8000		1.70/–0.90	1.96/–0.76	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.

Global Clock Setup and Hold for LVTTL Standard, *Without* DCM

Table 37: **Global Clock Setup and Hold for LVTTL Standard, *Without* DCM**

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard.(2) For data input with different standards, adjust the setup time delay by the values shown in IOB Input Switching Characteristics Standard Adjustments, page 11.						
Full Delay Global Clock and IFF(1) without DCM	T_{PSFD}/T_{PHFD}	XC2V40	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V80	2.10/ 0.00	2.10/ 0.00	2.21/ 0.00	ns
		XC2V250	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V500	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V1000	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V1500	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V2000	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V3000	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V4000	2.00/ 0.00	2.00/ 0.00	2.30/ 0.00	ns
		XC2V6000	1.92/ 0.50	1.92/ 0.50	2.21/ 0.50	ns
		XC2V8000		2.38/ 0.00	2.60/ 0.00	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. These values are parametrically measured.

Source Synchronous Timing Budgets

This section describes how to use the parameters provided in the Source-Synchronous Switching Characteristics section to develop system-specific timing budgets. The following analysis provides information necessary for determining Virtex-II contributions to an overall system timing analysis; no assumptions are made about the effects of Inter-Symbol Interference or PCB skew.

Virtex-II Transmitter Data-Valid Window (T_X)

T_X is the minimum aggregate valid data period for a source-synchronous data bus at the pins of the device and is calculated as follows:

$$T_X = \text{Data Period} - [\text{Jitter}^{(1)} + \text{Duty Cycle Distortion}^{(2)} + \text{TCKSKEW}^{(3)} + \text{TPKGSKEW}^{(4)}]$$

Notes:

1. Jitter values and accumulation methodology to be provided in a future release of this document. The absolute period jitter values found in the DCM Timing Parameters section of the particular DCM output clock used to clock the IOB FF can be used for a best case analysis.
2. This value depends on the clocking methodology used. See Note1 for Table 45.
3. This value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.
4. These values represent the worst-case skew between any two balls of the package: shortest flight time to longest flight time from Pad to Ball.

Virtex-II Receiver Data-Valid Window (R_X)

R_X is the required minimum aggregate valid data period for a source-synchronous data bus at the pins of the device and is calculated as follows:

$$R_X = [\text{TSAMP}^{(1)} + \text{TCKSKEW}^{(2)} + \text{TPKGSKEW}^{(3)}]$$

Notes:

1. This parameter indicates the total sampling error of Virtex-II DDR input registers across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 and CLK180 DCM jitter in a quiet system
   - Worst-case duty-cycle distortion
   - DCM accuracy (phase offset)
   - DCM phase shift resolution.

   These measurements do not include package or clock tree skew.
2. This value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.
3. These values represent the worst-case skew between any two balls of the package: shortest flight time to longest flight time from Pad to Ball.

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
11/07/00	1.0	Early access draft.
12/06/00	1.1	Initial release.
01/15/01	1.2	Added values to the tables in the Virtex-II Performance Characteristics and Virtex-II Switching Characteristics sections.
01/25/01	1.3	• The data sheet was divided into four modules (per the current style standard). • Updated values in the Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables. • Table 18, "Delay Measurement Methodology"
04/23/01	1.5	• Updated values in the Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables. • Added T_{REG32} symbol to Table 23. • Skipped v1.4 to sync with other modules. Reverted to traditional double-column format.

Date	Version	Revision
08/01/03	3.0	• Table 13: All Virtex-II devices and speed grades now Production. • Updated values in Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables, based on values extracted from **speedsfile version 1.116**. • Table 34 and Table 35: Revised test setup footnote to refer to Figure 1. Previously specified a capacitive load parameter. • Figure 1: Added note to figure regarding termination resistors.
10/14/03	3.1	• Table 1: Changed T_J description from “Operating junction temperature” to “Maximum junction temperature”. • In section General Power Supply Requirements, replaced reference to Answer Record 11713 with reference to **XAPP689** regarding handling of simultaneously switching outputs (SSO). • In section I/O Standard Adjustment Measurement Methodology: - Table 18 renamed Input Delay Measurement Methodology. Added footnotes. - Added new Table 19, Output Delay Measurement Methodology. - Replaced Figure 1, Generalized Test Setup, with new drawing. - Revised and extended text describing output delay measurement procedure. • Table 45, Table 47, and Table 48: All Source-Synchronous parameters for all devices now available in these tables. • XC2V8000 is no longer offered in the -6 speed grade. The following tables containing parameters or other references to this device/grade combination were corrected accordingly: Table 13, Table 14, Table 34, Table 35, Table 36, Table 37, Table 45, Table 47, and Table 48. • Table 39: For Input Clock Low/High Pulse Width, PSCLK and CLKIN, changed existing Footnote (2) to new Footnote (3).
03/29/04	3.2	• Table 4: - For XC2V40, added Maximum quiescent supply current specifications. - For all devices, updated Typical specifications for I_{CCINTQ} and I_{CCAUXQ}. • Section Power-On Power Supply Requirements, page 3: Added Footnote (1) qualifying statement that power supplies can be turned on in any sequence. • Added section Configuration Timing, page 27. This section includes new timing diagrams as well as parameter specification tables formerly included in the **Virtex-II Platform FPGA User Guide**. • Table 20, Clock Distribution Switching Characteristics: Added parameter T_{GSI}/T_{GIS} (Global Clock Buffer S Input Setup/Hold to I1 and I2 Inputs). • Table 38, Operating Frequency Ranges: Added Footnote (4) to all four CLKIN parameters. • Recompiled for backward compatibility with Acrobat 4 and above.
06/24/04	3.3	• Table 1: Added T_{SOL} parameters for Pb-free package devices.
03/01/05	3.4	• Updated values in Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables, based on values extracted from **speedsfile version 1.120**. • Table 2: Corrected Footnote (1) to require connecting V_{BATT} to V_{CCAUX} or GND if battery is not used. • Table 3: Corrected "V_{REF} current per bank" to "V_{REF} current per pin." • Section Power-On Power Supply Requirements: Added word “monotonically” to description of supply voltage ramp-on requirements. Added sentence to footnote (1) indicating that if the stated requirements are violated, no damage to the device will result, but configuration will probably fail. • Figure 3 and Figure 4: Corrected to show DOUT transitions driven by falling edge of CCLK.

Table 4: **Virtex-II Pin Definitions *(Continued)***

Pin Name	Direction	Description
PROG_B	Input	Active Low asynchronous reset to configuration logic. This pin has a permanent weak pull-up resistor.
DONE	Input/Output	DONE is a bidirectional signal with an optional internal pull-up resistor. As an output, this pin indicates completion of the configuration process. As an input, a Low level on DONE can be configured to delay the start-up sequence.
M2, M1, M0	Input	Configuration mode selection.
HSWAP_EN	Input	Enable I/O pull-ups during configuration.
TCK	Input	Boundary Scan Clock.
TDI	Input	Boundary Scan Data Input.
TDO	Output	Boundary Scan Data Output.
TMS	Input	Boundary Scan Mode Select.
PWRDWN_B	Input *(unsupported)*	Active Low power-down pin (unsupported). *Driving this pin Low can adversely affect device operation and configuration.* PWRDWN_B is internally pulled High, which is its default state. It does not require an external pull-up.
Other Pins		
DXN, DXP	N/A	Temperature-sensing diode pins (Anode: DXP, Cathode: DXN).
V_{BATT}	Input	Decryptor key memory backup supply. Connect V_{BATT} to V_{CCAUX} or GND if battery is not used.
RSVD	N/A	Reserved pin - do not connect.
V_{CCO}	Input	Power-supply pins for the output drivers (per bank).
V_{CCAUX}	Input	Power-supply pins for auxiliary circuits.
V_{CCINT}	Input	Power-supply pins for the internal core logic.
GND	Input	Ground.

Notes:
1. All dedicated pins (JTAG and configuration) are powered by V_{CCAUX} (independent of the bank V_{CCO} voltage).

Table 6: **FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
7	IO_L45N_7	F5	NC	NC
7	IO_L43P_7	F1	NC	NC
7	IO_L43N_7	F2	NC	NC
7	IO_L06P_7	F3	NC	
7	IO_L06N_7	F4	NC	
7	IO_L04P_7	E1	NC	
7	IO_L04N_7	E2	NC	
7	IO_L03P_7/VREF_7	E3		
7	IO_L03N_7	E4		
7	IO_L02P_7/VRN_7	D2		
7	IO_L02N_7/VRP_7	D3		
7	IO_L01P_7	D1		
7	IO_L01N_7	C1		
0	VCCO_0	F8		
0	VCCO_0	F7		
0	VCCO_0	E8		
1	VCCO_1	F10		
1	VCCO_1	F9		
1	VCCO_1	E9		
2	VCCO_2	H12		
2	VCCO_2	H11		
2	VCCO_2	G11		
3	VCCO_3	K11		
3	VCCO_3	J12		
3	VCCO_3	J11		
4	VCCO_4	M9		
4	VCCO_4	L10		
4	VCCO_4	L9		
5	VCCO_5	M8		
5	VCCO_5	L8		
5	VCCO_5	L7		
6	VCCO_6	K6		
6	VCCO_6	J6		

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
0	VCCO_0	F7		
1	VCCO_1	G14		
1	VCCO_1	G13		
1	VCCO_1	G12		
1	VCCO_1	F16		
1	VCCO_1	F15		
2	VCCO_2	L16		
2	VCCO_2	K16		
2	VCCO_2	J16		
2	VCCO_2	H17		
2	VCCO_2	G17		
3	VCCO_3	T17		
3	VCCO_3	R17		
3	VCCO_3	P16		
3	VCCO_3	N16		
3	VCCO_3	M16		
4	VCCO_4	U16		
4	VCCO_4	U15		
4	VCCO_4	T14		
4	VCCO_4	T13		
4	VCCO_4	T12		
5	VCCO_5	U8		
5	VCCO_5	U7		
5	VCCO_5	T11		
5	VCCO_5	T10		
5	VCCO_5	T9		
6	VCCO_6	T6		
6	VCCO_6	R6		
6	VCCO_6	P7		
6	VCCO_6	N7		
6	VCCO_6	M7		
7	VCCO_7	L7		
7	VCCO_7	K7		
7	VCCO_7	J7		

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
4	IO_L78N_4	Y15	NC	
4	IO_L78P_4	AA15	NC	
4	IO_L91N_4/VREF_4	W15		
4	IO_L91P_4	W16		
4	IO_L92N_4	AB15		
4	IO_L92P_4	AC15		
4	IO_L93N_4	AD15		
4	IO_L93P_4	AE15		
4	IO_L94N_4/VREF_4	W14		
4	IO_L94P_4	Y14		
4	IO_L95N_4/GCLK3S	AA14		
4	IO_L95P_4/GCLK2P	AB14		
4	IO_L96N_4/GCLK1S	AC14		
4	IO_L96P_4/GCLK0P	AD14		
5	IO_L96N_5/GCLK7S	AC13		
5	IO_L96P_5/GCLK6P	AB13		
5	IO_L95N_5/GCLK5S	AA13		
5	IO_L95P_5/GCLK4P	Y13		
5	IO_L94N_5	W13		
5	IO_L94P_5/VREF_5	W12		
5	IO_L93N_5	AF15		
5	IO_L93P_5	AF14		
5	IO_L92N_5	AF13		
5	IO_L92P_5	AF12		
5	IO_L91N_5	AE12		
5	IO_L91P_5/VREF_5	AD12		
5	IO_L78N_5	AC12	NC	
5	IO_L78P_5	AB12	NC	
5	IO_L76N_5	AA12	NC	
5	IO_L76P_5	Y12	NC	
5	IO_L75N_5/VREF_5	AF11	NC	
5	IO_L75P_5	AF10	NC	
5	IO_L73N_5	AE11	NC	
5	IO_L73P_5	AD11	NC	
5	IO_L72N_5	AC11		
5	IO_L72P_5	AB11		

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
2	IO_L70P_2	N19
2	IO_L72N_2	M22
2	IO_L72P_2	M23
2	IO_L73N_2	M24
2	IO_L73P_2	N24
2	IO_L75N_2	M26
2	IO_L75P_2/VREF_2	M27
2	IO_L76N_2	N20
2	IO_L76P_2	N21
2	IO_L78N_2	N22
2	IO_L78P_2	N23
2	IO_L91N_2	N25
2	IO_L91P_2	P25
2	IO_L93N_2	N26
2	IO_L93P_2/VREF_2	N27
2	IO_L94N_2	P20
2	IO_L94P_2	P21
2	IO_L96N_2	P22
2	IO_L96P_2	P23
3	IO_L96N_3	R27
3	IO_L96P_3	R26
3	IO_L94N_3	R25
3	IO_L94P_3	R24
3	IO_L93N_3/VREF_3	R23
3	IO_L93P_3	T23
3	IO_L91N_3	R22
3	IO_L91P_3	R21
3	IO_L78N_3	R20
3	IO_L78P_3	R19
3	IO_L76N_3	T27
3	IO_L76P_3	T26
3	IO_L75N_3/VREF_3	T24
3	IO_L75P_3	U24
3	IO_L73N_3	T22
3	IO_L73P_3	U22

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
2	IO_L21N_2	H7	
2	IO_L21P_2/VREF_2	J7	
2	IO_L22N_2	H6	
2	IO_L22P_2	G6	
2	IO_L23N_2	L10	
2	IO_L23P_2	L9	
2	IO_L24N_2	G3	
2	IO_L24P_2	F3	
2	IO_L25N_2	G2	
2	IO_L25P_2	F2	
2	IO_L26N_2	M10	
2	IO_L26P_2	N10	
2	IO_L27N_2	J6	
2	IO_L27P_2/VREF_2	K6	
2	IO_L28N_2	J5	
2	IO_L28P_2	H5	
2	IO_L29N_2	L7	
2	IO_L29P_2	K7	
2	IO_L30N_2	J4	
2	IO_L30P_2	H4	
2	IO_L43N_2	G1	
2	IO_L43P_2	F1	
2	IO_L44N_2	L8	
2	IO_L44P_2	M8	
2	IO_L45N_2	J1	
2	IO_L45P_2/VREF_2	H2	
2	IO_L46N_2	J3	
2	IO_L46P_2	H3	
2	IO_L47N_2	M9	
2	IO_L47P_2	N9	
2	IO_L48N_2	L5	
2	IO_L48P_2	K5	
2	IO_L49N_2	K2	
2	IO_L49P_2	J2	
2	IO_L50N_2	N7	
2	IO_L50P_2	M7	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
7	IO_L03N_7	F30	
7	IO_L02P_7/VRN_7	K25	
7	IO_L02N_7/VRP_7	J25	
7	IO_L01P_7	D33	
7	IO_L01N_7	E33	
0	VCCO_0	M22	
0	VCCO_0	M21	
0	VCCO_0	M20	
0	VCCO_0	M19	
0	VCCO_0	M18	
0	VCCO_0	L23	
0	VCCO_0	L22	
0	VCCO_0	L21	
0	VCCO_0	L20	
0	VCCO_0	E20	
0	VCCO_0	D28	
0	VCCO_0	A25	
0	VCCO_0	A19	
1	VCCO_1	M17	
1	VCCO_1	M16	
1	VCCO_1	M15	
1	VCCO_1	M14	
1	VCCO_1	M13	
1	VCCO_1	L15	
1	VCCO_1	L14	
1	VCCO_1	L13	
1	VCCO_1	L12	
1	VCCO_1	E15	
1	VCCO_1	D7	
1	VCCO_1	A16	
1	VCCO_1	A10	
2	VCCO_2	U12	
2	VCCO_2	T12	
2	VCCO_2	T1	
2	VCCO_2	R12	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
3	IO_L58N_3	AD5		
3	IO_L58P_3	AE5		
3	IO_L57N_3/VREF_3	AE11		
3	IO_L57P_3	AD11		
3	IO_L56N_3	AG1		
3	IO_L56P_3	AH1		
3	IO_L55N_3	AD6		
3	IO_L55P_3	AE6		
3	IO_L54N_3	AF10		
3	IO_L54P_3	AE10		
3	IO_L53N_3	AG2		
3	IO_L53P_3	AH2		
3	IO_L52N_3	AF4		
3	IO_L52P_3	AG4		
3	IO_L51N_3/VREF_3	AG8		
3	IO_L51P_3	AF8		
3	IO_L50N_3	AH3		
3	IO_L50P_3	AJ3		
3	IO_L49N_3	AE7		
3	IO_L49P_3	AF7		
3	IO_L48N_3	AG9		
3	IO_L48P_3	AF9		
3	IO_L47N_3	AF6		
3	IO_L47P_3	AG6		
3	IO_L46N_3	AG5		
3	IO_L46P_3	AH5		
3	IO_L45N_3/VREF_3	AF12		
3	IO_L45P_3	AE12		
3	IO_L44N_3	AJ1		
3	IO_L44P_3	AK1		
3	IO_L43N_3	AH4		
3	IO_L43P_3	AJ4		
3	IO_L36N_3	AG11	NC	
3	IO_L36P_3	AF11	NC	
3	IO_L35N_3	AK2	NC	
3	IO_L35P_3	AL2	NC	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
3	IO_L10N_3	AK7	NC	
3	IO_L10P_3	AL7	NC	
3	IO_L09N_3/VREF_3	AK11	NC	
3	IO_L09P_3	AJ10	NC	
3	IO_L08N_3	AR1	NC	
3	IO_L08P_3	AT1	NC	
3	IO_L07N_3	AM5	NC	
3	IO_L07P_3	AN5	NC	
3	IO_L06N_3	AM7		
3	IO_L06P_3	AL8		
3	IO_L05N_3	AP3		
3	IO_L05P_3	AP4		
3	IO_L04N_3	AM6		
3	IO_L04P_3	AN6		
3	IO_L03N_3/VREF_3	AJ13		
3	IO_L03P_3	AH13		
3	IO_L02N_3/VRP_3	AR3		
3	IO_L02P_3/VRN_3	AT2		
3	IO_L01N_3	AP5		
3	IO_L01P_3	AR4		
4	IO_L01N_4/BUSY/DOUT(1)	AV4		
4	IO_L01P_4/INIT_B	AU4		
4	IO_L02N_4/D0/DIN(1)	AM9		
4	IO_L02P_4/D1	AM10		
4	IO_L03N_4/D2/ALT_VRP_4	AT6		
4	IO_L03P_4/D3/ALT_VRN_4	AR6		
4	IO_L04N_4/VREF_4	AU6		
4	IO_L04P_4	AU5		
4	IO_L05N_4/VRP_4	AL10		
4	IO_L05P_4/VRN_4	AL11		
4	IO_L06N_4	AR8		
4	IO_L06P_4	AR7		
4	IO_L07N_4	AW5	NC	
4	IO_L07P_4	AW4	NC	
4	IO_L08N_4	AK12	NC	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
6	VCCO_6	AG33		
6	VCCO_6	AF38		
6	VCCO_6	AF27		
6	VCCO_6	AE31		
6	VCCO_6	AE27		
6	VCCO_6	AE26		
6	VCCO_6	AD27		
6	VCCO_6	AD26		
6	VCCO_6	AC29		
6	VCCO_6	AC27		
6	VCCO_6	AC26		
6	VCCO_6	AB37		
6	VCCO_6	AB27		
6	VCCO_6	AB26		
6	VCCO_6	AA27		
6	VCCO_6	AA26		
7	VCCO_7	W27		
7	VCCO_7	W26		
7	VCCO_7	V37		
7	VCCO_7	V27		
7	VCCO_7	V26		
7	VCCO_7	U29		
7	VCCO_7	U27		
7	VCCO_7	U26		
7	VCCO_7	T27		
7	VCCO_7	T26		
7	VCCO_7	R31		
7	VCCO_7	R27		
7	VCCO_7	R26		
7	VCCO_7	P38		
7	VCCO_7	P27		
7	VCCO_7	N33		
7	VCCO_7	L35		
NA	CCLK	AT5		
NA	PROG_B	H31		

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
5	IO_L73P_5	AJ20	
5	IO_L72N_5	AG18	
5	IO_L72P_5	AG19	
5	IO_L71N_5	AF18	
5	IO_L71P_5	AF19	
5	IO_L70N_5	AK20	
5	IO_L70P_5	AK21	
5	IO_L69N_5/VREF_5	AH20	
5	IO_L69P_5	AH21	
5	IO_L68N_5	AD19	
5	IO_L68P_5	AD20	
5	IO_L67N_5	AL21	
5	IO_L67P_5	AL22	
5	IO_L54N_5	AG20	
5	IO_L54P_5	AG21	
5	IO_L53N_5	AB19	
5	IO_L53P_5	AB20	
5	IO_L52N_5	AJ21	
5	IO_L52P_5	AJ22	
5	IO_L51N_5/VREF_5	AF20	
5	IO_L51P_5	AF21	
5	IO_L50N_5	AE20	
5	IO_L50P_5	AE21	
5	IO_L49N_5	AK22	
5	IO_L49P_5	AK23	
5	IO_L30N_5	AJ23	NC
5	IO_L30P_5	AJ24	NC
5	IO_L29N_5	AC20	NC
5	IO_L29P_5	AC21	NC
5	IO_L28N_5	AL23	NC
5	IO_L28P_5	AL24	NC
5	IO_L27N_5/VREF_5	AL25	NC
5	IO_L27P_5	AL26	NC
5	IO_L26N_5	AD21	NC
5	IO_L26P_5	AD22	NC
5	IO_L25N_5	AH23	NC
5	IO_L25P_5	AH24	NC
5	IO_L24N_5	AG22	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
7	IO_L06N_7	E28	
7	IO_L05P_7	K22	
7	IO_L05N_7	K21	
7	IO_L04P_7	F29	
7	IO_L04N_7	E29	
7	IO_L03P_7/VREF_7	H26	
7	IO_L03N_7	H25	
7	IO_L02P_7/VRN_7	G26	
7	IO_L02N_7/VRP_7	F27	
7	IO_L01P_7	D30	
7	IO_L01N_7	D29	
0	VCCO_0	C18	
0	VCCO_0	C25	
0	VCCO_0	F22	
0	VCCO_0	H18	
0	VCCO_0	L17	
0	VCCO_0	L18	
0	VCCO_0	L19	
0	VCCO_0	L20	
0	VCCO_0	M17	
0	VCCO_0	M18	
0	VCCO_0	M19	
1	VCCO_1	C7	
1	VCCO_1	C14	
1	VCCO_1	F10	
1	VCCO_1	H14	
1	VCCO_1	L12	
1	VCCO_1	L13	
1	VCCO_1	L14	
1	VCCO_1	L15	
1	VCCO_1	M13	
1	VCCO_1	M14	
1	VCCO_1	M15	
2	VCCO_2	G3	
2	VCCO_2	K6	
2	VCCO_2	M11	
2	VCCO_2	N11	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
NA	DXP	B28	
NA	VBATT	D5	
NA	RSVD	B4	
NA	VCCAUX	B16	
NA	VCCAUX	C2	
NA	VCCAUX	C30	
NA	VCCAUX	T2	
NA	VCCAUX	T30	
NA	VCCAUX	AJ2	
NA	VCCAUX	AJ30	
NA	VCCAUX	AK16	
NA	VCCINT	K15	
NA	VCCINT	K17	
NA	VCCINT	L11	
NA	VCCINT	L16	
NA	VCCINT	L21	
NA	VCCINT	M12	
NA	VCCINT	M16	
NA	VCCINT	M20	
NA	VCCINT	N13	
NA	VCCINT	N14	
NA	VCCINT	N15	
NA	VCCINT	N16	
NA	VCCINT	N17	
NA	VCCINT	N18	
NA	VCCINT	N19	
NA	VCCINT	P13	
NA	VCCINT	P19	
NA	VCCINT	R10	
NA	VCCINT	R13	
NA	VCCINT	R19	
NA	VCCINT	R22	
NA	VCCINT	T11	
NA	VCCINT	T12	
NA	VCCINT	T13	
NA	VCCINT	T19	
NA	VCCINT	T20	