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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	8448
Number of Logic Elements/Cells	-
Total RAM Bits	2654208
Number of I/O	684
Number of Gates	6000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	957-BBGA, FCBGA
Supplier Device Package	957-FCBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v6000-4bf957i

Virtex-II Platform FPGAs: Introduction and Overview

DS031-1 (v3.5) November 5, 2007 **Product Specification**

Summary of Virtex-II™ Features

- Industry First Platform FPGA Solution
- IP-Immersion Architecture
  - Densities from 40K to 8M system gates
  - 420 MHz internal clock speed (Advance Data)
  - 840+ Mb/s I/O (Advance Data)
- SelectRAM™ Memory Hierarchy
  - 3 Mb of dual-port RAM in 18 Kbit block SelectRAM resources
  - Up to 1.5 Mb of distributed SelectRAM resources
- High-Performance Interfaces to External Memory
  - DRAM interfaces
    - SDR / DDR SDRAM
    - Network FCRAM
    - Reduced Latency DRAM
  - SRAM interfaces
    - SDR / DDR SRAM
    - QDR™ SRAM
  - CAM interfaces
- Arithmetic Functions
  - Dedicated 18-bit x 18-bit multiplier blocks
  - Fast look-ahead carry logic chains
- Flexible Logic Resources
  - Up to 93,184 internal registers / latches with Clock Enable
  - Up to 93,184 look-up tables (LUTs) or cascadable 16-bit shift registers
  - Wide multiplexers and wide-input function support
  - Horizontal cascade chain and sum-of-products support
  - Internal 3-state bussing
- High-Performance Clock Management Circuitry
  - Up to 12 DCM (Digital Clock Manager) modules
    - Precise clock de-skew
    - Flexible frequency synthesis
    - High-resolution phase shifting
  - 16 global clock multiplexer buffers
- Active Interconnect Technology
  - Fourth generation segmented routing structure
  - Predictable, fast routing delay, independent of fanout
- SelectIO™-Ultra Technology
  - Up to 1,108 user I/Os
  - 19 single-ended and six differential standards
  - Programmable sink current (2 mA to 24 mA) per I/O
  - Digitally Controlled Impedance (DCI) I/O: on-chip termination resistors for single-ended I/O standards
  - PCI-X compatible (133 MHz and 66 MHz) at 3.3V
  - PCI compliant (66 MHz and 33 MHz) at 3.3V
  - CardBus compliant (33 MHz) at 3.3V
  - Differential Signaling
    - 840 Mb/s Low-Voltage Differential Signaling I/O (LVDS) with current mode drivers
    - Bus LVDS I/O
    - Lightning Data Transport (LDT) I/O with current driver buffers
    - Low-Voltage Positive Emitter-Coupled Logic (LVPECL) I/O
    - Built-in DDR input and output registers
  - Proprietary high-performance SelectLink Technology
    - High-bandwidth data path
    - Double Data Rate (DDR) link
    - Web-based HDL generation methodology
- Supported by Xilinx Foundation™ and Alliance Series™ Development Systems
  - Integrated VHDL and Verilog design flows
  - Compilation of 10M system gates designs
  - Internet Team Design (ITD) tool
- SRAM-Based In-System Configuration
  - Fast SelectMAP configuration
  - Triple Data Encryption Standard (DES) security option (Bitstream Encryption)
  - IEEE 1532 support
  - Partial reconfiguration
  - Unlimited reprogrammability
  - Readback capability
- 0.15 µm 8-Layer Metal Process with 0.12 µm High-Speed Transistors
- 1.5V (V_{CCINT}) Core Power Supply, Dedicated 3.3V V_{CCAUX} Auxiliary and V_{CCO} I/O Power Supplies
- IEEE 1149.1 Compatible Boundary-Scan Logic Support
- Flip-Chip and Wire-Bond Ball Grid Array (BGA) Packages in Three Standard Fine Pitches (0.80 mm, 1.00 mm, and 1.27 mm)
- Wire-Bond BGA Devices Available in Pb-Free Packaging (www.xilinx.com/pbfree)
- 100% Factory Tested

Table 4: **LVTTL and LVCMOS Programmable Currents (Sink and Source)**

SelectI/O-Ultra	Programmable Current (Worst-Case Guaranteed Minimum)						
LVTTL	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA
LVCMOS33	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA
LVCMOS25	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA
LVCMOS18	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	n/a
LVCMOS15	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	n/a

Figure 6 shows the SSTL2, SSTL3, and HSTL configurations. HSTL can sink current up to 48 mA. (HSTL IV)

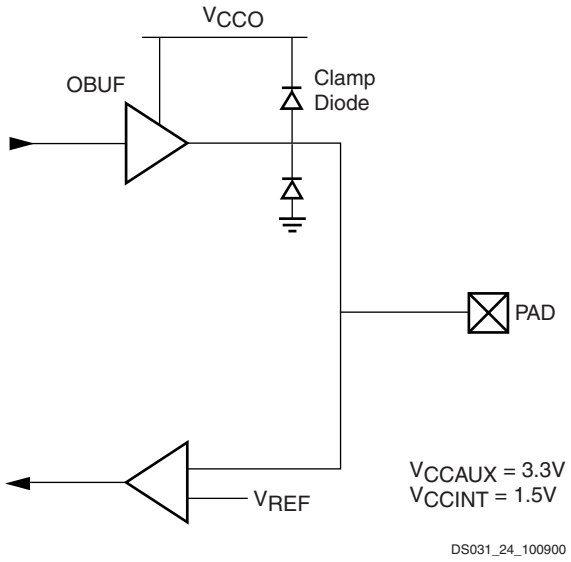


Figure 6: **SSTL or HSTL SelectI/O-Ultra Standards**

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. Virtex-II uses two memory cells to control the configuration of an I/O as an input. This is to reduce the probability of an I/O configured as an input from flipping to an output when subjected to a single event upset (SEU) in space applications.

Prior to configuration, all outputs not involved in configuration are forced into their high-impedance state. The pull-down resistors and the weak-keeper circuits are inactive. The dedicated pin HSWAP_EN controls the pull-up resistors prior to configuration. By default, HSWAP_EN is set high, which disables the pull-up resistors on user I/O pins. When HSWAP_EN is set low, the pull-up resistors are activated on user I/O pins.

All Virtex-II IOBs support IEEE 1149.1 compatible Boundary-Scan testing.

Input Path

The Virtex-II IOB input path routes input signals directly to internal logic and / or through an optional input flip-flop or latch, or through the DDR input registers. An optional delay element at the D-input of the storage element eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the Virtex-II device, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signaling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, V_{REF}. The need to supply V_{REF} imposes constraints on which standards can be used in the same bank. See I/O banking description.

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output and / or the 3-state signal can be routed to the buffer directly from the internal logic or through an output / 3-state flip-flop or latch, or through the DDR output / 3-state registers.

Each output driver can be individually programmed for a wide range of low-voltage signaling standards. In most signaling standards, the output High voltage depends on an externally supplied V_{CCO} voltage. The need to supply V_{CCO} imposes constraints on which standards can be used in the same bank. See I/O banking description.

I/O Banking

Some of the I/O standards described above require V_{CCO} and V_{REF} voltages. These voltages are externally supplied and connected to device pins that serve groups of IOB blocks, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from dividing each edge of the FPGA into two banks, as shown in Figure 7 and Figure 8. Each bank has multiple V_{CCO} pins, all of which must be connected to the same voltage. This voltage is determined by the output standards in use.

IOB Output Switching Characteristics Standard Adjustments

Table 17 gives all standard-specific adjustments for output delays terminating at pads, based on standard capacitive load, C_{REF}. Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

Table 17: **IOB Output Switching Characteristics Standard Adjustments**

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-6	-5	-4	
LVTTL (Low-Voltage Transistor-Transistor Logic), Slow, 2 mA	LVTTL_S2	T_{OLVTTL_S2}	9.42	9.71	10.68	ns
LVTTL, Slow, 4 mA	LVTTL_S4	T_{OLVTTL_S4}	5.77	5.95	6.55	ns
LVTTL, Slow, 6 mA	LVTTL_S6	T_{OLVTTL_S6}	4.11	4.24	4.66	ns
LVTTL, Slow, 8 mA	LVTTL_S8	T_{OLVTTL_S8}	2.87	2.96	3.26	ns
LVTTL, Slow, 12 mA	LVTTL_S12	T_{OLVTTL_S12}	2.32	2.39	2.63	ns
LVTTL, Slow, 16 mA	LVTTL_S16	T_{OLVTTL_S16}	1.70	1.75	1.93	ns
LVTTL, Slow, 24 mA	LVTTL_S24	T_{OLVTTL_S24}	1.26	1.30	1.43	ns
LVTTL, Fast, 2 mA	LVTTL_F2	T_{OLVTTL_F2}	6.52	6.72	7.39	ns
LVTTL, Fast, 4 mA	LVTTL_F4	T_{OLVTTL_F4}	2.80	2.88	3.17	ns
LVTTL, Fast, 6 mA	LVTTL_F6	T_{OLVTTL_F6}	1.57	1.62	1.78	ns
LVTTL, Fast, 8 mA	LVTTL_F8	T_{OLVTTL_F8}	0.46	0.48	0.52	ns
LVTTL, Fast, 12 mA	LVTTL_F12	T_{OLVTTL_F12}	0.00	0.00	0.00	ns
LVTTL, Fast, 16 mA	LVTTL_F16	T_{OLVTTL_F16}	–0.13	–0.14	–0.15	ns
LVTTL, Fast, 24 mA	LVTTL_F24	T_{OLVTTL_F24}	–0.22	–0.23	–0.26	ns
LVCMOS (Low-Voltage CMOS), 3.3V, Slow, 2 mA	LVCMOS33_S2	$T_{OLVCMOS33\_S2}$	7.67	7.91	8.70	ns
LVCMOS, 3.3V, Slow, 4 mA	LVCMOS33_S4	$T_{OLVCMOS33\_S4}$	4.37	4.50	4.95	ns
LVCMOS, 3.3V, Slow, 6 mA	LVCMOS33_S6	$T_{OLVCMOS33\_S6}$	3.34	3.44	3.78	ns
LVCMOS, 3.3V, Slow, 8 mA	LVCMOS33_S8	$T_{OLVCMOS33\_S8}$	2.29	2.36	2.60	ns
LVCMOS, 3.3V, Slow, 12 mA	LVCMOS33_S12	$T_{OLVCMOS33\_S12}$	1.91	1.97	2.16	ns
LVCMOS, 3.3V, Slow, 16 mA	LVCMOS33_S16	$T_{OLVCMOS33\_S16}$	1.24	1.27	1.40	ns
LVCMOS, 3.3V, Slow, 24 mA	LVCMOS33_S24	$T_{OLVCMOS33\_S24}$	1.18	1.22	1.34	ns
LVCMOS, 3.3V, Fast, 2 mA	LVCMOS33_F2	$T_{OLVCMOS33\_F2}$	5.82	6.00	6.60	ns
LVCMOS, 3.3V, Fast, 4 mA	LVCMOS33_F4	$T_{OLVCMOS33\_F4}$	2.48	2.55	2.81	ns
LVCMOS, 3.3V, Fast, 6 mA	LVCMOS33_F6	$T_{OLVCMOS33\_F6}$	1.28	1.31	1.45	ns
LVCMOS, 3.3V, Fast, 8 mA	LVCMOS33_F8	$T_{OLVCMOS33\_F8}$	0.48	0.49	0.54	ns
LVCMOS, 3.3V, Fast, 12 mA	LVCMOS33_F12	$T_{OLVCMOS33\_F12}$	0.27	0.28	0.31	ns
LVCMOS, 3.3V, Fast, 16 mA	LVCMOS33_F16	$T_{OLVCMOS33\_F16}$	–0.14	–0.14	–0.15	ns
LVCMOS, 3.3V, Fast, 24 mA	LVCMOS33_F24	$T_{OLVCMOS33\_F24}$	–0.21	–0.21	–0.23	ns
LVCMOS, 2.5V, Slow, 2 mA	LVCMOS25_S2	$T_{OLVCMOS25\_S2}$	9.11	9.39	10.33	ns
LVCMOS, 2.5V, Slow, 4 mA	LVCMOS25_S4	$T_{OLVCMOS25\_S4}$	5.00	5.16	5.67	ns
LVCMOS, 2.5V, Slow, 6 mA	LVCMOS25_S6	$T_{OLVCMOS25\_S6}$	4.53	4.67	5.13	ns
LVCMOS, 2.5V, Slow, 8 mA	LVCMOS25_S8	$T_{OLVCMOS25\_S8}$	3.86	3.98	4.38	ns
LVCMOS, 2.5V, Slow, 12 mA	LVCMOS25_S12	$T_{OLVCMOS25\_S12}$	2.84	2.93	3.22	ns
LVCMOS, 2.5V, Slow, 16 mA	LVCMOS25_S16	$T_{OLVCMOS25\_S16}$	2.36	2.43	2.67	ns
LVCMOS, 2.5V, Slow, 24 mA	LVCMOS25_S24	$T_{OLVCMOS25\_S24}$	2.00	2.06	2.27	ns
LVCMOS, 2.5V, Fast, 2 mA	LVCMOS25_F2	$T_{OLVCMOS25\_F2}$	4.06	4.18	4.60	ns
LVCMOS, 2.5V, Fast, 4 mA	LVCMOS25_F4	$T_{OLVCMOS25\_F4}$	1.15	1.18	1.30	ns
LVCMOS, 2.5V, Fast, 6 mA	LVCMOS25_F6	$T_{OLVCMOS25\_F6}$	0.72	0.74	0.81	ns
LVCMOS, 2.5V, Fast, 8 mA	LVCMOS25_F8	$T_{OLVCMOS25\_F8}$	0.33	0.34	0.37	ns
LVCMOS, 2.5V, Fast, 12 mA	LVCMOS25_F12	$T_{OLVCMOS25\_F12}$	0.02	0.02	0.03	ns

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
3	IO_L52P_3	P18	NC	
3	IO_L51N_3/VREF_3	P22	NC	
3	IO_L51P_3	P21	NC	
3	IO_L49N_3	P20	NC	
3	IO_L49P_3	P19	NC	
3	IO_L48N_3	R22		
3	IO_L48P_3	R21		
3	IO_L46N_3	R20		
3	IO_L46P_3	R19		
3	IO_L45N_3/VREF_3	R18		
3	IO_L45P_3	P17		
3	IO_L43N_3	T22		
3	IO_L43P_3	T21		
3	IO_L24N_3	T20	NC	NC
3	IO_L24P_3	T19	NC	NC
3	IO_L22N_3	U22	NC	NC
3	IO_L22P_3	U21	NC	NC
3	IO_L21N_3/VREF_3	U20	NC	NC
3	IO_L21P_3	U19	NC	NC
3	IO_L19N_3	T18	NC	NC
3	IO_L19P_3	U18	NC	NC
3	IO_L06N_3	V22		
3	IO_L06P_3	V21		
3	IO_L04N_3	V20		
3	IO_L04P_3	V19		
3	IO_L03N_3/VREF_3	W22		
3	IO_L03P_3	W21		
3	IO_L02N_3/VRP_3	Y22		
3	IO_L02P_3/VRN_3	Y21		
3	IO_L01N_3	W20		
3	IO_L01P_3	AA20		
4	IO_L01N_4/BUSY/DOUT(1)	AB19		
4	IO_L01P_4/INIT_B	AA19		

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
NA	GND	M10		
NA	GND	M9		
NA	GND	L14		
NA	GND	L13		
NA	GND	L12		
NA	GND	L11		
NA	GND	L10		
NA	GND	L9		
NA	GND	K14		
NA	GND	K13		
NA	GND	K12		
NA	GND	K11		
NA	GND	K10		
NA	GND	K9		
NA	GND	J14		
NA	GND	J13		
NA	GND	J12		
NA	GND	J11		
NA	GND	J10		
NA	GND	J9		
NA	GND	D19		
NA	GND	D4		
NA	GND	C20		
NA	GND	C3		
NA	GND	B21		
NA	GND	B2		
NA	GND	A22		
NA	GND	A1		

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

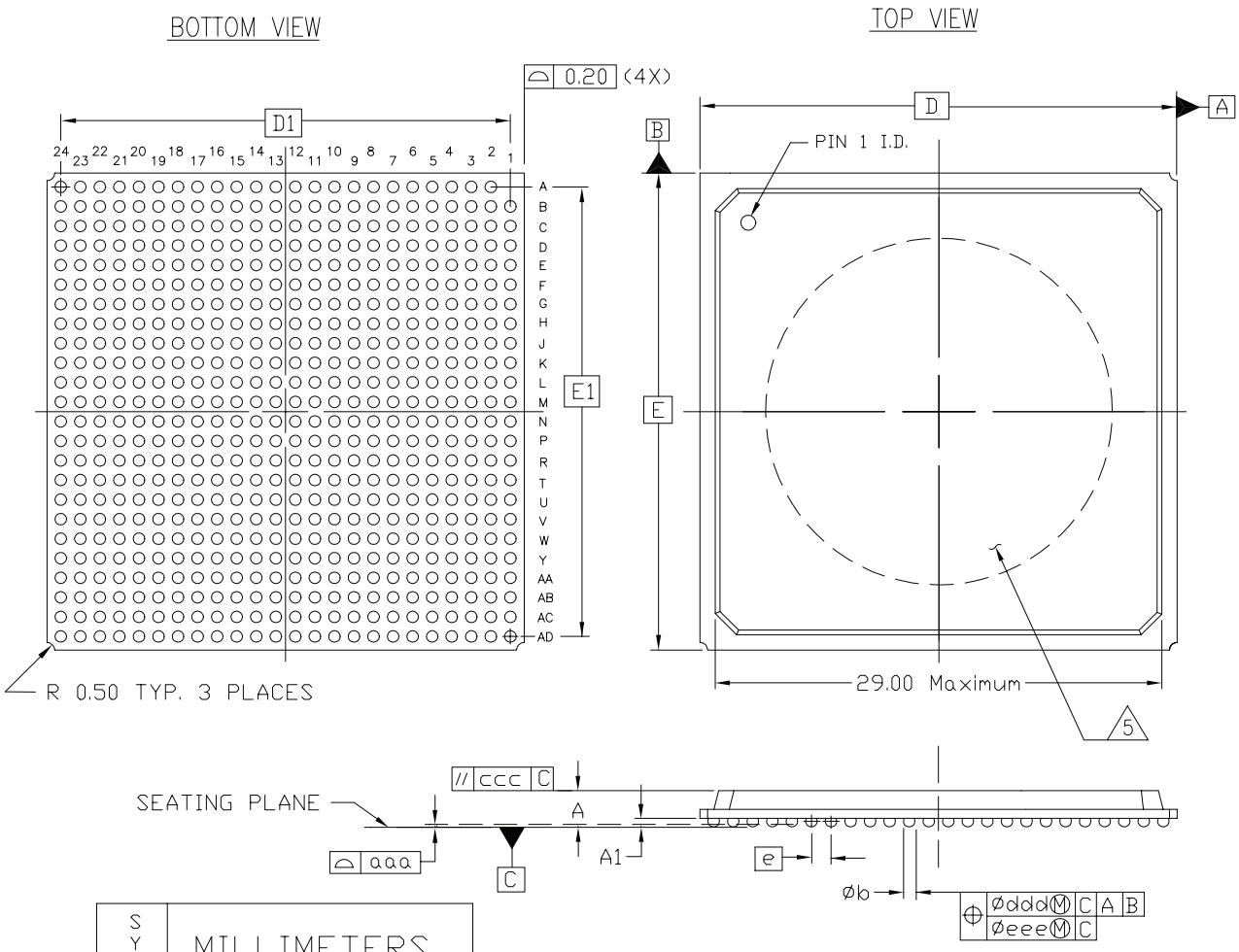
Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
1	IO_L92P_1	A15		
1	IO_L91N_1	B15		
1	IO_L91P_1/VREF_1	C15		
1	IO_L78N_1	D15	NC	
1	IO_L78P_1	E15	NC	
1	IO_L76N_1	F15	NC	
1	IO_L76P_1	G15	NC	
1	IO_L75N_1/VREF_1	G16	NC	
1	IO_L75P_1	F16	NC	
1	IO_L73N_1	A16	NC	
1	IO_L73P_1	A17	NC	
1	IO_L72N_1	B16		
1	IO_L72P_1	C16		
1	IO_L70N_1	D16		
1	IO_L70P_1	E16		
1	IO_L69N_1/VREF_1	C17		
1	IO_L69P_1	D17		
1	IO_L67N_1	H16		
1	IO_L67P_1	G17		
1	IO_L54N_1	E17		
1	IO_L54P_1	F17		
1	IO_L52N_1	A18		
1	IO_L52P_1	A19		
1	IO_L51N_1/VREF_1	E18		
1	IO_L51P_1	D18		
1	IO_L49N_1	B18		
1	IO_L49P_1	C18		
1	IO_L27N_1/VREF_1	F19	NC	NC
1	IO_L27P_1	F18	NC	NC
1	IO_L25N_1	G18	NC	NC
1	IO_L25P_1	G19	NC	NC
1	IO_L24N_1	B19		
1	IO_L24P_1	C19		
1	IO_L22N_1	D19		
1	IO_L22P_1	E19		
1	IO_L21N_1/VREF_1	A20		
1	IO_L21P_1	A21		

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
1	VCCO_1	B14		
2	VCCO_2	M16		
2	VCCO_2	L23		
2	VCCO_2	L19		
2	VCCO_2	L16		
2	VCCO_2	K16		
2	VCCO_2	F22		
3	VCCO_3	W22		
3	VCCO_3	R16		
3	VCCO_3	P23		
3	VCCO_3	P19		
3	VCCO_3	P16		
3	VCCO_3	N16		
4	VCCO_4	AC14		
4	VCCO_4	AB19		
4	VCCO_4	W14		
4	VCCO_4	T15		
4	VCCO_4	T14		
4	VCCO_4	T13		
5	VCCO_5	AC11		
5	VCCO_5	AB6		
5	VCCO_5	W11		
5	VCCO_5	T12		
5	VCCO_5	T11		
5	VCCO_5	T10		
6	VCCO_6	W3		
6	VCCO_6	R9		
6	VCCO_6	P9		
6	VCCO_6	P6		
6	VCCO_6	P2		
6	VCCO_6	N9		
7	VCCO_7	M9		
7	VCCO_7	L9		
7	VCCO_7	L6		
7	VCCO_7	L2		
7	VCCO_7	K9		

BG575/BGG575 Standard BGA Package Specifications (1.27mm pitch)



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A		2.33	2.60
A_1	0.50	0.60	0.70
D/E	31.00 BSC		
D_1/E_1	29.21 REF		
e	1.27BSC		
Øb	0.60	0.75	0.90
aaa			0.20
ccc			0.35
ddd			0.30
eee			0.15
M	24		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-BAN-1 (DEPOPULATED)
4. NO SOLDER BALL AND LAND ON A1.

5 HEAT SINK OPTION

575-BALL MOLDED BGA (BG575/BGG575)

Figure 5: **BG575/BGG575 Standard BGA Package Specifications**

BG728/BGG728 Standard BGA Package

As shown in Table 10, XC2V3000 Virtex-II devices are available in the BG728/BGG728 BGA package. Following this table are the BG728/BGG728 Standard BGA Package Specifications (1.27mm pitch).

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
0	IO_L01N_0	B3
0	IO_L01P_0	A3
0	IO_L02N_0	B4
0	IO_L02P_0	A4
0	IO_L03N_0/VRP_0	C5
0	IO_L03P_0/VRN_0	C6
0	IO_L04N_0/VREF_0	B5
0	IO_L04P_0	A5
0	IO_L05N_0	E6
0	IO_L05P_0	D6
0	IO_L06N_0	B6
0	IO_L06P_0	A6
0	IO_L19N_0	E7
0	IO_L19P_0	D8
0	IO_L21N_0	F8
0	IO_L21P_0/VREF_0	E8
0	IO_L22N_0	C7
0	IO_L22P_0	C8
0	IO_L24N_0	B7
0	IO_L24P_0	A7
0	IO_L25N_0	H9
0	IO_L25P_0	J9
0	IO_L27N_0	F9
0	IO_L27P_0/VREF_0	G9
0	IO_L28N_0	E9
0	IO_L28P_0	D9
0	IO_L30N_0	C9
0	IO_L30P_0	B9
0	IO_L49N_0	A8
0	IO_L49P_0	A9
0	IO_L51N_0	G10
0	IO_L51P_0/VREF_0	H10
0	IO_L52N_0	F10

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
1	IO_L27N_1/VREF_1	F19
1	IO_L27P_1	G19
1	IO_L25N_1	J19
1	IO_L25P_1	J20
1	IO_L24N_1	C20
1	IO_L24P_1	C21
1	IO_L22N_1	D20
1	IO_L22P_1	E21
1	IO_L21N_1/VREF_1	E20
1	IO_L21P_1	F20
1	IO_L19N_1	A21
1	IO_L19P_1	B21
1	IO_L06N_1	A22
1	IO_L06P_1	B22
1	IO_L05N_1	C22
1	IO_L05P_1	C23
1	IO_L04N_1	D22
1	IO_L04P_1/VREF_1	E22
1	IO_L03N_1/VRP_1	A23
1	IO_L03P_1/VRN_1	B23
1	IO_L02N_1	A24
1	IO_L02P_1	B24
1	IO_L01N_1	A25
1	IO_L01P_1	B25
2	IO_L01N_2	C27
2	IO_L01P_2	D27
2	IO_L02N_2/VRP_2	D25
2	IO_L02P_2/VRN_2	D26
2	IO_L03N_2	E24
2	IO_L03P_2/VREF_2	E25
2	IO_L04N_2	E26
2	IO_L04P_2	E27
2	IO_L06N_2	F23
2	IO_L06P_2	F24
2	IO_L19N_2	F25

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
2	VCCO_2	L10		
2	VCCO_2	L9		
2	VCCO_2	K9		
2	VCCO_2	E2		
3	VCCO_3	AF2		
3	VCCO_3	AA9		
3	VCCO_3	Y10		
3	VCCO_3	Y9		
3	VCCO_3	W10		
3	VCCO_3	W9		
3	VCCO_3	V10		
3	VCCO_3	V9		
3	VCCO_3	V3		
3	VCCO_3	U10		
3	VCCO_3	T10		
4	VCCO_4	AJ5		
4	VCCO_4	AH13		
4	VCCO_4	AB13		
4	VCCO_4	AB12		
4	VCCO_4	AB11		
4	VCCO_4	AB10		
4	VCCO_4	AA15		
4	VCCO_4	AA14		
4	VCCO_4	AA13		
4	VCCO_4	AA12		
4	VCCO_4	AA11		
5	VCCO_5	AJ26		
5	VCCO_5	AH18		
5	VCCO_5	AB21		
5	VCCO_5	AB20		
5	VCCO_5	AB19		
5	VCCO_5	AB18		
5	VCCO_5	AA20		
5	VCCO_5	AA19		
5	VCCO_5	AA18		
5	VCCO_5	AA17		
5	VCCO_5	AA16		

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
NA	GND	AE32	
NA	GND	AE3	
NA	GND	AC30	
NA	GND	AC5	
NA	GND	AA28	
NA	GND	AA21	
NA	GND	AA20	
NA	GND	AA19	
NA	GND	AA18	
NA	GND	AA17	
NA	GND	AA16	
NA	GND	AA15	
NA	GND	AA14	
NA	GND	AA7	
NA	GND	Y33	
NA	GND	Y21	
NA	GND	Y20	
NA	GND	Y19	
NA	GND	Y18	
NA	GND	Y17	
NA	GND	Y16	
NA	GND	Y15	
NA	GND	Y14	
NA	GND	Y2	
NA	GND	W26	
NA	GND	W21	
NA	GND	W20	
NA	GND	W19	
NA	GND	W18	
NA	GND	W17	
NA	GND	W16	
NA	GND	W15	
NA	GND	W14	
NA	GND	W9	
NA	GND	V21	
NA	GND	V20	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
0	IO_L76P_0	C24		
0	IO_L77N_0	K22		
0	IO_L77P_0	K21		
0	IO_L78N_0	E22		
0	IO_L78P_0	E23		
0	IO_L79N_0	B23		
0	IO_L79P_0	B24		
0	IO_L80N_0	J22		
0	IO_L80P_0	J21		
0	IO_L81N_0	G21		
0	IO_L81P_0/VREF_0	G22		
0	IO_L82N_0	A23		
0	IO_L82P_0	A24		
0	IO_L83N_0	H22		
0	IO_L83P_0	H21		
0	IO_L84N_0	F21		
0	IO_L84P_0	F22		
0	IO_L91N_0/VREF_0	B21		
0	IO_L91P_0	B22		
0	IO_L92N_0	L20		
0	IO_L92P_0	M20		
0	IO_L93N_0	E21		
0	IO_L93P_0	D22		
0	IO_L94N_0/VREF_0	A21		
0	IO_L94P_0	A22		
0	IO_L95N_0/GCLK7P	H20		
0	IO_L95P_0/GCLK6S	J20		
0	IO_L96N_0/GCLK5P	C21		
0	IO_L96P_0/GCLK4S	D21		
1	IO_L96N_1/GCLK3P	F19		
1	IO_L96P_1/GCLK2S	F20		
1	IO_L95N_1/GCLK1P	H19		
1	IO_L95P_1/GCLK0S	H18		
1	IO_L94N_1	C19		
1	IO_L94P_1/VREF_1	C20		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
1	IO_L69N_1/VREF_1	E15		
1	IO_L69P_1	E16		
1	IO_L68N_1	K17		
1	IO_L68P_1	K16		
1	IO_L67N_1	C15		
1	IO_L67P_1	B15		
1	IO_L60N_1	F15		
1	IO_L60P_1	F16		
1	IO_L59N_1	H16		
1	IO_L59P_1	H15		
1	IO_L58N_1	C13		
1	IO_L58P_1	C14		
1	IO_L57N_1/VREF_1	D13		
1	IO_L57P_1	D14		
1	IO_L56N_1	M17		
1	IO_L56P_1	M16		
1	IO_L55N_1	A12		
1	IO_L55P_1	A13		
1	IO_L54N_1	B12		
1	IO_L54P_1	B13		
1	IO_L53N_1	G15		
1	IO_L53P_1	G14		
1	IO_L52N_1	C11		
1	IO_L52P_1	C12		
1	IO_L51N_1/VREF_1	F13		
1	IO_L51P_1	F14		
1	IO_L50N_1	L16		
1	IO_L50P_1	L15		
1	IO_L49N_1	A10		
1	IO_L49P_1	A11		
1	IO_L36N_1	E12	NC	
1	IO_L36P_1	E13	NC	
1	IO_L35N_1	K15	NC	
1	IO_L35P_1	J14	NC	
1	IO_L34N_1	B9	NC	
1	IO_L34P_1	B10	NC	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
4	IO_L08P_4	AL12	NC	
4	IO_L09N_4	AP9	NC	
4	IO_L09P_4/VREF_4	AP8	NC	
4	IO_L10N_4	AV6	NC	
4	IO_L10P_4	AV5	NC	
4	IO_L11N_4	AM11	NC	
4	IO_L11P_4	AM12	NC	
4	IO_L12N_4	AN10	NC	
4	IO_L12P_4	AN9	NC	
4	IO_L19N_4	AU8		
4	IO_L19P_4	AU7		
4	IO_L20N_4	AH14		
4	IO_L20P_4	AH15		
4	IO_L21N_4	AT8		
4	IO_L21P_4/VREF_4	AT7		
4	IO_L22N_4	AW7		
4	IO_L22P_4	AW6		
4	IO_L23N_4	AK13		
4	IO_L23P_4	AK14		
4	IO_L24N_4	AR10		
4	IO_L24P_4	AR9		
4	IO_L25N_4	AV8		
4	IO_L25P_4	AV7		
4	IO_L26N_4	AJ14		
4	IO_L26P_4	AJ15		
4	IO_L27N_4	AP11		
4	IO_L27P_4/VREF_4	AP10		
4	IO_L28N_4	AU10		
4	IO_L28P_4	AU9		
4	IO_L29N_4	AL13		
4	IO_L29P_4	AL14		
4	IO_L30N_4	AN12		
4	IO_L30P_4	AN11		
4	IO_L31N_4	AW9	NC	
4	IO_L31P_4	AW8	NC	
4	IO_L32N_4	AM13	NC	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
6	IO_L47N_6	AJ39		
6	IO_L48P_6	AG35		
6	IO_L48N_6	AH35		
6	IO_L49P_6	AG32		
6	IO_L49N_6	AF32		
6	IO_L50P_6	AH37		
6	IO_L50N_6	AG37		
6	IO_L51P_6	AD29		
6	IO_L51N_6/VREF_6	AE29		
6	IO_L52P_6	AD28		
6	IO_L52N_6	AC28		
6	IO_L53P_6	AH38		
6	IO_L53N_6	AG38		
6	IO_L54P_6	AF34		
6	IO_L54N_6	AG34		
6	IO_L55P_6	AE32		
6	IO_L55N_6	AD32		
6	IO_L56P_6	AH39		
6	IO_L56N_6	AG39		
6	IO_L57P_6	AE33		
6	IO_L57N_6/VREF_6	AF33		
6	IO_L58P_6	AD30		
6	IO_L58N_6	AC30		
6	IO_L59P_6	AF37		
6	IO_L59N_6	AE37		
6	IO_L60P_6	AF36		
6	IO_L60N_6	AG36		
6	IO_L67P_6	AD31		
6	IO_L67N_6	AC31		
6	IO_L68P_6	AE34		
6	IO_L68N_6	AD34		
6	IO_L69P_6	AD35		
6	IO_L69N_6/VREF_6	AE35		
6	IO_L70P_6	AB28		
6	IO_L70N_6	AA28		
6	IO_L71P_6	AF39		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
7	IO_L02P_7/VRN_7	M27		
7	IO_L02N_7/VRP_7	L27		
7	IO_L01P_7	D38		
7	IO_L01N_7	E37		
0	VCCO_0	P25		
0	VCCO_0	P24		
0	VCCO_0	P23		
0	VCCO_0	P22		
0	VCCO_0	P21		
0	VCCO_0	N26		
0	VCCO_0	N25		
0	VCCO_0	N24		
0	VCCO_0	N23		
0	VCCO_0	N22		
0	VCCO_0	N21		
0	VCCO_0	L23		
0	VCCO_0	J25		
0	VCCO_0	G27		
0	VCCO_0	E29		
0	VCCO_0	C22		
0	VCCO_0	B26		
1	VCCO_1	P19		
1	VCCO_1	P18		
1	VCCO_1	P17		
1	VCCO_1	P16		
1	VCCO_1	P15		
1	VCCO_1	N19		
1	VCCO_1	N18		
1	VCCO_1	N17		
1	VCCO_1	N16		
1	VCCO_1	N15		
1	VCCO_1	N14		
1	VCCO_1	L17		
1	VCCO_1	J15		
1	VCCO_1	G13		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	GND	AR26		
NA	GND	AR14		
NA	GND	AR5		
NA	GND	AP34		
NA	GND	AP6		
NA	GND	AN33		
NA	GND	AN20		
NA	GND	AN7		
NA	GND	AM32		
NA	GND	AM23		
NA	GND	AM17		
NA	GND	AM8		
NA	GND	AL31		
NA	GND	AL9		
NA	GND	AK30		
NA	GND	AK20		
NA	GND	AK10		
NA	GND	AJ38		
NA	GND	AJ29		
NA	GND	AJ11		
NA	GND	AJ2		
NA	GND	AF35		
NA	GND	AF5		
NA	GND	AD23		
NA	GND	AD22		
NA	GND	AD21		
NA	GND	AD20		
NA	GND	AD19		
NA	GND	AD18		
NA	GND	AD17		
NA	GND	AC36		
NA	GND	AC32		
NA	GND	AC24		
NA	GND	AC23		
NA	GND	AC22		
NA	GND	AC21		

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
NA	GND	T14	
NA	GND	T15	
NA	GND	T16	
NA	GND	T17	
NA	GND	T18	
NA	GND	T22	
NA	GND	T25	
NA	GND	T28	
NA	GND	T31	
NA	GND	U14	
NA	GND	U15	
NA	GND	U16	
NA	GND	U17	
NA	GND	U18	
NA	GND	V14	
NA	GND	V15	
NA	GND	V16	
NA	GND	V17	
NA	GND	V18	
NA	GND	W7	
NA	GND	W25	
NA	GND	AB4	
NA	GND	AB16	
NA	GND	AB28	
NA	GND	AC9	
NA	GND	AC23	
NA	GND	AD2	
NA	GND	AD8	
NA	GND	AD24	
NA	GND	AD30	
NA	GND	AE7	
NA	GND	AE13	
NA	GND	AE16	
NA	GND	AE19	
NA	GND	AE25	
NA	GND	AF6	
NA	GND	AF26	
NA	GND	AG5	

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
11/07/00	1.0	Early access draft.
11/22/00	1.1	Initial Xilinx release. Made the following corrections: CS144 package - Table 5, page 5: • Added missing pin D10 in Bank 1. • Changed dedicated pins A2 and B2 to RSVD (from DXN and DXP). FG256 package - Table 6, page 10: • Changed dedicated pins A3 and A4 to RSVD (from DXN and DXP). FG896 package - Table 11, page 94: • Corrected pin AG1 in Bank 4 to be AG12. FF1152 package - Table 12, page 120: • Corrected pin Y3 in Bank 6 to be Y32.
12/19/00	1.2	Reverse designations were fixed for pins in every package.
01/25/01	1.3	Data sheet divided into four modules (per current style standard). DXN and DXP pin information added for CS144 package (Table 5) and FG256 package (Table 6).
02/07/01	1.4	DXN and DXP pin information was changed back to RSVD for the CS144 package (Table 5) and the FG256 package (Table 6).
04/02/01	1.5	• ALT_VRN and ALT_VRP pin information was added for each package. • Table 8, page 34 – added No Connect designations for the XC2V1500 device in the FG676 package. • Reverted to traditional double-column format.
11/07/01	1.6	• Updated list of devices supported in the FF1152, FF1517, and BF957 packages.
09/26/02	1.7	• Updated Table 3 to reflect devices supported in the BG728 and BF957 packages. • Added mention of LVPECL to pin definition in Table 4.
10/07/02	1.8	• Corrected Table 10 heading to reflect supported devices in the BG728 package.
12/06/02	1.8.1	• Enhanced the description of the PWRDWN_B pin in Table 4.
05/07/03	1.8.2	• Added clarification to Table 4 and all device pinout tables regarding the dual-use nature of pins D0/DIN and BUSY/DOUT during configuration.
06/19/03	1.8.3	• The final GND pin in each of five pinout tables was inadvertently deleted in v1.8.2. This revision restores the deleted GND pins as follows: - Pin C5, Table 5, page 5 (CS144) - Pin A1, Table 6, page 10 (FG256) - Pin A2, Table 10, page 72 (BG728) - Pin A2, Table 12, page 120 (FF1152) - Pin AL30, Table 14, page 198 (BF957)
08/01/03	2.0	All Virtex-II devices and speed grades now Production. See Table 13, Module 3.
03/29/04	2.0.1	Recompiled for backward compatibility with Acrobat 4 and above.
06/24/04	3.3	Added references to, and new package drawings for, Pb-free wire-bond packages CSG, FGG, and BGG. (Revision number advanced to level of complete data sheet.)
03/01/05	3.4	Table 4: Changed Direction for User I/O pins (IO_LXXY_#) from “Input/Output” to “Input/Output/Bidirectional”. Added requirement to V_{BATT} to connect pin to V_{CCAUX} or GND if battery is not used.
11/05/07	3.5	Updated copyright notice and legal disclaimer.