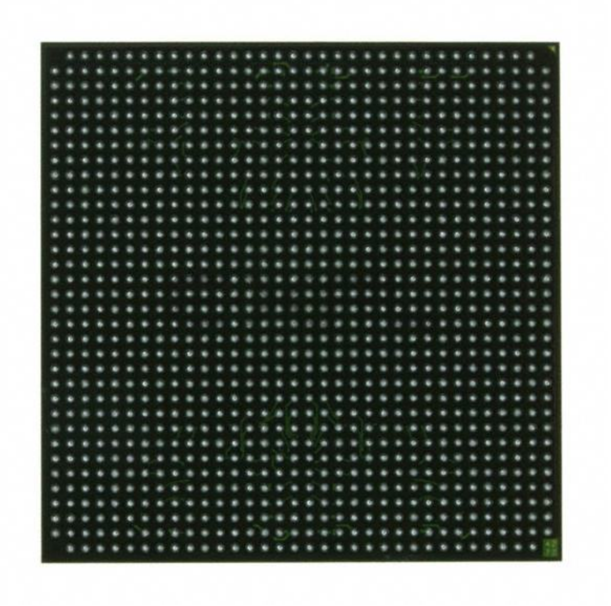
AMD Xilinx - XC2V6000-4FFG1152I Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	8448
Number of Logic Elements/Cells	-
Total RAM Bits	2654208
Number of I/O	824
Number of Gates	6000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v6000-4ffg1152i

Digitally Controlled Impedance (DCI)

Today's chip output signals with fast edge rates require termination to prevent reflections and maintain signal integrity. High pin count packages (especially ball grid arrays) can not accommodate external termination resistors.

Virtex-II XCITE DCI provides controlled impedance drivers and on-chip termination for single-ended and differential I/Os. This eliminates the need for external resistors, and improves signal integrity. The DCI feature can be used on any IOB by selecting one of the DCI I/O standards.

When applied to inputs, DCI provides input parallel termination. When applied to outputs, DCI provides controlled impedance drivers (series termination) or output parallel termination.

DCI operates independently on each I/O bank. When a DCI I/O standard is used in a particular I/O bank, external reference resistors must be connected to two dual-function pins on the bank. These resistors, voltage reference of N transistor (VRN) and the voltage reference of P transistor (VRP) are shown in Figure 9.

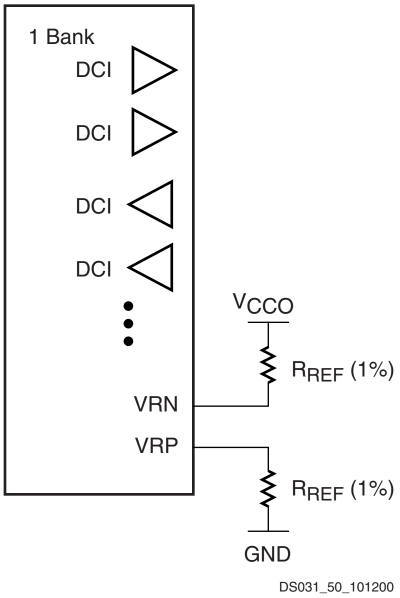


Figure 9: **DCI in a Virtex-II Bank**

When used with a terminated I/O standard, the value of resistors are specified by the standard (typically 50Ω). When used with a controlled impedance driver, the resistors set the output impedance of the driver within the specified range (25Ω to 100Ω). For all series and parallel terminations listed in Table 6 and Table 7, the reference resistors must have the same value for any given bank. One percent resistors are recommended.

The DCI system adjusts the I/O impedance to match the two external reference resistors, or half of the reference resistors, and compensates for impedance changes due to voltage and/or temperature fluctuations. The adjustment is done by turning parallel transistors in the IOB on or off.

Controlled Impedance Drivers (Series Term.)

DCI can be used to provide a buffer with a controlled output impedance. It is desirable for this output impedance to match the transmission line impedance (Z_0). Virtex-II input buffers also support LVDCI and LVDCI_DV2 I/O standards.

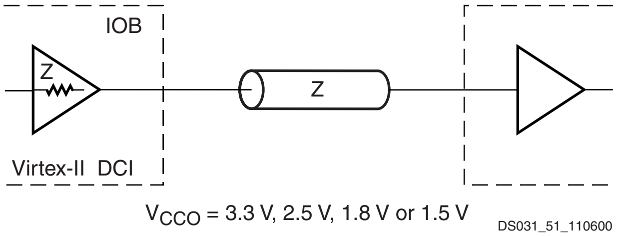


Figure 10: **Internal Series Termination**

Table 6: **SelectI/O-Ultra Controlled Impedance Buffers**

V_{CCO}	DCI	DCI Half Impedance
3.3 V	LVDCI_33	LVDCI_DV2_33
2.5 V	LVDCI_25	LVDCI_DV2_25
1.8 V	LVDCI_18	LVDCI_DV2_18
1.5 V	LVDCI_15	LVDCI_DV2_15

Controlled Impedance Drivers (Parallel)

DCI also provides on-chip termination for SSTL3, SSTL2, HSTL (Class I, II, III, or IV), and GTL/GTLP receivers or transmitters on bidirectional lines.

Table 7 and Table 8 list the on-chip parallel terminations available in Virtex-II devices. V_{CCO} must be set according to Table 3. Note that there is a V_{CCO} requirement for GTL_DCI and GTLP_DCI, due to the on-chip termination resistor.

Table 7: **SelectI/O-Ultra Buffers With On-Chip Parallel Termination**

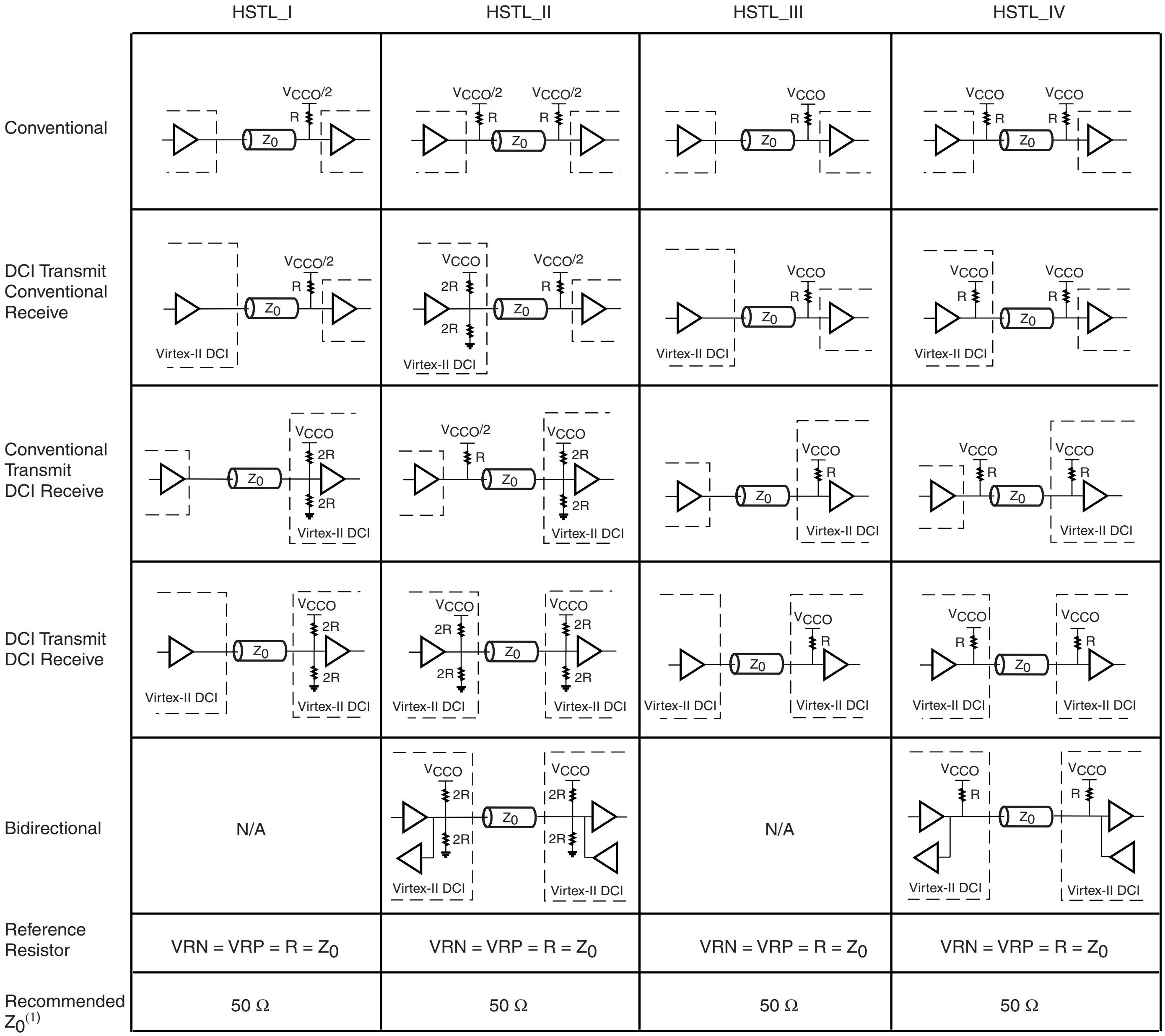
I/O Standard Description	IOSTANDARD Attribute	
	External Termination	On-Chip Termination
SSTL3 Class I	SSTL3_I	SSTL3_I_DCI[1]
SSTL3 Class II	SSTL3_II	SSTL3_II_DCI[1]
SSTL2 Class I	SSTL2_I	SSTL2_I_DCI[1]
SSTL2 Class II	SSTL2_II	SSTL2_II_DCI[1]
HSTL Class I	HSTL_I	HSTL_I_DCI
HSTL Class II	HSTL_II	HSTL_II_DCI
HSTL Class III	HSTL_III	HSTL_III_DCI
HSTL Class IV	HSTL_IV	HSTL_IV_DCI
GTL	GTL	GTL_DCI
GTLP	GTLP	GTLP_DCI

Notes:
1. SSTL-compatible

Table 8: **SelectI/O-Ultra Differential Buffers With On-Chip Termination**

I/O Standard Description	IOSTANDARD Attribute	
	External Termination	**On-Chip Termination**
LVDS 2.5V	LVDS_25	LVDS_25_DCI
LVDS Extended 2.5V	LVDSEXT_25	LVDSEXT_25_DCI

Figure 11 provides examples illustrating the use of the HSTL_I_DCI, HSTL_II_DCI, HSTL_III_DCI, and HSTL_IV_DCI I/O standards. For a complete list, see the **Virtex-II Platform FPGA User Guide**.



DS031_65a_100201

Note:

1. Z_0 is the recommended PCB trace impedance.

Figure 11: **HSTL DCI Usage Examples**

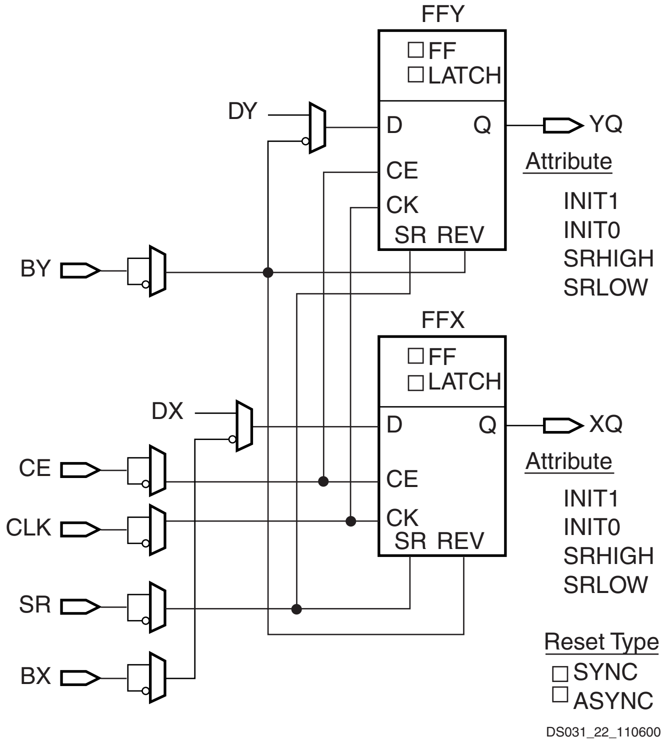


Figure 17: **Register / Latch Configuration in a Slice**

The set and reset functionality of a register or a latch can be configured as follows:

- No set or reset
- Synchronous set
- Synchronous reset
- Synchronous set and reset
- Asynchronous set (preset)
- Asynchronous reset (clear)
- Asynchronous set and reset (preset and clear)

The synchronous reset has precedence over a set, and an asynchronous clear has precedence over a preset.

Distributed SelectRAM Memory

Each function generator (LUT) can implement a 16 x 1-bit synchronous RAM resource called a distributed SelectRAM element. The SelectRAM elements are configurable within a CLB to implement the following:

- Single-Port 16 x 8 bit RAM
- Single-Port 32 x 4 bit RAM
- Single-Port 64 x 2 bit RAM
- Single-Port 128 x 1 bit RAM
- Dual-Port 16 x 4 bit RAM
- Dual-Port 32 x 2 bit RAM
- Dual-Port 64 x 1 bit RAM

Distributed SelectRAM memory modules are synchronous (write) resources. The combinatorial read access time is extremely fast, while the synchronous write simplifies high-speed designs. A synchronous read can be implemented with a storage element in the same slice. The distributed SelectRAM memory and the storage element share the same clock input. A Write Enable (WE) input is active High, and is driven by the SR input.

Table 9 shows the number of LUTs (2 per slice) occupied by each distributed SelectRAM configuration.

Table 9: **Distributed SelectRAM Configurations**

RAM	Number of LUTs
16 x 1S	1
16 x 1D	2
32 x 1S	2
32 x 1D	4
64 x 1S	4
64 x 1D	8
128 x 1S	8

Notes:

1. S = single-port configuration; D = dual-port configuration

For single-port configurations, distributed SelectRAM memory has one address port for synchronous writes and asynchronous reads.

For dual-port configurations, distributed SelectRAM memory has one port for synchronous writes and asynchronous reads and another port for asynchronous reads. The function generator (LUT) has separated read address inputs (A1, A2, A3, A4) and write address inputs (WG1/WF1, WG2/WF2, WG3/WF3, WG4/WF4).

In single-port mode, read and write addresses share the same address bus. In dual-port mode, one function generator (R/W port) is connected with shared read and write addresses. The second function generator has the A inputs (read) connected to the second read-only port address and the W inputs (write) shared with the first read/write port address.

Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. (See ***Virtex-II Platform FPGA User Guide*** for details.) The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setup shown in Figure 1.

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. (IBIS models can be found on the web at **http://support.xilinx.com/support/sw_ibis.htm**.) Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 19.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. The increase or decrease in delay should be added to or subtracted from the I/O Output Standard Adjustment value (Table 17) to yield the actual worst-case propagation delay (clock-to-input) of the PCB trace.

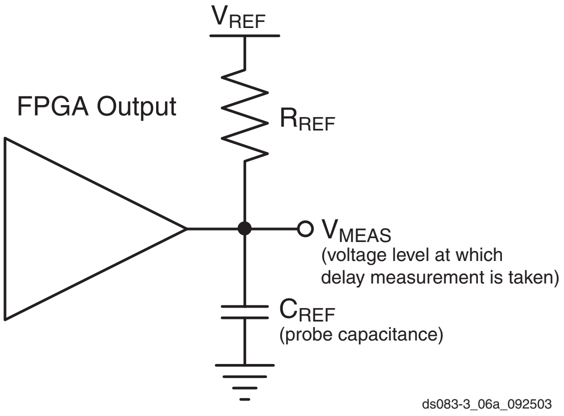


Figure 1: **Generalized Test Setup**

Table 19: **Output Delay Measurement Methodology**

Description	IOSTANDARD Attribute	R_{REF} (Ω)	C_{REF}[(1)] (pF)	V_{MEAS} (V)	V_{REF} (V)
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL (all)	1M	0	1.4	0
LVCMOS (Low-Voltage CMOS), 3.3V	LVCMOS33	1M	0	1.65	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3 (rising edge)	25	10(2)	0.94	0
	PCI33_3 (falling edge)	25	10(2)	2.03	3.3
PCI, 66 MHz, 3.3V	PCI66_3 (rising edge)	25	10(2)	0.94	0
	PCI66_3 (falling edge)	25	10(2)	2.03	3.3
PCI-X, 133 MHz, 3.3V	PCIX (rising edge)	25	10(3)	0.94	
	PCIX (falling edge	25	10(3)	2.03	3.3
GTL (Gunning Transceiver Logic)	GTL	25	0	0.8	1.2
GTL Plus	GTLP	25	0	1.0	1.5
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class III	HSTL_III	50	0	0.9	1.5
HSTL, Class IV	HSTL_IV	25	0	0.9	1.5
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSTL, Class III, 1.8V	HSTL_III_18	50	0	1.1	1.8
HSTL, Class IV, 1.8V	HSTL_IV_18	25	0	1.1	1.8

Table 3: **Virtex-II Device/Package Combinations and Maximum Number of Available I/Os**

Package	Available I/Os										
	XC2V 40	**XC2V 80**	**XC2V 250**	**XC2V 500**	**XC2V 1000**	**XC2V 1500**	**XC2V 2000**	**XC2V 3000**	**XC2V 4000**	**XC2V 6000**	**XC2V 8000**
CS144	88	92	92	-	-	-	-	-	-	-	-
FG256	88	120	172	172	172	-	-	-	-	-	-
FG456	-	-	200	264	324	-	-	-	-	-	-
FG676	-	-	-	-	-	392	456	484	-	-	-
FF896	-	-	-	-	432	528	624	-	-	-	-
FF1152	-	-	-	-	-	-	-	720	824	824	824
FF1517	-	-	-	-	-	-	-	-	912	1,104	1,108
BG575	-	-	-	-	328	392	408	-	-	-	-
BG728	-	-	-	-	-	-	-	516	-	-	-
BF957	-	-	-	-	-	-	624	684	684	684	-

Virtex-II Pin Definitions

This section describes the pinouts for Virtex-II devices in the following packages:

- CS144: wire-bond chip-scale ball grid array (BGA) of 0.80 mm pitch
- FG256, FG456, and FG676: wire-bond fine-pitch BGA of 1.00 mm pitch
- FF896, FF1152, FF1517: flip-chip fine-pitch BGA of 1.00 mm pitch
- BG575 and BG728: wire-bond BGA of 1.27 mm pitch
- BF957: flip-chip BGA of 1.27 mm pitch

All of the devices supported in a particular package are pinout compatible and are listed in the same table (one table per package). In addition, the FG456 and FG676 packages are compatible, as are the FF896 and FF1152 packages. Pins that are not available for the smallest devices are listed in right-hand columns.

Each device is split into eight I/O banks to allow for flexibility in the choice of I/O standards (see the Virtex-II *Data Sheet*). Global pins, including JTAG, configuration, and power/ground pins, are listed at the end of each table. Table 4 provides definitions for all pin types.

The FG256 pinouts (Table 6) is included as an example. All Virtex-II pinout tables are available on the distribution CD-ROM, or on the web (at **http://www.xilinx.com**).

Table 6: **FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
1	IO_L92P_1	E11	NC	NC
1	IO_L05N_1	A11	NC	NC
1	IO_L05P_1	B11	NC	NC
1	IO_L04N_1	C11	NC	NC
1	IO_L04P_1/VREF_1	D11	NC	NC
1	IO_L03N_1/VRP_1	A12		
1	IO_L03P_1/VRN_1	B12		
1	IO_L02N_1	C12		
1	IO_L02P_1	D12		
1	IO_L01N_1	B13		
1	IO_L01P_1	C13		
2	IO_L01N_2	C16		
2	IO_L01P_2	D16		
2	IO_L02N_2/VRP_2	D14		
2	IO_L02P_2/VRN_2	D15		
2	IO_L03N_2	E13		
2	IO_L03P_2/VREF_2	E14		
2	IO_L04N_2	E15	NC	
2	IO_L04P_2	E16	NC	
2	IO_L06N_2	F13	NC	
2	IO_L06P_2	F14	NC	
2	IO_L43N_2	F15	NC	NC
2	IO_L43P_2	F16	NC	NC
2	IO_L45N_2	F12	NC	NC
2	IO_L45P_2/VREF_2	G12	NC	NC
2	IO_L91N_2	G13	NC	
2	IO_L91P_2	G14	NC	
2	IO_L93N_2	G15	NC	
2	IO_L93P_2/VREF_2	G16	NC	
2	IO_L94N_2	H13		
2	IO_L94P_2	H14		
2	IO_L96N_2	H15		
2	IO_L96P_2	H16		

Table 6: **FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
4	IO_L91N_4/VREF_4	R11	NC	NC
4	IO_L91P_4	T11	NC	NC
4	IO_L92N_4	M11	NC	NC
4	IO_L92P_4	M10	NC	NC
4	IO_L93N_4	N10	NC	NC
4	IO_L93P_4	P10	NC	NC
4	IO_L94N_4/VREF_4	R10		
4	IO_L94P_4	T10		
4	IO_L95N_4/GCLK3S	N9		
4	IO_L95P_4/GCLK2P	P9		
4	IO_L96N_4/GCLK1S	R9		
4	IO_L96P_4/GCLK0P	T9		
5	IO_L96N_5/GCLK7S	T8		
5	IO_L96P_5/GCLK6P	R8		
5	IO_L95N_5/GCLK5S	P8		
5	IO_L95P_5/GCLK4P	N8		
5	IO_L94N_5	T7		
5	IO_L94P_5/VREF_5	R7		
5	IO_L93N_5	P7	NC	NC
5	IO_L93P_5	N7	NC	NC
5	IO_L92N_5	M7	NC	NC
5	IO_L92P_5	M6	NC	NC
5	IO_L91N_5	T6	NC	NC
5	IO_L91P_5/VREF_5	R6	NC	NC
5	IO_L05N_5/VRP_5	P6	NC	NC
5	IO_L05P_5/VRN_5	N6	NC	NC
5	IO_L04N_5	T5	NC	NC
5	IO_L04P_5/VREF_5	R5	NC	NC
5	IO_L03N_5/D4/ALT_VRP_5	P5		
5	IO_L03P_5/D5/ALT_VRN_5	N5		
5	IO_L02N_5/D6	R4		
5	IO_L02P_5/D7	P4		
5	IO_L01N_5/RDWR_B	T4		

Table 6: **FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
7	IO_L45N_7	F5	NC	NC
7	IO_L43P_7	F1	NC	NC
7	IO_L43N_7	F2	NC	NC
7	IO_L06P_7	F3	NC	
7	IO_L06N_7	F4	NC	
7	IO_L04P_7	E1	NC	
7	IO_L04N_7	E2	NC	
7	IO_L03P_7/VREF_7	E3		
7	IO_L03N_7	E4		
7	IO_L02P_7/VRN_7	D2		
7	IO_L02N_7/VRP_7	D3		
7	IO_L01P_7	D1		
7	IO_L01N_7	C1		
0	VCCO_0	F8		
0	VCCO_0	F7		
0	VCCO_0	E8		
1	VCCO_1	F10		
1	VCCO_1	F9		
1	VCCO_1	E9		
2	VCCO_2	H12		
2	VCCO_2	H11		
2	VCCO_2	G11		
3	VCCO_3	K11		
3	VCCO_3	J12		
3	VCCO_3	J11		
4	VCCO_4	M9		
4	VCCO_4	L10		
4	VCCO_4	L9		
5	VCCO_5	M8		
5	VCCO_5	L8		
5	VCCO_5	L7		
6	VCCO_6	K6		
6	VCCO_6	J6		

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
0	VCCO_0	F7		
1	VCCO_1	G14		
1	VCCO_1	G13		
1	VCCO_1	G12		
1	VCCO_1	F16		
1	VCCO_1	F15		
2	VCCO_2	L16		
2	VCCO_2	K16		
2	VCCO_2	J16		
2	VCCO_2	H17		
2	VCCO_2	G17		
3	VCCO_3	T17		
3	VCCO_3	R17		
3	VCCO_3	P16		
3	VCCO_3	N16		
3	VCCO_3	M16		
4	VCCO_4	U16		
4	VCCO_4	U15		
4	VCCO_4	T14		
4	VCCO_4	T13		
4	VCCO_4	T12		
5	VCCO_5	U8		
5	VCCO_5	U7		
5	VCCO_5	T11		
5	VCCO_5	T10		
5	VCCO_5	T9		
6	VCCO_6	T6		
6	VCCO_6	R6		
6	VCCO_6	P7		
6	VCCO_6	N7		
6	VCCO_6	M7		
7	VCCO_7	L7		
7	VCCO_7	K7		
7	VCCO_7	J7		

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
NA	GND	M10		
NA	GND	M9		
NA	GND	L14		
NA	GND	L13		
NA	GND	L12		
NA	GND	L11		
NA	GND	L10		
NA	GND	L9		
NA	GND	K14		
NA	GND	K13		
NA	GND	K12		
NA	GND	K11		
NA	GND	K10		
NA	GND	K9		
NA	GND	J14		
NA	GND	J13		
NA	GND	J12		
NA	GND	J11		
NA	GND	J10		
NA	GND	J9		
NA	GND	D19		
NA	GND	D4		
NA	GND	C20		
NA	GND	C3		
NA	GND	B21		
NA	GND	B2		
NA	GND	A22		
NA	GND	A1		

Notes:

1. See Table 4 for an explanation of the signals available on this pin.

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
7	IO_L78N_7	M2	NC	
7	IO_L76P_7	M5	NC	
7	IO_L76N_7	M6	NC	
7	IO_L75P_7/VREF_7	M3	NC	
7	IO_L75N_7	M4	NC	
7	IO_L73P_7	M7	NC	
7	IO_L73N_7	M8	NC	
7	IO_L72P_7	L1		
7	IO_L72N_7	L2		
7	IO_L70P_7	L5		
7	IO_L70N_7	L6		
7	IO_L69P_7/VREF_7	L3		
7	IO_L69N_7	L4		
7	IO_L67P_7	K1		
7	IO_L67N_7	J1		
7	IO_L54P_7	K3		
7	IO_L54N_7	K4		
7	IO_L52P_7	K5		
7	IO_L52N_7	K6		
7	IO_L51P_7/VREF_7	L8		
7	IO_L51N_7	L7		
7	IO_L49P_7	J2		
7	IO_L49N_7	H1		
7	IO_L48P_7	J3		
7	IO_L48N_7	J4		
7	IO_L46P_7	J5		
7	IO_L46N_7	J6		
7	IO_L45P_7/VREF_7	H5		
7	IO_L45N_7	H4		
7	IO_L43P_7	K7		
7	IO_L43N_7	J7		
7	IO_L25P_7	H2	NC	NC
7	IO_L25N_7	H3	NC	NC
7	IO_L24P_7	G1		
7	IO_L24N_7	F1		
7	IO_L22P_7	G3		
7	IO_L22N_7	G4		

BG575/BGG575 Standard BGA Package

As shown in Table 9, XC2V1000, XC2V1500, and XC2V2000 Virtex-II devices are available in the BG575/BGG575 BGA package. Pins in the XC2V1000, XC2V1500, and XC2V2000 devices are the same, except for the pin differences in the XC2V1000 and XC2V1500 devices shown in the No Connect columns. Following this table are the BG575/BGG575 Standard BGA Package Specifications (1.27mm pitch).

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
0	IO_L01N_0	A3		
0	IO_L01P_0	A4		
0	IO_L02N_0	D5		
0	IO_L02P_0	C5		
0	IO_L03N_0/VRP_0	E6		
0	IO_L03P_0/VRN_0	D6		
0	IO_L04N_0/VREF_0	F7		
0	IO_L04P_0	E7		
0	IO_L05N_0	G8		
0	IO_L05P_0	H9		
0	IO_L06N_0	A5		
0	IO_L06P_0	A6		
0	IO_L19N_0	B5		
0	IO_L19P_0	B6		
0	IO_L21N_0	D7		
0	IO_L21P_0/VREF_0	C7		
0	IO_L22N_0	F8		
0	IO_L22P_0	E8		
0	IO_L24N_0	G9		
0	IO_L24P_0	F9		
0	IO_L49N_0	G10		
0	IO_L49P_0	H10		
0	IO_L51N_0	B7		
0	IO_L51P_0/VREF_0	B8		
0	IO_L52N_0	D8		
0	IO_L52P_0	C8		
0	IO_L54N_0	E9		
0	IO_L54P_0	D9		
0	IO_L67N_0	A8	NC	
0	IO_L67P_0	A9	NC	
0	IO_L69N_0	C9	NC	

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
5	IO_L52N_5	AA9		
5	IO_L52P_5	Y9		
5	IO_L51N_5/VREF_5	W9		
5	IO_L51P_5	V9		
5	IO_L49N_5	AD8		
5	IO_L49P_5	AD6		
5	IO_L24N_5	AC8		
5	IO_L24P_5	AC7		
5	IO_L22N_5	AB8		
5	IO_L22P_5	AA8		
5	IO_L21N_5/VREF_5	W8		
5	IO_L21P_5	Y8		
5	IO_L19N_5	AD5		
5	IO_L19P_5	AD4		
5	IO_L06N_5	AC6		
5	IO_L06P_5	AC5		
5	IO_L05N_5/VRP_5	AB7		
5	IO_L05P_5/VRN_5	AA7		
5	IO_L04N_5	AB5		
5	IO_L04P_5/VREF_5	AA5		
5	IO_L03N_5/D4/ALT_VRP_5	AA6		
5	IO_L03P_5/D5/ALT_VRN_5	Y6		
5	IO_L02N_5/D6	Y7		
5	IO_L02P_5/D7	W7		
5	IO_L01N_5/RDWR_B	V8		
5	IO_L01P_5/CS_B	U9		
6	IO_L01P_6	AB2		
6	IO_L01N_6	AB1		
6	IO_L02P_6/VRN_6	AA3		
6	IO_L02N_6/VRP_6	AA2		
6	IO_L03P_6	Y4		
6	IO_L03N_6/VREF_6	Y3		
6	IO_L04P_6	W4		
6	IO_L04N_6	W5		
6	IO_L06P_6	V5		

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
NA	GND	Y5		
NA	GND	W19		
NA	GND	W6		
NA	GND	V24		
NA	GND	V18		
NA	GND	V7		
NA	GND	V1		
NA	GND	R21		
NA	GND	R4		
NA	GND	P14		
NA	GND	P13		
NA	GND	P12		
NA	GND	P11		
NA	GND	N14		
NA	GND	N13		
NA	GND	N12		
NA	GND	N11		
NA	GND	M14		
NA	GND	M13		
NA	GND	M12		
NA	GND	M11		
NA	GND	L14		
NA	GND	L13		
NA	GND	L12		
NA	GND	L11		
NA	GND	K21		
NA	GND	K4		
NA	GND	G24		
NA	GND	G18		
NA	GND	G7		
NA	GND	G1		
NA	GND	F19		
NA	GND	F6		
NA	GND	E20		
NA	GND	E5		
NA	GND	D21		

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
2	IO_L70P_2	N19
2	IO_L72N_2	M22
2	IO_L72P_2	M23
2	IO_L73N_2	M24
2	IO_L73P_2	N24
2	IO_L75N_2	M26
2	IO_L75P_2/VREF_2	M27
2	IO_L76N_2	N20
2	IO_L76P_2	N21
2	IO_L78N_2	N22
2	IO_L78P_2	N23
2	IO_L91N_2	N25
2	IO_L91P_2	P25
2	IO_L93N_2	N26
2	IO_L93P_2/VREF_2	N27
2	IO_L94N_2	P20
2	IO_L94P_2	P21
2	IO_L96N_2	P22
2	IO_L96P_2	P23
3	IO_L96N_3	R27
3	IO_L96P_3	R26
3	IO_L94N_3	R25
3	IO_L94P_3	R24
3	IO_L93N_3/VREF_3	R23
3	IO_L93P_3	T23
3	IO_L91N_3	R22
3	IO_L91P_3	R21
3	IO_L78N_3	R20
3	IO_L78P_3	R19
3	IO_L76N_3	T27
3	IO_L76P_3	T26
3	IO_L75N_3/VREF_3	T24
3	IO_L75P_3	U24
3	IO_L73N_3	T22
3	IO_L73P_3	U22

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
NA	GND	AC1		
NA	GND	AA28		
NA	GND	AA3		
NA	GND	W26		
NA	GND	W19		
NA	GND	W18		
NA	GND	W17		
NA	GND	W16		
NA	GND	W15		
NA	GND	W14		
NA	GND	W13		
NA	GND	W12		
NA	GND	W5		
NA	GND	V19		
NA	GND	V18		
NA	GND	V17		
NA	GND	V16		
NA	GND	V15		
NA	GND	V14		
NA	GND	V13		
NA	GND	V12		
NA	GND	U24		
NA	GND	U19		
NA	GND	U18		
NA	GND	U17		
NA	GND	U16		
NA	GND	U15		
NA	GND	U14		
NA	GND	U13		
NA	GND	U12		
NA	GND	U7		
NA	GND	T19		
NA	GND	T18		
NA	GND	T17		
NA	GND	T16		
NA	GND	T15		
NA	GND	T14		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
3	IO_L34N_3	AH6	NC	
3	IO_L34P_3	AJ6	NC	
3	IO_L33N_3/VREF_3	AJ8	NC	
3	IO_L33P_3	AH8	NC	
3	IO_L32N_3	AL1	NC	
3	IO_L32P_3	AM1	NC	
3	IO_L31N_3	AH7	NC	
3	IO_L31P_3	AJ7	NC	
3	IO_L30N_3	AH10		
3	IO_L30P_3	AG10		
3	IO_L29N_3	AK3		
3	IO_L29P_3	AL3		
3	IO_L28N_3	AK4		
3	IO_L28P_3	AL4		
3	IO_L27N_3/VREF_3	AJ9		
3	IO_L27P_3	AH9		
3	IO_L26N_3	AM2		
3	IO_L26P_3	AN2		
3	IO_L25N_3	AK5		
3	IO_L25P_3	AL5		
3	IO_L24N_3	AK9		
3	IO_L24P_3	AK8		
3	IO_L23N_3	AN1		
3	IO_L23P_3	AP1		
3	IO_L22N_3	AK6		
3	IO_L22P_3	AL6		
3	IO_L21N_3/VREF_3	AH12		
3	IO_L21P_3	AG12		
3	IO_L20N_3	AM3		
3	IO_L20P_3	AN3		
3	IO_L19N_3	AM4		
3	IO_L19P_3	AN4		
3	IO_L12N_3	AJ12	NC	
3	IO_L12P_3	AH11	NC	
3	IO_L11N_3	AP2	NC	
3	IO_L11P_3	AR2	NC	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
4	IO_L08P_4	AL12	NC	
4	IO_L09N_4	AP9	NC	
4	IO_L09P_4/VREF_4	AP8	NC	
4	IO_L10N_4	AV6	NC	
4	IO_L10P_4	AV5	NC	
4	IO_L11N_4	AM11	NC	
4	IO_L11P_4	AM12	NC	
4	IO_L12N_4	AN10	NC	
4	IO_L12P_4	AN9	NC	
4	IO_L19N_4	AU8		
4	IO_L19P_4	AU7		
4	IO_L20N_4	AH14		
4	IO_L20P_4	AH15		
4	IO_L21N_4	AT8		
4	IO_L21P_4/VREF_4	AT7		
4	IO_L22N_4	AW7		
4	IO_L22P_4	AW6		
4	IO_L23N_4	AK13		
4	IO_L23P_4	AK14		
4	IO_L24N_4	AR10		
4	IO_L24P_4	AR9		
4	IO_L25N_4	AV8		
4	IO_L25P_4	AV7		
4	IO_L26N_4	AJ14		
4	IO_L26P_4	AJ15		
4	IO_L27N_4	AP11		
4	IO_L27P_4/VREF_4	AP10		
4	IO_L28N_4	AU10		
4	IO_L28P_4	AU9		
4	IO_L29N_4	AL13		
4	IO_L29P_4	AL14		
4	IO_L30N_4	AN12		
4	IO_L30P_4	AN11		
4	IO_L31N_4	AW9	NC	
4	IO_L31P_4	AW8	NC	
4	IO_L32N_4	AM13	NC	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
6	IO_L47N_6	AJ39		
6	IO_L48P_6	AG35		
6	IO_L48N_6	AH35		
6	IO_L49P_6	AG32		
6	IO_L49N_6	AF32		
6	IO_L50P_6	AH37		
6	IO_L50N_6	AG37		
6	IO_L51P_6	AD29		
6	IO_L51N_6/VREF_6	AE29		
6	IO_L52P_6	AD28		
6	IO_L52N_6	AC28		
6	IO_L53P_6	AH38		
6	IO_L53N_6	AG38		
6	IO_L54P_6	AF34		
6	IO_L54N_6	AG34		
6	IO_L55P_6	AE32		
6	IO_L55N_6	AD32		
6	IO_L56P_6	AH39		
6	IO_L56N_6	AG39		
6	IO_L57P_6	AE33		
6	IO_L57N_6/VREF_6	AF33		
6	IO_L58P_6	AD30		
6	IO_L58N_6	AC30		
6	IO_L59P_6	AF37		
6	IO_L59N_6	AE37		
6	IO_L60P_6	AF36		
6	IO_L60N_6	AG36		
6	IO_L67P_6	AD31		
6	IO_L67N_6	AC31		
6	IO_L68P_6	AE34		
6	IO_L68N_6	AD34		
6	IO_L69P_6	AD35		
6	IO_L69N_6/VREF_6	AE35		
6	IO_L70P_6	AB28		
6	IO_L70N_6	AA28		
6	IO_L71P_6	AF39		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
7	IO_L02P_7/VRN_7	M27		
7	IO_L02N_7/VRP_7	L27		
7	IO_L01P_7	D38		
7	IO_L01N_7	E37		
0	VCCO_0	P25		
0	VCCO_0	P24		
0	VCCO_0	P23		
0	VCCO_0	P22		
0	VCCO_0	P21		
0	VCCO_0	N26		
0	VCCO_0	N25		
0	VCCO_0	N24		
0	VCCO_0	N23		
0	VCCO_0	N22		
0	VCCO_0	N21		
0	VCCO_0	L23		
0	VCCO_0	J25		
0	VCCO_0	G27		
0	VCCO_0	E29		
0	VCCO_0	C22		
0	VCCO_0	B26		
1	VCCO_1	P19		
1	VCCO_1	P18		
1	VCCO_1	P17		
1	VCCO_1	P16		
1	VCCO_1	P15		
1	VCCO_1	N19		
1	VCCO_1	N18		
1	VCCO_1	N17		
1	VCCO_1	N16		
1	VCCO_1	N15		
1	VCCO_1	N14		
1	VCCO_1	L17		
1	VCCO_1	J15		
1	VCCO_1	G13		