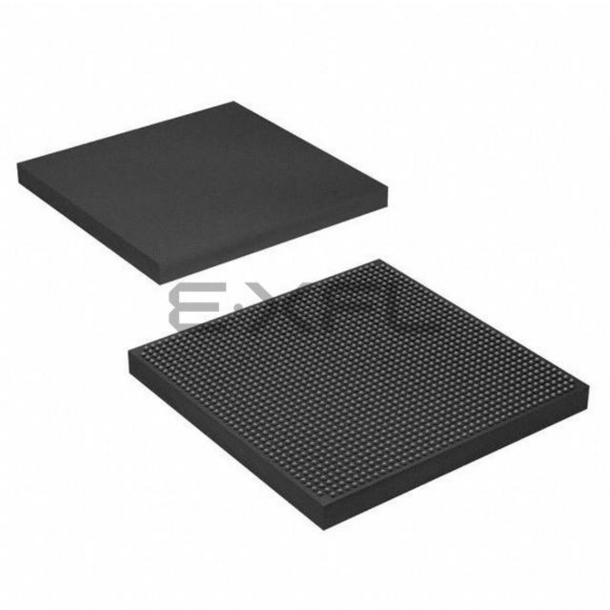

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	8448
Number of Logic Elements/Cells	-
Total RAM Bits	2654208
Number of I/O	1104
Number of Gates	6000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FCBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v6000-4ffg1517c

Virtex-II Platform FPGAs: Functional Description

DS031-2 (v3.5) November 5, 2007 **Product Specification**

Detailed Description

Input/Output Blocks (IOBs)

Virtex-II™ I/O blocks (IOBs) are provided in groups of two or four on the perimeter of each device. Each IOB can be used as input and/or output for single-ended I/Os. Two IOBs can be used as a differential pair. A differential pair is always connected to the same switch matrix, as shown in Figure 1.

IOB blocks are designed for high performances I/Os, supporting 19 single-ended standards, as well as differential signaling with LVDS, LDT, Bus LVDS, and LVPECL.

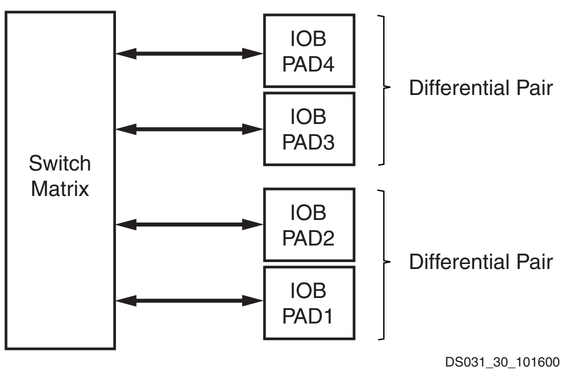

Figure 1: **Virtex-II Input/Output Tile**

Note: Differential I/Os must use the same clock.

Supported I/O Standards

Virtex-II IOB blocks feature SelectI/O-Ultra inputs and outputs that support a wide variety of I/O signaling standards. In addition to the internal supply voltage (V_{CCINT} = 1.5V), output driver supply voltage (V_{CCO}) is dependent on the I/O standard (see Table 1 and Table 2). An auxiliary supply voltage (V_{CCAUX} = 3.3 V) is required, regardless of the I/O standard used. For exact supply voltage absolute maximum ratings, see DC Input and Output Levels in Module 3.

All of the user IOBs have fixed-clamp diodes to V_{CCO} and to ground. As outputs, these IOBs are not compatible or compliant with 5V I/O standards. As inputs, these IOBs are not normally 5V tolerant, but can be used with 5V I/O standards when external current-limiting resistors are used. For more details, see the "5V Tolerant I/Os" Tech Topic at **www.xilinx.com**.

Table 3 lists supported I/O standards with Digitally Controlled Impedance. See Digitally Controlled Impedance (DCI), page 8.

Table 1: **Supported Single-Ended I/O Standards**

IOSTANDARD Attribute	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Board Termination Voltage (V_{TT})
LVTTL	3.3	3.3	N/R(3)	N/R
LVCMOS33	3.3	3.3	N/R	N/R
LVCMOS25	2.5	2.5	N/R	N/R
LVCMOS18	1.8	1.8	N/R	N/R
LVCMOS15	1.5	1.5	N/R	N/R
PCI33_3	3.3	3.3	N/R	N/R
PCI66_3	3.3	3.3	N/R	N/R
PCI-X	3.3	3.3	N/R	N/R
GTL	Note (1)	Note (1)	0.8	1.2
GTLP	Note (1)	Note (1)	1.0	1.5
HSTL_I	1.5	N/R	0.75	0.75
HSTL_II	1.5	N/R	0.75	0.75
HSTL_III	1.5	N/R	0.9	1.5
HSTL_IV	1.5	N/R	0.9	1.5
HSTL_I_18	1.8	N/R	0.9	0.9
HSTL_II_18	1.8	N/R	0.9	0.9
HSTL_III _18	1.8	N/R	1.1	1.8
HSTL_IV_18	1.8	N/R	1.1	1.8
SSTL18_I(2)	1.8	N/R	0.9	0.9
SSTL18_II	1.8	N/R	0.9	0.9
SSTL2_I	2.5	N/R	1.25	1.25
SSTL2_II	2.5	N/R	1.25	1.25
SSTL3_I	3.3	N/R	1.5	1.5
SSTL3_II	3.3	N/R	1.5	1.5
AGP-2X/AGP	3.3	N/R	1.32	N/R

Notes:

1. V_{CCO} of GTL or GTLP should not be lower than the termination voltage or the voltage seen at the I/O pad. Example: If the pin High level is 1.5V, connect V_{CCO} to 1.5V.
2. SSTL18_I is not a JEDEC-supported standard.
3. N/R = no requirement.

Table 4: **LVTTL and LVCMOS Programmable Currents (Sink and Source)**

SelectI/O-Ultra	Programmable Current (Worst-Case Guaranteed Minimum)						
LVTTL	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA
LVCMOS33	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA
LVCMOS25	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA
LVCMOS18	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	n/a
LVCMOS15	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	n/a

Figure 6 shows the SSTL2, SSTL3, and HSTL configurations. HSTL can sink current up to 48 mA. (HSTL IV)

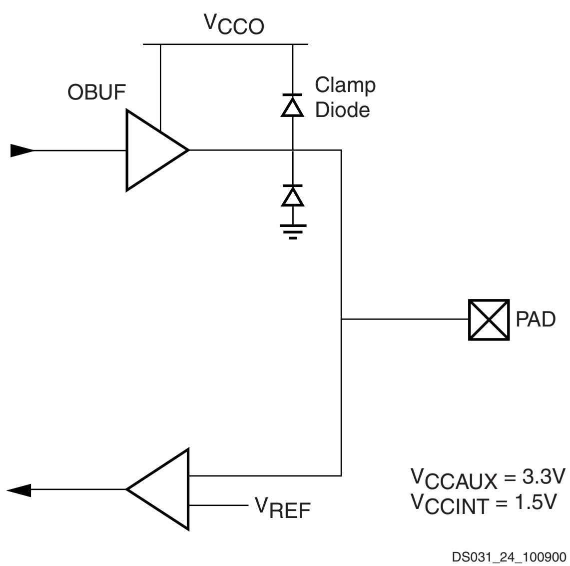

Figure 6: **SSTL or HSTL SelectI/O-Ultra Standards**

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. Virtex-II uses two memory cells to control the configuration of an I/O as an input. This is to reduce the probability of an I/O configured as an input from flipping to an output when subjected to a single event upset (SEU) in space applications.

Prior to configuration, all outputs not involved in configuration are forced into their high-impedance state. The pull-down resistors and the weak-keeper circuits are inactive. The dedicated pin HSWAP_EN controls the pull-up resistors prior to configuration. By default, HSWAP_EN is set high, which disables the pull-up resistors on user I/O pins. When HSWAP_EN is set low, the pull-up resistors are activated on user I/O pins.

All Virtex-II IOBs support IEEE 1149.1 compatible Boundary-Scan testing.

Input Path

The Virtex-II IOB input path routes input signals directly to internal logic and / or through an optional input flip-flop or latch, or through the DDR input registers. An optional delay element at the D-input of the storage element eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the Virtex-II device, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signaling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, V_{REF}. The need to supply V_{REF} imposes constraints on which standards can be used in the same bank. See I/O banking description.

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output and / or the 3-state signal can be routed to the buffer directly from the internal logic or through an output / 3-state flip-flop or latch, or through the DDR output / 3-state registers.

Each output driver can be individually programmed for a wide range of low-voltage signaling standards. In most signaling standards, the output High voltage depends on an externally supplied V_{CCO} voltage. The need to supply V_{CCO} imposes constraints on which standards can be used in the same bank. See I/O banking description.

I/O Banking

Some of the I/O standards described above require V_{CCO} and V_{REF} voltages. These voltages are externally supplied and connected to device pins that serve groups of IOB blocks, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from dividing each edge of the FPGA into two banks, as shown in Figure 7 and Figure 8. Each bank has multiple V_{CCO} pins, all of which must be connected to the same voltage. This voltage is determined by the output standards in use.

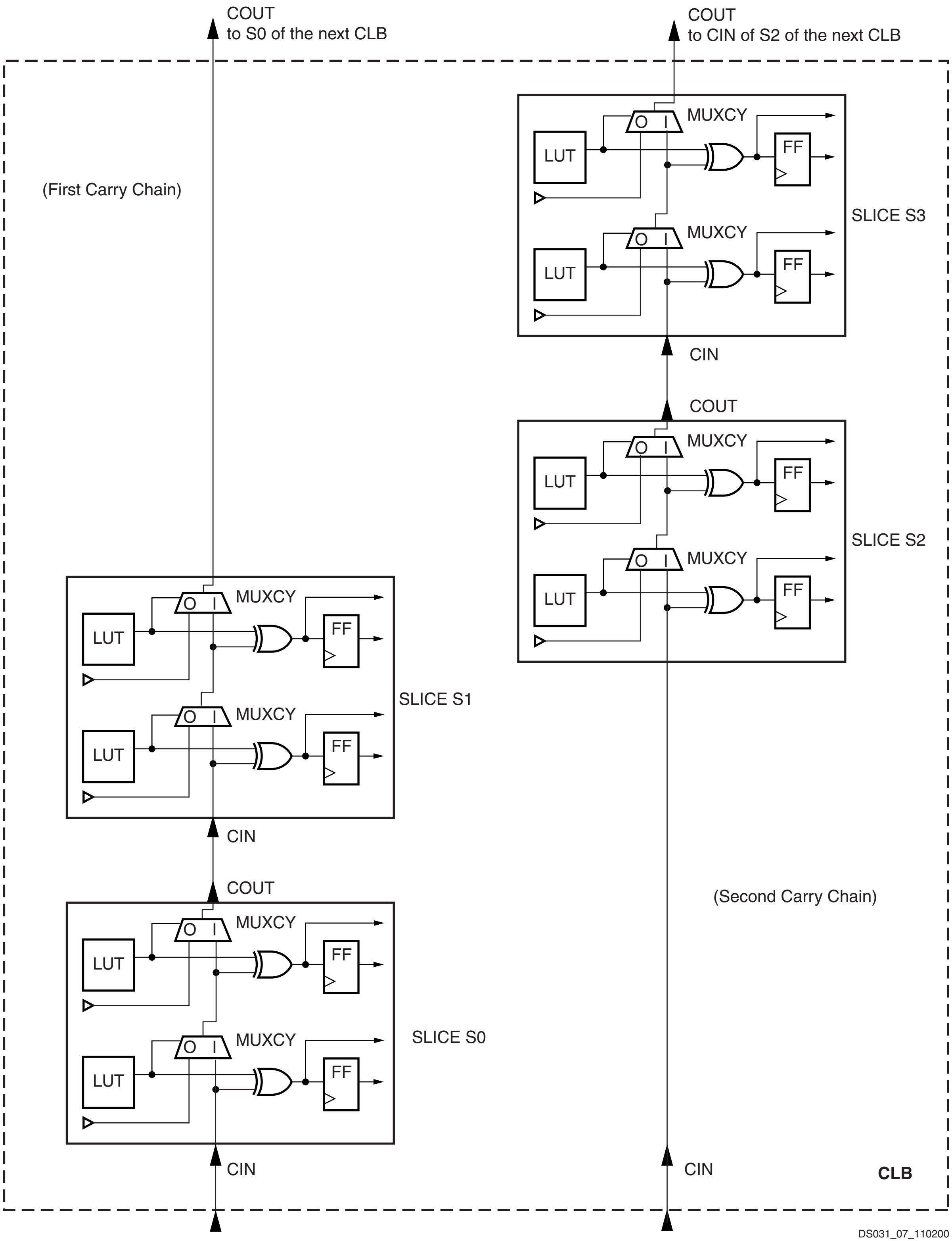

Figure 24: **Fast Carry Logic Path**

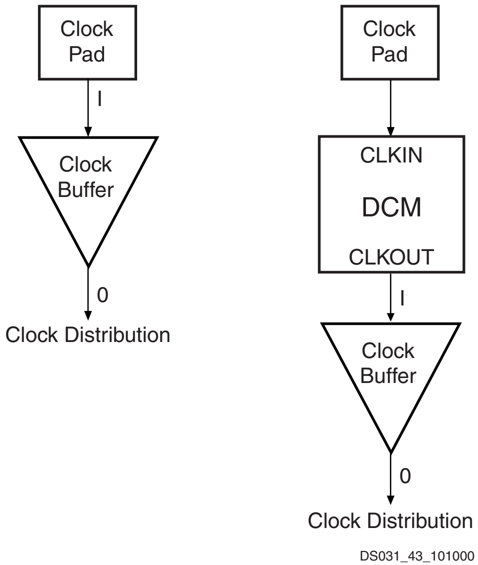

Figure 39: **Virtex-II Clock Distribution Configurations**

Global clock buffers are used to distribute the clock to some or all synchronous logic elements (such as registers in CLBs and IOBs, and SelectRAM blocks.

Eight global clocks can be used in each quadrant of the Virtex-II device. Designers should consider the clock distribution detail of the device prior to pin-locking and floorplanning (see the Virtex-II *User Guide*).

Figure 40 shows clock distribution in Virtex-II devices.

In each quadrant, up to eight clocks are organized in clock rows. A clock row supports up to 16 CLB rows (eight up and eight down). For the largest devices a new clock row is added, as necessary.

To reduce power consumption, any unused clock branches remain static.

Global clocks are driven by dedicated clock buffers (BUFG), which can also be used to gate the clock (BUFGCE) or to multiplex between two independent clock inputs (BUFGMUX).

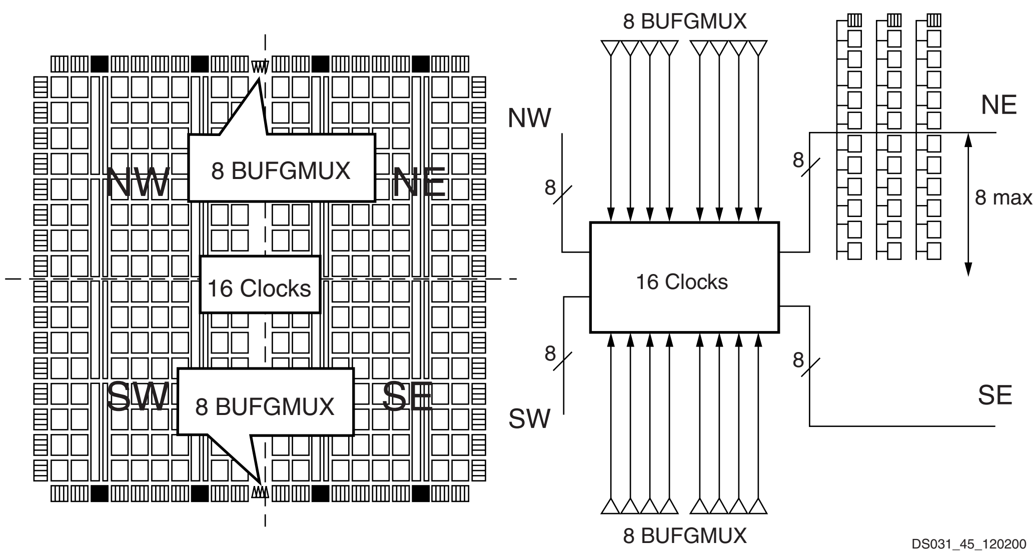

Figure 40: **Virtex-II Clock Distribution**

The most common configuration option of this element is as a buffer. A BUFG function in this (global buffer) mode, is shown in Figure 41.

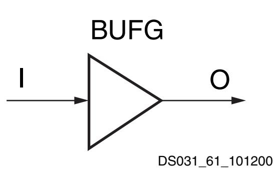

Figure 41: **Virtex-II BUFG Function**

The Virtex-II global clock buffer BUFG can also be configured as a clock enable/disable circuit (Figure 42), as well as a two-input clock multiplexer (Figure 43). A functional description of these two options is provided below. Each of them can be used in either of two modes, selected by configuration: rising clock edge or falling clock edge.

This section describes the rising clock edge option. For the opposite option, falling clock edge, just change all "rising" references to "falling" and all "High" references to "Low", except for the description of the CE or S levels. The rising clock edge option uses the BUFGCE and BUFGMUX primitives. The falling clock edge option uses the BUFGCE_1 and BUFGMUX_1 primitives.

BUFGCE

If the CE input is active (High) prior to the incoming rising clock edge, this Low-to-High-to-Low clock pulse passes through the clock buffer. Any level change of CE during the incoming clock High time has no effect.

Configuration Timing

Configuration Memory Clearing Parameters

Power-up timing of configuration signals is shown in Figure 2; corresponding timing characteristics are listed in Table 30.

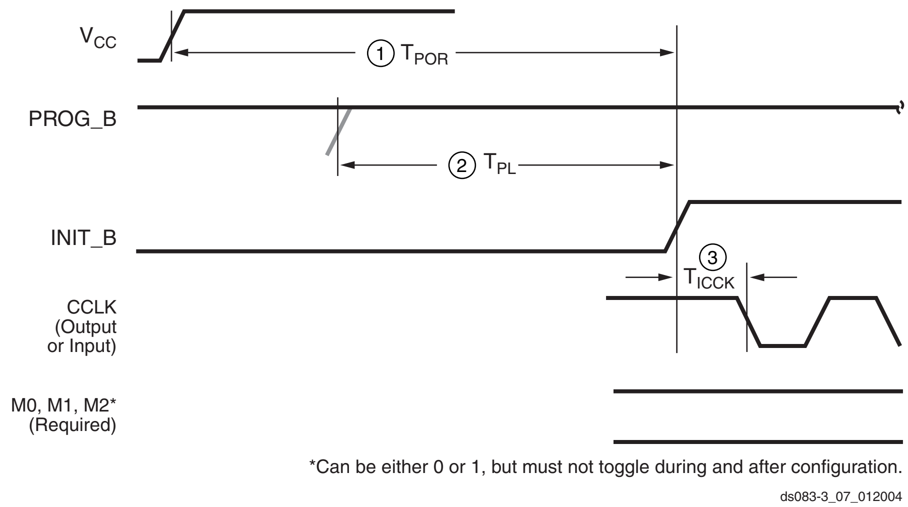

Figure 2: **Configuration Power-Up Timing**

Table 30: **Power-Up Timing Characteristics**

Description	Figure References	Symbol	Value	Units
Power-on reset	1	T_{POR}	$T_{PL} + 2$	ms, max
Program latency	2	T_{PL}	4	μs per frame, max
CCLK (output) delay	3	T_{ICCK}	0.5	μs, min
			4.0	μs, max
Program pulse width		$T_{PROGRAM}$	300	ns, min

Notes:
1. The M2, M1, and M0 mode pins should be set at a constant DC voltage level, either through pull-up or pull-down resistors, or tied directly to ground or V_{CCAUX}. The mode pins should not be toggled during and after configuration.

Master/Slave Serial Mode Parameters

Clock timing for Slave Serial configuration programming is shown in Figure 3, with Master Serial clock timing shown in Figure 4. Programming parameters for both Slave and Master modes are given in Table 31.

Global Clock Setup and Hold for LVTTL Standard, *Without* DCM

Table 37: **Global Clock Setup and Hold for LVTTL Standard, *Without* DCM**

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard.(2) For data input with different standards, adjust the setup time delay by the values shown in IOB Input Switching Characteristics Standard Adjustments, page 11.						
Full Delay Global Clock and IFF(1) without DCM	T_{PSFD}/T_{PHFD}	XC2V40	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V80	2.10/ 0.00	2.10/ 0.00	2.21/ 0.00	ns
		XC2V250	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V500	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V1000	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V1500	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V2000	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V3000	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V4000	2.00/ 0.00	2.00/ 0.00	2.30/ 0.00	ns
		XC2V6000	1.92/ 0.50	1.92/ 0.50	2.21/ 0.50	ns
		XC2V8000		2.38/ 0.00	2.60/ 0.00	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. These values are parametrically measured.

Table 6: **FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
6	VCCO_6	J5		
7	VCCO_7	H6		
7	VCCO_7	H5		
7	VCCO_7	G6		
NA	CCLK	P15		
NA	PROG_B	A2		
NA	DONE	R14		
NA	M0	T2		
NA	M1	P2		
NA	M2	R3		
NA	HSWAP_EN	B3		
NA	TCK	A15		
NA	TDI	C2		
NA	TDO	C15		
NA	TMS	B14		
NA	PWRDWN_B	T15		
NA	RSVD	A4		
NA	RSVD	A3		
NA	VBATT	A14		
NA	RSVD	A13		
NA	VCCAUX	R16		
NA	VCCAUX	R1		
NA	VCCAUX	B16		
NA	VCCAUX	B1		
NA	VCCINT	N13		
NA	VCCINT	N4		
NA	VCCINT	M12		
NA	VCCINT	M5		
NA	VCCINT	E12		
NA	VCCINT	E5		
NA	VCCINT	D13		
NA	VCCINT	D4		

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
0	VCCO_0	F7		
1	VCCO_1	G14		
1	VCCO_1	G13		
1	VCCO_1	G12		
1	VCCO_1	F16		
1	VCCO_1	F15		
2	VCCO_2	L16		
2	VCCO_2	K16		
2	VCCO_2	J16		
2	VCCO_2	H17		
2	VCCO_2	G17		
3	VCCO_3	T17		
3	VCCO_3	R17		
3	VCCO_3	P16		
3	VCCO_3	N16		
3	VCCO_3	M16		
4	VCCO_4	U16		
4	VCCO_4	U15		
4	VCCO_4	T14		
4	VCCO_4	T13		
4	VCCO_4	T12		
5	VCCO_5	U8		
5	VCCO_5	U7		
5	VCCO_5	T11		
5	VCCO_5	T10		
5	VCCO_5	T9		
6	VCCO_6	T6		
6	VCCO_6	R6		
6	VCCO_6	P7		
6	VCCO_6	N7		
6	VCCO_6	M7		
7	VCCO_7	L7		
7	VCCO_7	K7		
7	VCCO_7	J7		

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
4	IO_L78N_4	Y15	NC	
4	IO_L78P_4	AA15	NC	
4	IO_L91N_4/VREF_4	W15		
4	IO_L91P_4	W16		
4	IO_L92N_4	AB15		
4	IO_L92P_4	AC15		
4	IO_L93N_4	AD15		
4	IO_L93P_4	AE15		
4	IO_L94N_4/VREF_4	W14		
4	IO_L94P_4	Y14		
4	IO_L95N_4/GCLK3S	AA14		
4	IO_L95P_4/GCLK2P	AB14		
4	IO_L96N_4/GCLK1S	AC14		
4	IO_L96P_4/GCLK0P	AD14		
5	IO_L96N_5/GCLK7S	AC13		
5	IO_L96P_5/GCLK6P	AB13		
5	IO_L95N_5/GCLK5S	AA13		
5	IO_L95P_5/GCLK4P	Y13		
5	IO_L94N_5	W13		
5	IO_L94P_5/VREF_5	W12		
5	IO_L93N_5	AF15		
5	IO_L93P_5	AF14		
5	IO_L92N_5	AF13		
5	IO_L92P_5	AF12		
5	IO_L91N_5	AE12		
5	IO_L91P_5/VREF_5	AD12		
5	IO_L78N_5	AC12	NC	
5	IO_L78P_5	AB12	NC	
5	IO_L76N_5	AA12	NC	
5	IO_L76P_5	Y12	NC	
5	IO_L75N_5/VREF_5	AF11	NC	
5	IO_L75P_5	AF10	NC	
5	IO_L73N_5	AE11	NC	
5	IO_L73P_5	AD11	NC	
5	IO_L72N_5	AC11		
5	IO_L72P_5	AB11		

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
3	IO_L52N_3	T21		
3	IO_L52P_3	T20		
3	IO_L51N_3/VREF_3	R20		
3	IO_L51P_3	R19		
3	IO_L49N_3	W24		
3	IO_L49P_3	W23		
3	IO_L48N_3	U23		
3	IO_L48P_3	V23		
3	IO_L46N_3	U22		
3	IO_L46P_3	U21		
3	IO_L45N_3/VREF_3	V22		
3	IO_L45P_3	V21		
3	IO_L43N_3	U19		
3	IO_L43P_3	U20		
3	IO_L24N_3	T19		
3	IO_L24P_3	T18		
3	IO_L22N_3	R18		
3	IO_L22P_3	R17		
3	IO_L21N_3/VREF_3	Y24		
3	IO_L21P_3	Y23		
3	IO_L19N_3	AA24		
3	IO_L19P_3	AB24		
3	IO_L06N_3	AA23		
3	IO_L06P_3	AA22		
3	IO_L04N_3	Y22		
3	IO_L04P_3	Y21		
3	IO_L03N_3/VREF_3	W21		
3	IO_L03P_3	W20		
3	IO_L02N_3/VRP_3	V20		
3	IO_L02P_3/VRN_3	V19		
3	IO_L01N_3	U18		
3	IO_L01P_3	T17		
4	IO_L01N_4/BUSY/DOUT[(1)]	AD22		
4	IO_L01P_4/INIT_B	AD21		
4	IO_L02N_4/D0/DIN[(1)]	AA20		

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
NA	GND	D15		
NA	GND	D10		
NA	GND	D4		
NA	GND	C22		
NA	GND	C3		
NA	GND	B24		
NA	GND	B23		
NA	GND	B2		
NA	GND	B1		
NA	GND	A24		
NA	GND	A23		
NA	GND	A18		
NA	GND	A7		
NA	GND	A2		

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
7	IO_L52P_7	J29		
7	IO_L52N_7	K29		
7	IO_L51P_7/VREF_7	K27		
7	IO_L51N_7	J27		
7	IO_L50P_7	L24		
7	IO_L50N_7	K24		
7	IO_L49P_7	H27		
7	IO_L49N_7	J28		
7	IO_L48P_7	H26		
7	IO_L48N_7	J26		
7	IO_L47P_7	K25		
7	IO_L47N_7	J25		
7	IO_L46P_7	H28		
7	IO_L46N_7	H29		
7	IO_L45P_7/VREF_7	G28		
7	IO_L45N_7	F28		
7	IO_L44P_7	L23		
7	IO_L44N_7	K23		
7	IO_L43P_7	F30		
7	IO_L43N_7	G30		
7	IO_L24P_7	F26		
7	IO_L24N_7	G27		
7	IO_L23P_7	J24		
7	IO_L23N_7	H24		
7	IO_L22P_7	F29		
7	IO_L22N_7	G29		
7	IO_L21P_7/VREF_7	G26		
7	IO_L21N_7	G25		
7	IO_L20P_7	H25		
7	IO_L20N_7	G24		
7	IO_L19P_7	D30		
7	IO_L19N_7	E30		
7	IO_L06P_7	E27		
7	IO_L06N_7	F27		
7	IO_L05P_7	J23		
7	IO_L05N_7	H22		
7	IO_L04P_7	C29		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
7	IO_L04N_7	D29		
7	IO_L03P_7/VREF_7	E28		
7	IO_L03N_7	D28		
7	IO_L02P_7/VRN_7	H23		
7	IO_L02N_7/VRP_7	G23		
7	IO_L01P_7	B30		
7	IO_L01N_7	C30		
0	VCCO_0	K20		
0	VCCO_0	K19		
0	VCCO_0	K18		
0	VCCO_0	K17		
0	VCCO_0	K16		
0	VCCO_0	J21		
0	VCCO_0	J20		
0	VCCO_0	J19		
0	VCCO_0	J18		
0	VCCO_0	C18		
0	VCCO_0	B26		
1	VCCO_1	K15		
1	VCCO_1	K14		
1	VCCO_1	K13		
1	VCCO_1	K12		
1	VCCO_1	K11		
1	VCCO_1	J13		
1	VCCO_1	J12		
1	VCCO_1	J11		
1	VCCO_1	J10		
1	VCCO_1	C13		
1	VCCO_1	B5		
2	VCCO_2	R10		
2	VCCO_2	P10		
2	VCCO_2	N10		
2	VCCO_2	N9		
2	VCCO_2	N3		
2	VCCO_2	M10		
2	VCCO_2	M9		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
2	VCCO_2	L10		
2	VCCO_2	L9		
2	VCCO_2	K9		
2	VCCO_2	E2		
3	VCCO_3	AF2		
3	VCCO_3	AA9		
3	VCCO_3	Y10		
3	VCCO_3	Y9		
3	VCCO_3	W10		
3	VCCO_3	W9		
3	VCCO_3	V10		
3	VCCO_3	V9		
3	VCCO_3	V3		
3	VCCO_3	U10		
3	VCCO_3	T10		
4	VCCO_4	AJ5		
4	VCCO_4	AH13		
4	VCCO_4	AB13		
4	VCCO_4	AB12		
4	VCCO_4	AB11		
4	VCCO_4	AB10		
4	VCCO_4	AA15		
4	VCCO_4	AA14		
4	VCCO_4	AA13		
4	VCCO_4	AA12		
4	VCCO_4	AA11		
5	VCCO_5	AJ26		
5	VCCO_5	AH18		
5	VCCO_5	AB21		
5	VCCO_5	AB20		
5	VCCO_5	AB19		
5	VCCO_5	AB18		
5	VCCO_5	AA20		
5	VCCO_5	AA19		
5	VCCO_5	AA18		
5	VCCO_5	AA17		
5	VCCO_5	AA16		

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
1	IO_L93P_1	F17	
1	IO_L92N_1	G16	
1	IO_L92P_1	G17	
1	IO_L91N_1	C16	
1	IO_L91P_1/VREF_1	C15	
1	IO_L84N_1	D14	NC
1	IO_L84P_1	D15	NC
1	IO_L83N_1	J17	NC
1	IO_L83P_1	K17	NC
1	IO_L82N_1	B17	NC
1	IO_L82P_1	A17	NC
1	IO_L81N_1/VREF_1	A15	NC
1	IO_L81P_1	B16	NC
1	IO_L80N_1	L17	NC
1	IO_L80P_1	L16	NC
1	IO_L79N_1	A13	NC
1	IO_L79P_1	A14	NC
1	IO_L78N_1	C13	
1	IO_L78P_1	C14	
1	IO_L77N_1	K16	
1	IO_L77P_1	K15	
1	IO_L76N_1	B13	
1	IO_L76P_1	B14	
1	IO_L75N_1/VREF_1	F15	
1	IO_L75P_1	G15	
1	IO_L74N_1	H15	
1	IO_L74P_1	H14	
1	IO_L73N_1	A11	
1	IO_L73P_1	A12	
1	IO_L72N_1	E13	
1	IO_L72P_1	E14	
1	IO_L71N_1	J15	
1	IO_L71P_1	J14	
1	IO_L70N_1	D12	
1	IO_L70P_1	D13	
1	IO_L69N_1/VREF_1	F14	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
7	IO_L75N_7	R28	
7	IO_L74P_7	R26	
7	IO_L74N_7	P26	
7	IO_L73P_7	N31	
7	IO_L73N_7	P31	
7	IO_L72P_7	N30	
7	IO_L72N_7	P30	
7	IO_L71P_7	R25	
7	IO_L71N_7	P25	
7	IO_L70P_7	L34	
7	IO_L70N_7	M34	
7	IO_L69P_7/VREF_7	P29	
7	IO_L69N_7	N29	
7	IO_L68P_7	P27	
7	IO_L68N_7	N27	
7	IO_L67P_7	L32	
7	IO_L67N_7	M32	
7	IO_L54P_7	L31	
7	IO_L54N_7	M31	
7	IO_L53P_7	K29	
7	IO_L53N_7	L30	
7	IO_L52P_7	L33	
7	IO_L52N_7	M33	
7	IO_L51P_7/VREF_7	M29	
7	IO_L51N_7	L29	
7	IO_L50P_7	M28	
7	IO_L50N_7	N28	
7	IO_L49P_7	K30	
7	IO_L49N_7	K31	
7	IO_L48P_7	H32	
7	IO_L48N_7	J32	
7	IO_L47P_7	N26	
7	IO_L47N_7	M26	
7	IO_L46P_7	J33	
7	IO_L46N_7	K33	
7	IO_L45P_7/VREF_7	H33	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
3	IO_L10N_3	AK7	NC	
3	IO_L10P_3	AL7	NC	
3	IO_L09N_3/VREF_3	AK11	NC	
3	IO_L09P_3	AJ10	NC	
3	IO_L08N_3	AR1	NC	
3	IO_L08P_3	AT1	NC	
3	IO_L07N_3	AM5	NC	
3	IO_L07P_3	AN5	NC	
3	IO_L06N_3	AM7		
3	IO_L06P_3	AL8		
3	IO_L05N_3	AP3		
3	IO_L05P_3	AP4		
3	IO_L04N_3	AM6		
3	IO_L04P_3	AN6		
3	IO_L03N_3/VREF_3	AJ13		
3	IO_L03P_3	AH13		
3	IO_L02N_3/VRP_3	AR3		
3	IO_L02P_3/VRN_3	AT2		
3	IO_L01N_3	AP5		
3	IO_L01P_3	AR4		
4	IO_L01N_4/BUSY/DOUT(1)	AV4		
4	IO_L01P_4/INIT_B	AU4		
4	IO_L02N_4/D0/DIN(1)	AM9		
4	IO_L02P_4/D1	AM10		
4	IO_L03N_4/D2/ALT_VRP_4	AT6		
4	IO_L03P_4/D3/ALT_VRN_4	AR6		
4	IO_L04N_4/VREF_4	AU6		
4	IO_L04P_4	AU5		
4	IO_L05N_4/VRP_4	AL10		
4	IO_L05P_4/VRN_4	AL11		
4	IO_L06N_4	AR8		
4	IO_L06P_4	AR7		
4	IO_L07N_4	AW5	NC	
4	IO_L07P_4	AW4	NC	
4	IO_L08N_4	AK12	NC	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
5	IO_L01N_5/RDWR_B	AU36		
5	IO_L01P_5/CS_B	AV36		
6	IO_L01P_6	AJ27		
6	IO_L01N_6	AH27		
6	IO_L02P_6/VRN_6	AT38		
6	IO_L02N_6/VRP_6	AR37		
6	IO_L03P_6	AP36		
6	IO_L03N_6/VREF_6	AR36		
6	IO_L04P_6	AJ28		
6	IO_L04N_6	AH29		
6	IO_L05P_6	AT39		
6	IO_L05N_6	AR39		
6	IO_L06P_6	AN34		
6	IO_L06N_6	AP35		
6	IO_L07P_6	AH28	NC	
6	IO_L07N_6	AG28	NC	
6	IO_L08P_6	AR38	NC	
6	IO_L08N_6	AP38	NC	
6	IO_L09P_6	AM34	NC	
6	IO_L09N_6/VREF_6	AM33	NC	
6	IO_L10P_6	AL32	NC	
6	IO_L10N_6	AK32	NC	
6	IO_L11P_6	AP37	NC	
6	IO_L11N_6	AN37	NC	
6	IO_L12P_6	AM35	NC	
6	IO_L12N_6	AN35	NC	
6	IO_L19P_6	AK31		
6	IO_L19N_6	AJ30		
6	IO_L20P_6	AP39		
6	IO_L20N_6	AN39		
6	IO_L21P_6	AK33		
6	IO_L21N_6/VREF_6	AL33		
6	IO_L22P_6	AJ31		
6	IO_L22N_6	AH31		
6	IO_L23P_6	AN38		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
6	IO_L47N_6	AJ39		
6	IO_L48P_6	AG35		
6	IO_L48N_6	AH35		
6	IO_L49P_6	AG32		
6	IO_L49N_6	AF32		
6	IO_L50P_6	AH37		
6	IO_L50N_6	AG37		
6	IO_L51P_6	AD29		
6	IO_L51N_6/VREF_6	AE29		
6	IO_L52P_6	AD28		
6	IO_L52N_6	AC28		
6	IO_L53P_6	AH38		
6	IO_L53N_6	AG38		
6	IO_L54P_6	AF34		
6	IO_L54N_6	AG34		
6	IO_L55P_6	AE32		
6	IO_L55N_6	AD32		
6	IO_L56P_6	AH39		
6	IO_L56N_6	AG39		
6	IO_L57P_6	AE33		
6	IO_L57N_6/VREF_6	AF33		
6	IO_L58P_6	AD30		
6	IO_L58N_6	AC30		
6	IO_L59P_6	AF37		
6	IO_L59N_6	AE37		
6	IO_L60P_6	AF36		
6	IO_L60N_6	AG36		
6	IO_L67P_6	AD31		
6	IO_L67N_6	AC31		
6	IO_L68P_6	AE34		
6	IO_L68N_6	AD34		
6	IO_L69P_6	AD35		
6	IO_L69N_6/VREF_6	AE35		
6	IO_L70P_6	AB28		
6	IO_L70N_6	AA28		
6	IO_L71P_6	AF39		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	VCCINT	AE18		
NA	VCCINT	AE17		
NA	VCCINT	AE16		
NA	VCCINT	AE15		
NA	VCCINT	AD25		
NA	VCCINT	AD24		
NA	VCCINT	AD16		
NA	VCCINT	AD15		
NA	VCCINT	AC25		
NA	VCCINT	AC15		
NA	VCCINT	AB25		
NA	VCCINT	AB15		
NA	VCCINT	AA25		
NA	VCCINT	AA15		
NA	VCCINT	Y27		
NA	VCCINT	Y26		
NA	VCCINT	Y25		
NA	VCCINT	Y15		
NA	VCCINT	Y14		
NA	VCCINT	Y13		
NA	VCCINT	W25		
NA	VCCINT	W15		
NA	VCCINT	V25		
NA	VCCINT	V15		
NA	VCCINT	U25		
NA	VCCINT	U15		
NA	VCCINT	T25		
NA	VCCINT	T24		
NA	VCCINT	T16		
NA	VCCINT	T15		
NA	VCCINT	R25		
NA	VCCINT	R24		
NA	VCCINT	R23		
NA	VCCINT	R22		
NA	VCCINT	R21		
NA	VCCINT	R20		