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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	8448
Number of Logic Elements/Cells	-
Total RAM Bits	2654208
Number of I/O	684
Number of Gates	6000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	957-BBGA, FCBGA
Supplier Device Package	957-FCBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v6000-5bf957c

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
11/07/00	1.0	Early access draft.
12/06/00	1.1	Initial release.
01/15/01	1.2	Added values to the tables in the Virtex-II Performance Characteristics and Virtex-II Switching Characteristics sections.
01/25/01	1.3	The data sheet was divided into four modules (per the current style standard).
04/02/01	1.5	Skipped v1.4 to sync up modules. Reverted to traditional double-column format.
07/30/01	1.6	Made minor changes to items listed under Summary of Virtex-II™ Features .
10/02/01	1.7	Minor edits.
07/16/02	1.8	Updated Virtex-II Device/Package Combinations shown in Table 6 .
09/26/02	1.9	Updated Table 2 and Table 6 to reflect supported Virtex-II Device/Package Combinations.
08/01/03	2.0	All Virtex-II devices and speed grades now Production. See Table 13, Module 3.
03/29/04	2.0.1	Recompiled for backward compatibility with Acrobat 4 and above. No content changes.
06/24/04	3.3	Added references to available Pb-free wire-bond packages. (Revision number advanced to level of complete data sheet.)
03/01/05	3.4	<i>No changes in Module 1 for this revision.</i>
11/05/07	3.5	Updated copyright notice and legal disclaimer.

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Virtex-II Data Sheet

The Virtex-II Data Sheet contains the following modules:

- **Virtex-II Platform FPGAs: Introduction and Overview (Module 1)**
- **Virtex-II Platform FPGAs: Functional Description (Module 2)**
- **Virtex-II Platform FPGAs: DC and Switching Characteristics (Module 3)**
- **Virtex-II Platform FPGAs: Pinout Information (Module 4)**

Sum of Products

Each Virtex-II slice has a dedicated OR gate named ORCY, ORing together outputs from the slices carryout and the ORCY from an adjacent slice. The ORCY gate with the dedicated Sum of Products (SOP) chain are designed for implementing

large, flexible SOP chains. One input of each ORCY is connected through the fast SOP chain to the output of the previous ORCY in the same slice row. The second input is connected to the output of the top MUXCY in the same slice, as shown in **Figure 25**.

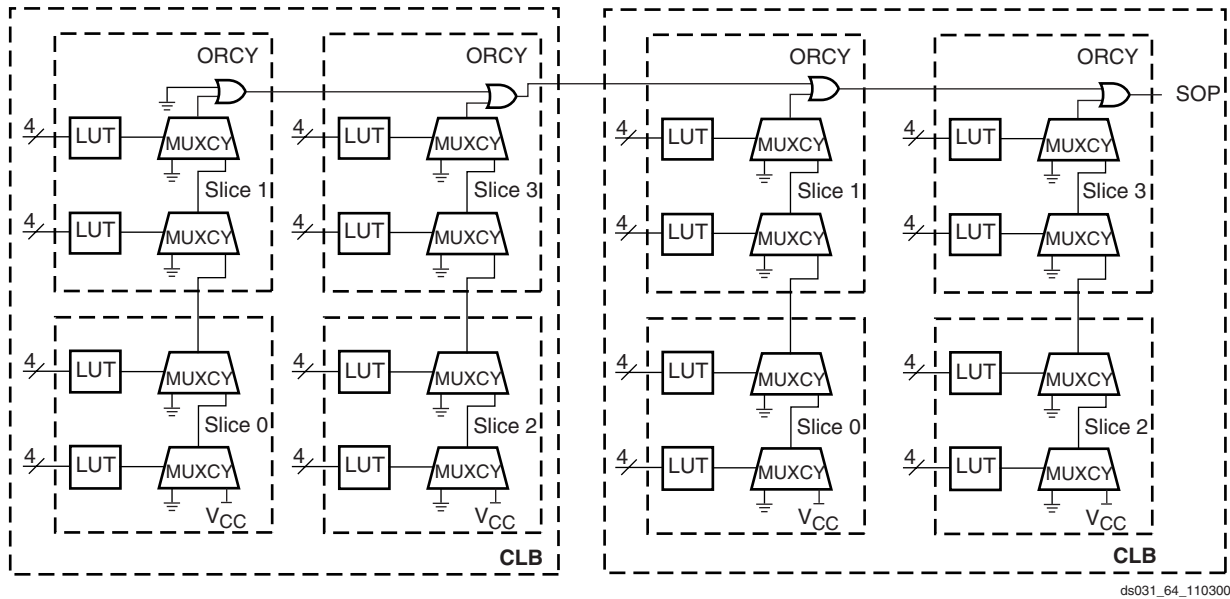


Figure 25: Horizontal Cascade Chain

LUTs and MUXCYs can implement large AND gates or other combinatorial logic functions. Figure 26 illustrates

LUT and MUXCY resources configured as a 16-input AND gate.

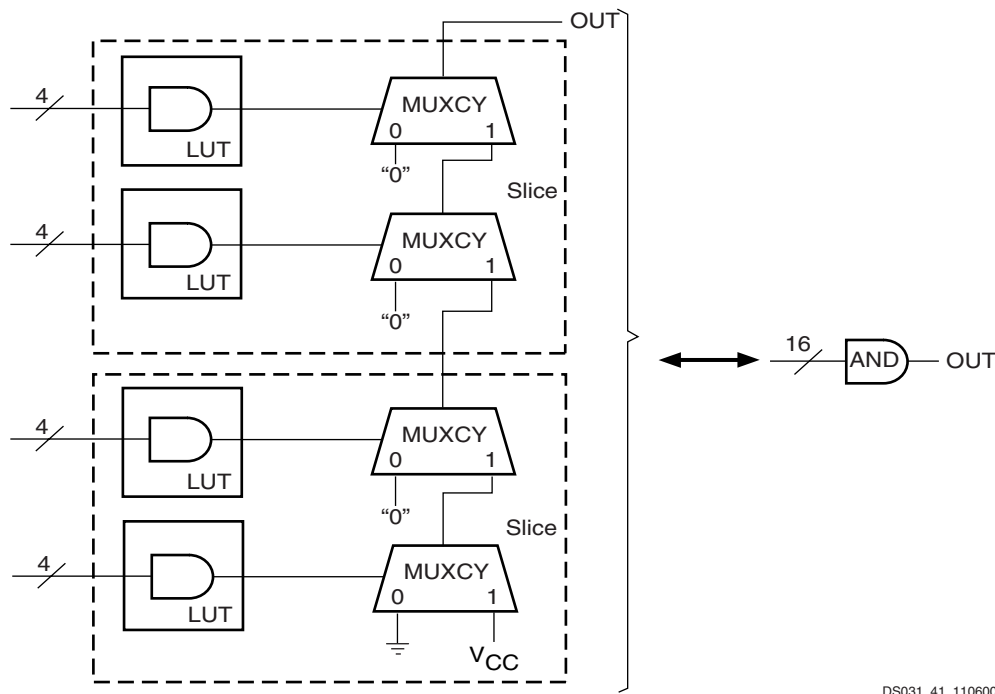


Figure 26: Wide-Input AND Gate (16 Inputs)

Routing

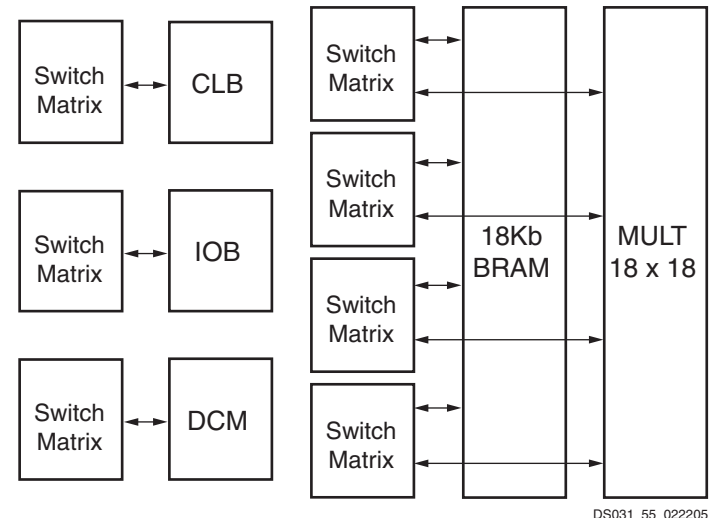
DCM Locations/Organization

Virtex-II DCMs are placed on the top and bottom of each block RAM and multiplier column. The number of DCMs depends on the device size, as shown in Table 24.

Table 24: DCM Organization

Device	Columns	DCMs
XC2V40	2	4
XC2V80	2	4
XC2V250	4	8
XC2V500	4	8
XC2V1000	4	8
XC2V1500	4	8
XC2V2000	4	8
XC2V3000	6	12
XC2V4000	6	12
XC2V6000	6	12
XC2V8000	6	12

ing resources are segmented to offer the advantages of a hierarchical solution. Virtex-II logic features like CLBs, IOBs, block RAM, multipliers, and DCMs are all connected to an identical switch matrix for access to global routing resources, as shown in Figure 47.



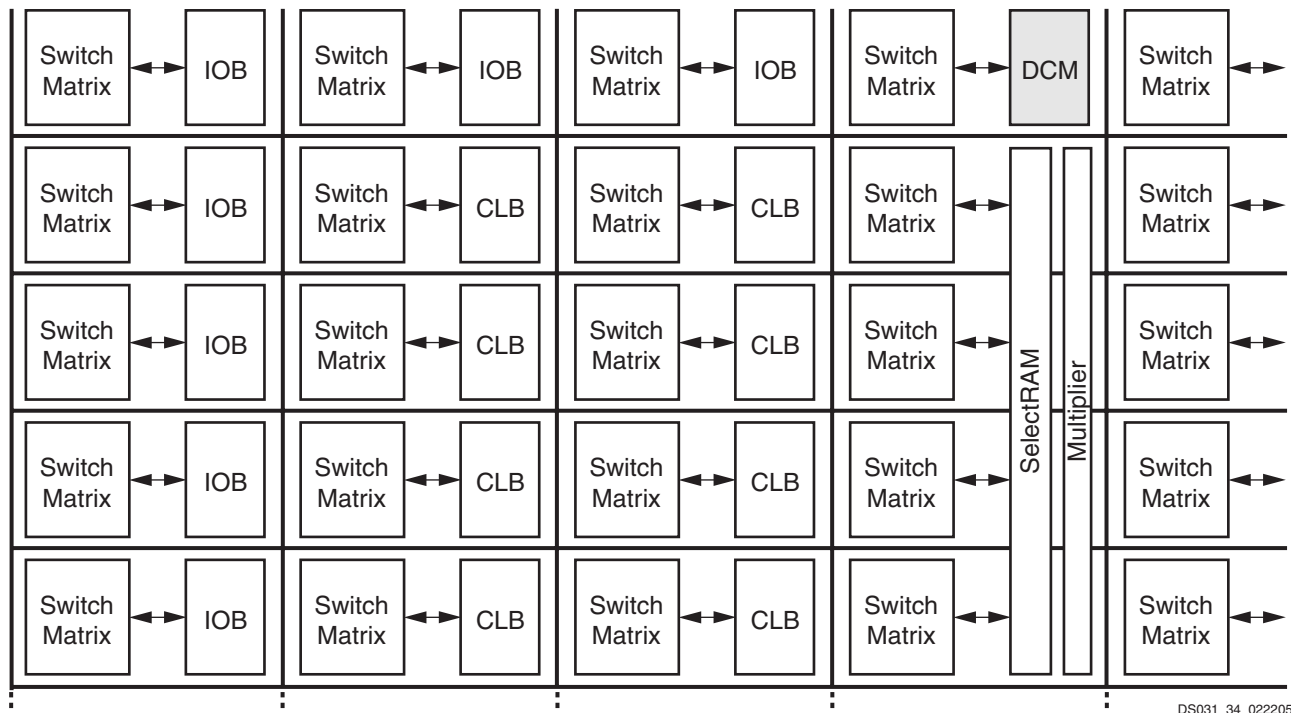
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Figure 47: Active Interconnect Technology

Active Interconnect Technology

Local and global Virtex-II routing resources are optimized for speed and timing predictability, as well as to facilitate IP cores implementation. Virtex-II Active Interconnect Technology is a fully buffered programmable routing matrix. All rout-

Each Virtex-II device can be represented as an array of switch matrixes with logic blocks attached, as illustrated in Figure 48.



DS031_34_022205

Figure 48: Routing Resources

Virtex-II FPGA device. Timing is similar to the Slave Serial-MAP mode except that CCLK is supplied by the Virtex-II FPGA.

Boundary-Scan (JTAG, IEEE 1532) Mode

In Boundary-Scan mode, dedicated pins are used for configuring the Virtex-II device. The configuration is done entirely through the IEEE 1149.1 Test Access Port (TAP). Virtex-II device configuration using Boundary-Scan is compatible with the IEEE 1149.1-1993 standard and the new

IEEE 1532 standard for In-System Configurable (ISC) devices. The IEEE 1532 standard is backward compliant with the IEEE 1149.1-1993 TAP and state machine. The IEEE Standard 1532 for In-System Configurable (ISC) devices is intended to be programmed, reprogrammed, or tested on the board via a physical and logical protocol.

Configuration through the Boundary-Scan port is always available, independent of the mode selection. Selecting the Boundary-Scan mode simply turns off the other modes.

Table 25: Virtex-II Configuration Mode Pin Settings

Configuration Mode ⁽¹⁾	M2	M1	M0	CCLK Direction	Data Width	Serial D _{OUT} ⁽²⁾
Master Serial	0	0	0	Out	1	Yes
Slave Serial	1	1	1	In	1	Yes
Master SelectMAP	0	1	1	Out	8	No
Slave SelectMAP	1	1	0	In	8	No
Boundary-Scan	1	0	1	N/A	1	No

Notes:

1. The HSWAP_EN pin controls the pull-ups. Setting M2, M1, and M0 selects the configuration mode, while the HSWAP_EN pin controls whether or not the pull-ups are used.
2. Daisy chaining is possible only in modes where Serial D_{OUT} is used. For example, in SelectMAP modes, the first device does NOT support daisy chaining of downstream devices.

Table 26 lists the total number of bits required to configure each device.

Table 26: Virtex-II Bitstream Lengths

Device	# of Configuration Bits
XC2V40	338,976
XC2V80	598,816
XC2V250	1,593,632
XC2V500	2,560,544
XC2V1000	4,082,592
XC2V1500	5,170,208
XC2V2000	6,812,960
XC2V3000	10,494,368
XC2V4000	15,659,936
XC2V6000	21,849,504
XC2V8000	26,194,208

Configuration Sequence

The configuration of Virtex-II devices is a three-phase process after Power On Reset or POR. POR occurs when V_{CCINT} is greater than 1.2V, V_{CCAUX} is greater than 2.5V,

and V_{CCO} (bank 4) is greater than 1.5V. Once the POR voltages have been reached, the three-phase process begins.

First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process.

Configuration is automatically initiated on power-up unless it is delayed by the user. The INIT_B pin can be held Low using an open-drain driver. An open-drain is required since INIT_B is a bidirectional open-drain pin that is held Low by a Virtex-II FPGA device while the configuration memory is being cleared. Extending the time that the pin is Low causes the configuration sequencer to wait. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

The configuration process can also be initiated by asserting the PROG_B pin. The end of the memory-clearing phase is signaled by the INIT_B pin going High, and the completion of the entire process is signaled by the DONE pin going High. The Global Set/Reset (GSR) signal is pulsed after the last frame of configuration data is written but before the start-up sequence. The GSR signal resets all flip-flops on the device.

The default start-up sequence is that one CCLK cycle after DONE goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary. One CCLK cycle later, the Global Write Enable (GWE) signal is released. This permits the internal storage ele-

Virtex-II Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex-II devices. The numbers reported here are worst-case values; they have all been fully characterized. Note that these values are subject to the same guidelines as [Virtex-II Switching Characteristics, page 9](#) (speed files).

Table 11 provides pin-to-pin values (in nanoseconds) including IOB delays; that is, delay through the device from input pin to output pin. In the case of multiple inputs and outputs, the worst delay is reported.

Table 11: Pin-to-Pin Performance

Description	Device Used & Speed Grade	Pin-to-Pin (with I/O delays)	Units
Basic Functions			
16-bit Address Decoder	XC2V1000 -5	6.3	ns
32-bit Address Decoder	XC2V1000 -5	7.7	ns
64-bit Address Decoder	XC2V1000 -5	9.3	ns
4:1 MUX	XC2V1000 -5	5.7	ns
8:1 MUX	XC2V1000 -5	6.5	ns
16:1 MUX	XC2V1000 -5	6.7	ns
32:1 MUX	XC2V1000 -5	8.7	ns
Combinatorial (pad to LUT to pad)	XC2V1000 -5	5.0	ns
Memory			
Block RAM			
Pad to setup		1.6	ns
Clock to Pad		9.5	ns
Distributed RAM			
Pad to setup	XC2V1000 -5	2.7	ns
Clock to Pad	XC2V1000 -5	5.1 (no clk skew)	ns

Table 12 shows internal (register-to-register) performance. Values are reported in MHz.

Table 12: Register-to-Register Performance

Description	Device Used & Speed Grade	Register-to-Register Performance	Units
Basic Functions			
16-bit Address Decoder	XC2V1000 -5	398	MHz
32-bit Address Decoder	XC2V1000 -5	291	MHz
64-bit Address Decoder	XC2V1000 -5	274	MHz
4:1 MUX	XC2V1000 -5	563	MHz
8:1 MUX	XC2V1000 -5	454	MHz
16:1 MUX	XC2V1000 -5	414	MHz
32:1 MUX	XC2V1000 -5	323	MHz
Register to LUT to Register	XC2V1000 -5	613	MHz

Table 19: Output Delay Measurement Methodology

Description	IOSTANDARD Attribute	R _{REF} (Ω)	C _{REF} ⁽¹⁾ (pF)	V _{MEAS} (V)	V _{REF} (V)
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	50	0	V _{REF}	0.9
SSTL, Class II, 1.8V	SSTL18_II	25	0	V _{REF}	0.9
SSTL, Class I, 2.5V	SSTL2_I	50	0	V _{REF}	1.25
SSTL, Class II, 2.5V	SSTL2_II	25	0	V _{REF}	1.25
SSTL, Class I, 3.3V	SSTL3_I	50	0	V _{REF}	1.5
SSTL, Class II, 3.3V	SSTL3_II	25	0	V _{REF}	1.5
AGP-2X/AGP (Accelerated Graphics Port)	AGP-2X/AGP (rising edge)	50	0	0.94	0
	AGP-2X/AGP (falling edge)	50	0	2.03	3.3
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	50	0	V _{REF}	1.2
LVDS, 3.3V	LVDSEXT_25	50	0	V _{REF}	1.2
LVDSEXT (LVDS Extended Mode), 2.5V	LVDS_33	50	0	V _{REF}	1.2
LVDSEXT, 3.3V	LVDSEXT_33	50	0	V _{REF}	1.2
BLVDS (Bus LVDS), 2.5V	BLVDS_25	1M	0	1.2	0
LDT (HyperTransport), 2.5V	LDT_25	50	0	V _{REF}	0.6
LVPECL (Low-Voltage Positive Electron-Coupled Logic), 3.3V	LVPECL_33	1M	0	1.23	0
LVDCI/HSLVDCI (Low-Voltage Digitally Controlled Impedance), 3.3V	LVDCI_33, HSLVDCI_33	1M	0	1.65	0
LVDCI/HSLVDCI, 2.5V	LVDCI_25, HSLVDCI_25	1M	0	1.25	0
LVDCI/HSLVDCI, 1.8V	LVDCI_18, HSLVDCI_18	1M	0	0.9	0
LVDCI/HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I & II, with DCI	HSTL_I_DCI, HSTL_II_DCI	50	0	V _{REF}	0.75
HSTL, Class III & IV, with DCI	HSTL_III_DCI, HSTL_IV_DCI	50	0	0.9	1.5
HSTL, Class I & II, 1.8V, with DCI	HSTL_I_DCI_18, HSTL_II_DCI_18	50	0	V _{REF}	0.9
HSTL, Class III & IV, 1.8V, with DCI	HSTL_III_DCI_18, HSTL_IV_DCI_18	50	0	1.1	1.8
SSTL (Stub Series Termini.Logic), Class I & II, 1.8V, with DCI	SSTL18_I_DCI, SSTL18_II_DCI	50	0	V _{REF}	0.9
SSTL, Class I & II, 2.5V, with DCI	SSTL2_I_DCI, SSTL2_II_DCI	50	0	V _{REF}	1.25
SSTL, Class I & II, 3.3V, with DCI	SSTL3_I_DCI, SSTL3_II_DCI	50	0	V _{REF}	1.5
GTL (Gunning Transceiver Logic) with DCI	GTL_DCI	50	0	0.8	1.2
GTL Plus with DCI	GTLP_DCI	50	0	1.0	1.5

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. Per PCI specifications.
3. Per PCI-X specifications.

Clock Distribution Switching Characteristics

Table 20: Clock Distribution Switching Characteristics

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Global Clock Buffer I input to O output	T_{GIO}	0.47	0.52	0.59	ns, Max
Global Clock Buffer S input Setup/Hold to I1 and I2 inputs	T_{GSI}/T_{GIS}	0.55/ 0	0.61/ 0	0.70/ 0	ns, Max

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used (see Figure 16 in Module 2). The values listed below are worst-case. Precise values are provided by the timing analyzer.

Table 21: CLB Switching Characteristics

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Combinatorial Delays					
4-input function: F/G inputs to X/Y outputs	T _{ILO}	0.35	0.39	0.44	ns, Max
5-input function: F/G inputs to F5 output	T _{IF5}	0.57	0.63	0.72	ns, Max
5-input function: F/G inputs to X output	T _{IF5X}	0.76	0.83	0.95	ns, Max
FXINA or FXINB inputs to Y output via MUXFX	T _{IFXY}	0.36	0.39	0.45	ns, Max
FXINA input to FX output via MUXFX	T _{INAFX}	0.26	0.28	0.32	ns, Max
FXINB input to FX output via MUXFX	T _{INBFX}	0.26	0.28	0.32	ns, Max
SOPIN input to SOPOUT output via ORCY	T _{SOPSOP}	0.35	0.38	0.44	ns, Max
Incremental delay routing through transparent latch to XQ/YQ outputs	T _{IFNCTL}	0.41	0.45	0.51	ns, Max
Sequential Delays					
FF Clock CLK to XQ/YQ outputs	T _{CKO}	0.45	0.50	0.57	ns, Max
Latch Clock CLK to XQ/YQ outputs	T _{CKLO}	0.54	0.59	0.68	ns, Max
Setup and Hold Times Before/After Clock CLK					
BX/BY inputs	T _{DICK} /T _{CKDI}	0.30/–0.07	0.33/–0.08	0.37/–0.09	ns, Min
DY inputs	T _{DYCK} /T _{CKDY}	0.30/–0.07	0.33/–0.08	0.37/–0.09	ns, Min
DX inputs	T _{DXCK} /T _{CKDX}	0.30/–0.07	0.33/–0.08	0.37/–0.09	ns, Min
CE input	T _{CECK} /T _{CKCE}	0.19/–0.06	0.21/–0.07	0.24/–0.08	ns, Min
SR/BY inputs (synchronous)	T _{SRCK} /T _{SCKR}	0.21/–0.02	0.23/–0.03	0.26/–0.03	ns, Min
Clock CLK					
Minimum Pulse Width, High	T _{CH}	0.61	0.67	0.77	ns, Min
Minimum Pulse Width, Low	T _{CL}	0.61	0.67	0.77	ns, Min
Set/Reset					
Minimum Pulse Width, SR/BY inputs (asynchronous)	T _{RPW}	0.61	0.67	0.77	ns, Min
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	T _{RQ}	1.06	1.17	1.34	ns, Max
Toggle Frequency (MHz) (for export control)	F _{TOG}	820	750	650	MHz

Block SelectRAM Switching Characteristics

Table 28: Block SelectRAM Switching Characteristics

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Sequential Delays					
Clock CLK to DOUT output	T _{BCKO}	2.10	2.31	2.65	ns, Max
Setup and Hold Times Before Clock CLK					
ADDR inputs	T _{BACK} /T _{BCKA}	0.29/ 0.00	0.32/ 0.00	0.36/ 0.00	ns, Min
DIN inputs	T _{BDCK} /T _{BCKD}	0.29/ 0.00	0.32/ 0.00	0.36/ 0.00	ns, Min
EN input	T _{BECK} /T _{BCKE}	0.95/−0.46	1.04/−0.50	1.20/−0.58	ns, Min
RST input	T _{BRCK} /T _{BCKR}	1.31/−0.71	1.44/−0.78	1.65/−0.90	ns, Min
WEN input	T _{BWCK} /T _{BCKW}	0.57/−0.19	0.63/−0.21	0.72/−0.25	ns, Min
Clock CLK					
CLKA to CLKB setup time for different ports	T _{BCCS}	1.0	1.0	1.0	ns, min
Minimum Pulse Width, High	T _{BPWH}	1.17	1.29	1.48	ns, Min
Minimum Pulse Width, Low	T _{BPWL}	1.17	1.29	1.48	ns, Min

TBUF Switching Characteristics

Table 29: TBUF Switching Characteristics

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Combinatorial Delays					
IN input to OUT output	T _{IO}	0.45	0.50	0.58	ns, Max
TRI input to OUT output high-impedance	T _{OFF}	0.44	0.48	0.55	ns, Max
TRI input to valid data on OUT output	T _{ON}	0.44	0.48	0.55	ns, Max

Table 5: CS144/CSG144 — XC2V40, XC2V80, and XC2V250

Bank	Pin Description	Pin Number	No Connect in the XC2V40
NA	CCLK	M13	
NA	PROG_B	B1	
NA	DONE	N12	
NA	M0	N2	
NA	M1	M2	
NA	M2	M3	
NA	TCK	B12	
NA	TDI	C1	
NA	TDO	C11	
NA	TMS	A13	
NA	PWRDWN_B	M12	
NA	HSWAP_EN	A1	
NA	RSVD	A2	
NA	RSVD	B2	
NA	VBATT	A12	
NA	RSVD	B11	
NA	VCCAUX	C2	
NA	VCCAUX	N1	
NA	VCCAUX	N13	
NA	VCCAUX	B13	
NA	VCCINT	H2	
NA	VCCINT	L7	
NA	VCCINT	H13	
NA	VCCINT	C7	
NA	GND	E1	
NA	GND	G2	
NA	GND	J1	
NA	GND	J4	
NA	GND	M5	
NA	GND	L9	
NA	GND	J11	
NA	GND	H10	
NA	GND	F13	
NA	GND	E12	
NA	GND	B9	
NA	GND	C5	

Notes:

- See Table 4 for an explanation of the signals available on this pin.

Table 7: FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
4	IO_L95N_4/GCLK3S	W12		
4	IO_L95P_4/GCLK2P	Y12		
4	IO_L96N_4/GCLK1S	AA12		
4	IO_L96P_4/GCLK0P	AB12		
5	IO_L96N_5/GCLK7S	AA11		
5	IO_L96P_5/GCLK6P	Y11		
5	IO_L95N_5/GCLK5S	W11		
5	IO_L95P_5/GCLK4P	V11		
5	IO_L94N_5	U11		
5	IO_L94P_5/VREF_5	U10		
5	IO_L93N_5	AB10		
5	IO_L93P_5	AA10		
5	IO_L92N_5	Y10		
5	IO_L92P_5	W10		
5	IO_L91N_5	V10		
5	IO_L91P_5/VREF_5	V9		
5	IO_L54N_5	AB9	NC	
5	IO_L54P_5	AA9	NC	
5	IO_L52N_5	Y9	NC	
5	IO_L52P_5	W9	NC	
5	IO_L51N_5/VREF_5	AB8	NC	
5	IO_L51P_5	AA8	NC	
5	IO_L49N_5	Y8	NC	
5	IO_L49P_5	W8	NC	
5	IO_L24N_5	U9	NC	NC
5	IO_L24P_5	V8	NC	NC
5	IO_L22N_5	AB7	NC	NC
5	IO_L22P_5	AA7	NC	NC
5	IO_L21N_5/VREF_5	Y7	NC	NC
5	IO_L21P_5	W7	NC	NC
5	IO_L19N_5	AB6	NC	NC
5	IO_L19P_5	AA6	NC	NC
5	IO_L06N_5	Y6		

Table 8: FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
1	IO_L92P_1	A15		
1	IO_L91N_1	B15		
1	IO_L91P_1/VREF_1	C15		
1	IO_L78N_1	D15	NC	
1	IO_L78P_1	E15	NC	
1	IO_L76N_1	F15	NC	
1	IO_L76P_1	G15	NC	
1	IO_L75N_1/VREF_1	G16	NC	
1	IO_L75P_1	F16	NC	
1	IO_L73N_1	A16	NC	
1	IO_L73P_1	A17	NC	
1	IO_L72N_1	B16		
1	IO_L72P_1	C16		
1	IO_L70N_1	D16		
1	IO_L70P_1	E16		
1	IO_L69N_1/VREF_1	C17		
1	IO_L69P_1	D17		
1	IO_L67N_1	H16		
1	IO_L67P_1	G17		
1	IO_L54N_1	E17		
1	IO_L54P_1	F17		
1	IO_L52N_1	A18		
1	IO_L52P_1	A19		
1	IO_L51N_1/VREF_1	E18		
1	IO_L51P_1	D18		
1	IO_L49N_1	B18		
1	IO_L49P_1	C18		
1	IO_L27N_1/VREF_1	F19	NC	NC
1	IO_L27P_1	F18	NC	NC
1	IO_L25N_1	G18	NC	NC
1	IO_L25P_1	G19	NC	NC
1	IO_L24N_1	B19		
1	IO_L24P_1	C19		
1	IO_L22N_1	D19		
1	IO_L22P_1	E19		
1	IO_L21N_1/VREF_1	A20		
1	IO_L21P_1	A21		

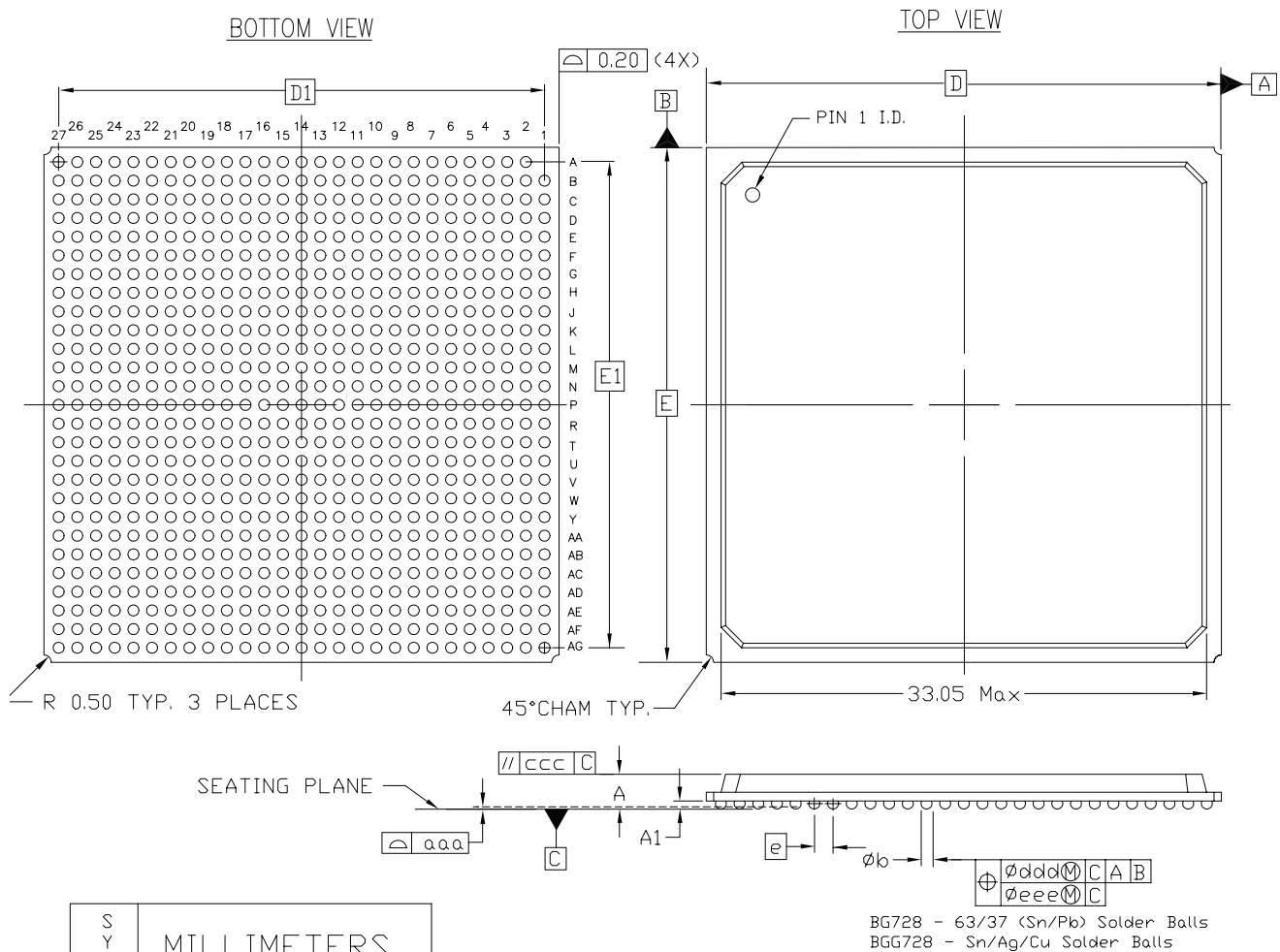
Table 8: FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
NA	DONE	AD22		
NA	M0	AD4		
NA	M1	AA5		
NA	M2	AD5		
NA	HSWAP_EN	D5		
NA	TCK	E21		
NA	TDI	F5		
NA	TDO	F22		
NA	TMS	D22		
NA	PWRDWN_B	AD23		
NA	DXN	F7		
NA	DXP	C5		
NA	VBATT	C23		
NA	RSVD	C22		
NA	VCCAUX	AD13		
NA	VCCAUX	AC24		
NA	VCCAUX	AC3		
NA	VCCAUX	P24		
NA	VCCAUX	N3		
NA	VCCAUX	D24		
NA	VCCAUX	D3		
NA	VCCAUX	C14		
NA	VCCINT	W19		
NA	VCCINT	W8		
NA	VCCINT	V18		
NA	VCCINT	V17		
NA	VCCINT	V10		
NA	VCCINT	V9		
NA	VCCINT	U18		
NA	VCCINT	U9		
NA	VCCINT	K18		
NA	VCCINT	K9		
NA	VCCINT	J18		
NA	VCCINT	J17		
NA	VCCINT	J10		
NA	VCCINT	J9		

Table 9: BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
4	IO_L02P_4/D1	AB20		
4	IO_L03N_4/D2/ALT_VRP_4	Y19		
4	IO_L03P_4/D3/ALT_VRN_4	AA19		
4	IO_L04N_4/VREF_4	W18		
4	IO_L04P_4	Y18		
4	IO_L05N_4/VRP_4	U16		
4	IO_L05P_4/VRN_4	V17		
4	IO_L06N_4	AD20		
4	IO_L06P_4	AD19		
4	IO_L19N_4	AC20		
4	IO_L19P_4	AC19		
4	IO_L21N_4	AA18		
4	IO_L21P_4/VREF_4	AB18		
4	IO_L22N_4	AC18		
4	IO_L22P_4	AC17		
4	IO_L24N_4	AA17		
4	IO_L24P_4	AB17		
4	IO_L49N_4	Y17		
4	IO_L49P_4	W17		
4	IO_L51N_4	V16		
4	IO_L51P_4/VREF_4	W16		
4	IO_L52N_4	AD17		
4	IO_L52P_4	AD16		
4	IO_L54N_4	AB16		
4	IO_L54P_4	AC16		
4	IO_L67N_4	Y16	NC	
4	IO_L67P_4	AA16	NC	
4	IO_L69N_4	W15	NC	
4	IO_L69P_4/VREF_4	Y15	NC	
4	IO_L70N_4	U15	NC	
4	IO_L70P_4	V15	NC	
4	IO_L72N_4	AD15	NC	
4	IO_L72P_4	AD14	NC	
4	IO_L73N_4	AB15	NC	NC
4	IO_L73P_4	AC15	NC	NC
4	IO_L91N_4/VREF_4	AA14		

BG728/BGG728 Standard BGA Package Specifications (1.27mm pitch)



NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-BAR-1
4. NO SOLDER BALL AND LAND ON A1.

728-BALL MOLDED BGA (BG728/BGG728)

Figure 6: BG728/BGG728 Standard BGA Package Specifications

Table 11: FF896 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
6	IO_L20P_6	AE26		
6	IO_L20N_6	AD26		
6	IO_L21P_6	AG30		
6	IO_L21N_6/VREF_6	AF30		
6	IO_L22P_6	AD25		
6	IO_L22N_6	AC25		
6	IO_L23P_6	AE28		
6	IO_L23N_6	AD28		
6	IO_L24P_6	AD29		
6	IO_L24N_6	AE29		
6	IO_L43P_6	AC24		
6	IO_L43N_6	AB24		
6	IO_L44P_6	AD27		
6	IO_L44N_6	AC27		
6	IO_L45P_6	AC26		
6	IO_L45N_6/VREF_6	AB26		
6	IO_L46P_6	AA23		
6	IO_L46N_6	Y23		
6	IO_L47P_6	AC28		
6	IO_L47N_6	AB28		
6	IO_L48P_6	AD30		
6	IO_L48N_6	AE30		
6	IO_L49P_6	AB25		
6	IO_L49N_6	AA25		
6	IO_L50P_6	AA24		
6	IO_L50N_6	Y24		
6	IO_L51P_6	AC29		
6	IO_L51N_6/VREF_6	AB30		
6	IO_L52P_6	Y25		
6	IO_L52N_6	W25		
6	IO_L53P_6	AB27		
6	IO_L53N_6	AA27		
6	IO_L54P_6	AA29		
6	IO_L54N_6	AB29		
6	IO_L67P_6	W23	NC	
6	IO_L67N_6	V23	NC	
6	IO_L68P_6	AA26	NC	

Table 12: FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
4	IO_L91N_4/VREF_4	AL16	
4	IO_L91P_4	AL17	
4	IO_L92N_4	AJ17	
4	IO_L92P_4	AJ16	
4	IO_L93N_4	AM15	
4	IO_L93P_4	AM14	
4	IO_L94N_4/VREF_4	AM16	
4	IO_L94P_4	AM17	
4	IO_L95N_4/GCLK3S	AF17	
4	IO_L95P_4/GCLK2P	AG17	
4	IO_L96N_4/GCLK1S	AK16	
4	IO_L96P_4/GCLK0P	AK17	
5	IO_L96N_5/GCLK7S	AK18	
5	IO_L96P_5/GCLK6P	AK19	
5	IO_L95N_5/GCLK5S	AG18	
5	IO_L95P_5/GCLK4P	AF18	
5	IO_L94N_5	AL18	
5	IO_L94P_5/VREF_5	AL19	
5	IO_L93N_5	AJ19	
5	IO_L93P_5	AJ18	
5	IO_L92N_5	AH19	
5	IO_L92P_5	AH18	
5	IO_L91N_5	AM19	
5	IO_L91P_5/VREF_5	AM20	
5	IO_L84N_5	AL21	NC
5	IO_L84P_5	AL20	NC
5	IO_L83N_5	AM22	NC
5	IO_L83P_5	AM21	NC
5	IO_L82N_5	AN18	NC
5	IO_L82P_5	AP18	NC
5	IO_L81N_5/VREF_5	AP20	NC
5	IO_L81P_5	AN19	NC
5	IO_L80N_5	AE18	NC
5	IO_L80P_5	AE19	NC
5	IO_L79N_5	AP22	NC

Table 12: FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
7	IO_L45N_7	J34	
7	IO_L44P_7	M27	
7	IO_L44N_7	L27	
7	IO_L43P_7	H31	
7	IO_L43N_7	J31	
7	IO_L30P_7	F32	
7	IO_L30N_7	G32	
7	IO_L29P_7	N25	
7	IO_L29N_7	M25	
7	IO_L28P_7	F34	
7	IO_L28N_7	G34	
7	IO_L27P_7/VREF_7	J30	
7	IO_L27N_7	H30	
7	IO_L26P_7	K28	
7	IO_L26N_7	L28	
7	IO_L25P_7	H28	
7	IO_L25N_7	J29	
7	IO_L24P_7	G29	
7	IO_L24N_7	H29	
7	IO_L23P_7	L26	
7	IO_L23N_7	K26	
7	IO_L22P_7	F33	
7	IO_L22N_7	G33	
7	IO_L21P_7/VREF_7	J28	
7	IO_L21N_7	J27	
7	IO_L20P_7	K27	
7	IO_L20N_7	J26	
7	IO_L19P_7	E31	
7	IO_L19N_7	F31	
7	IO_L06P_7	D32	
7	IO_L06N_7	E32	
7	IO_L05P_7	L25	
7	IO_L05N_7	K24	
7	IO_L04P_7	D34	
7	IO_L04N_7	E34	
7	IO_L03P_7/VREF_7	G30	

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
4	IO_L32P_4	AM14	NC	
4	IO_L33N_4	AT10	NC	
4	IO_L33P_4/VREF_4	AT9	NC	
4	IO_L34N_4	AV10	NC	
4	IO_L34P_4	AV9	NC	
4	IO_L35N_4	AH16	NC	
4	IO_L35P_4	AH17	NC	
4	IO_L36N_4	AP13	NC	
4	IO_L36P_4	AP12	NC	
4	IO_L49N_4	AU12		
4	IO_L49P_4	AU11		
4	IO_L50N_4	AK15		
4	IO_L50P_4	AJ16		
4	IO_L51N_4	AT12		
4	IO_L51P_4/VREF_4	AT11		
4	IO_L52N_4	AN15		
4	IO_L52P_4	AN14		
4	IO_L53N_4	AR12		
4	IO_L53P_4	AR13		
4	IO_L54N_4	AT14		
4	IO_L54P_4	AT13		
4	IO_L55N_4	AW11		
4	IO_L55P_4	AW10		
4	IO_L56N_4	AM15		
4	IO_L56P_4	AM16		
4	IO_L57N_4	AP15		
4	IO_L57P_4/VREF_4	AP14		
4	IO_L58N_4	AV13		
4	IO_L58P_4	AV12		
4	IO_L59N_4	AK16		
4	IO_L59P_4	AK17		
4	IO_L60N_4	AR16		
4	IO_L60P_4	AR15		
4	IO_L67N_4	AW13		
4	IO_L67P_4	AW12		
4	IO_L68N_4	AL16		

Table 14: BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000

Bank	Pin Description	Pin Number	No Connect in XC2V2000
0	IO_L92N_0	F17	
0	IO_L92P_0	F16	
0	IO_L93N_0	B18	
0	IO_L93P_0	B17	
0	IO_L94N_0/VREF_0	J17	
0	IO_L94P_0	J16	
0	IO_L95N_0/GCLK7P	E17	
0	IO_L95P_0/GCLK6S	E16	
0	IO_L96N_0/GCLK5P	A18	
0	IO_L96P_0/GCLK4S	A17	
1	IO_L96N_1/GCLK3P	C16	
1	IO_L96P_1/GCLK2S	C15	
1	IO_L95N_1/GCLK1P	H16	
1	IO_L95P_1/GCLK0S	H15	
1	IO_L94N_1	A15	
1	IO_L94P_1/VREF_1	A14	
1	IO_L93N_1	F15	
1	IO_L93P_1	F14	
1	IO_L92N_1	G15	
1	IO_L92P_1	G14	
1	IO_L91N_1	B15	
1	IO_L91P_1/VREF_1	B14	
1	IO_L78N_1	D15	
1	IO_L78P_1	E15	
1	IO_L77N_1	J15	
1	IO_L77P_1	K14	
1	IO_L76N_1	D14	
1	IO_L76P_1	D13	
1	IO_L75N_1/VREF_1	E14	
1	IO_L75P_1	E13	
1	IO_L74N_1	A13	
1	IO_L74P_1	A12	
1	IO_L73N_1	F13	
1	IO_L73P_1	F12	
1	IO_L72N_1	J14	
1	IO_L72P_1	J13	
1	IO_L71N_1	B13	

BF957 Flip-Chip BGA Package Specifications (1.27mm pitch)

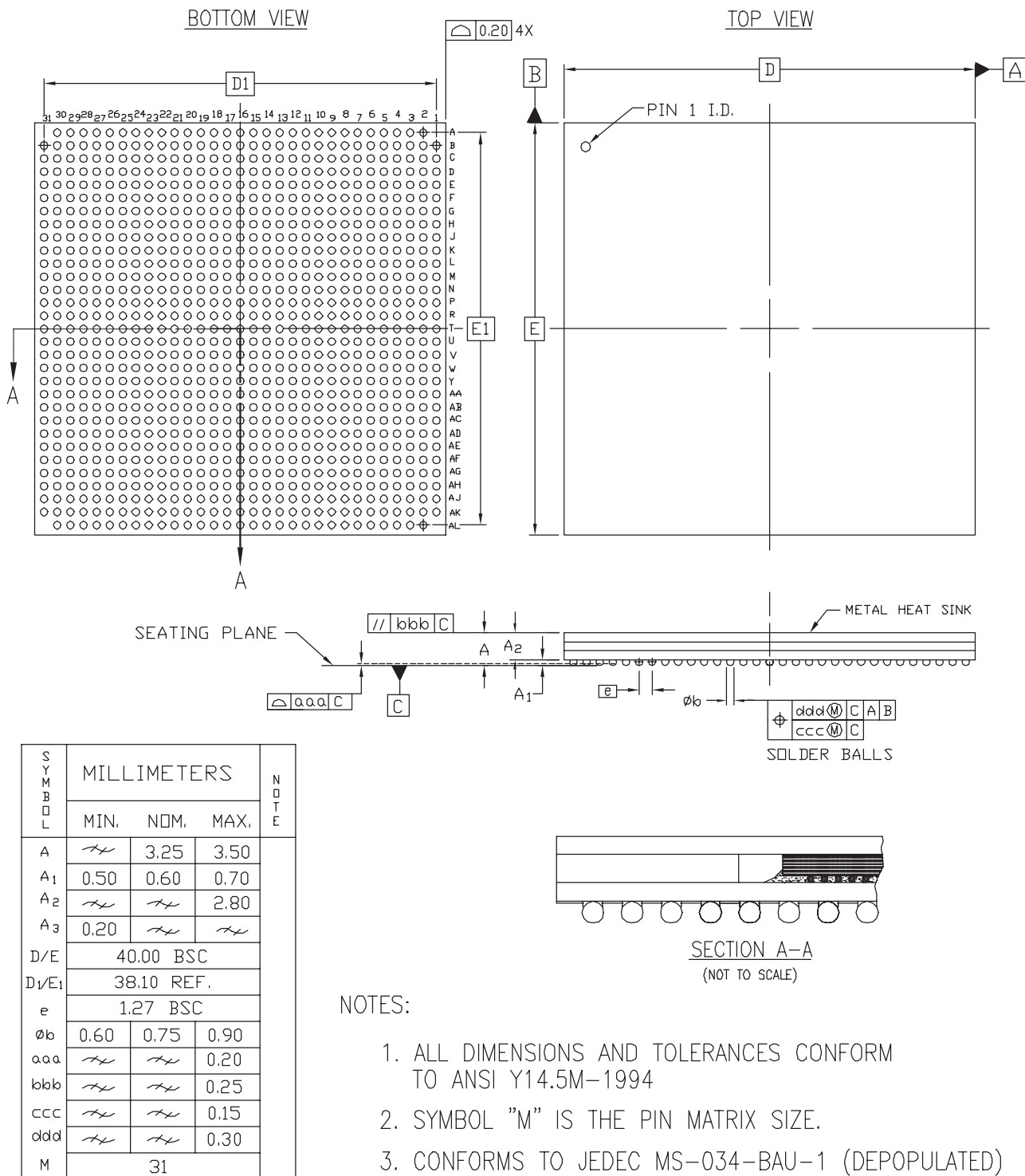


Figure 10: BF957 Flip-Chip BGA Package Specifications