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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	8448
Number of Logic Elements/Cells	-
Total RAM Bits	2654208
Number of I/O	684
Number of Gates	6000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	957-BBGA, FCBGA
Supplier Device Package	957-FCBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v6000-5bf957i

Architecture

Virtex-II Array Overview

Virtex-II devices are user-programmable gate arrays with various configurable elements. The Virtex-II architecture is optimized for high-density and high-performance logic designs. As shown in Figure 1, the programmable device is comprised of input/output blocks (IOBs) and internal configurable logic blocks (CLBs).

Programmable I/O blocks provide the interface between package pins and the internal configurable logic. Most popular and leading-edge I/O standards are supported by the programmable IOBs.

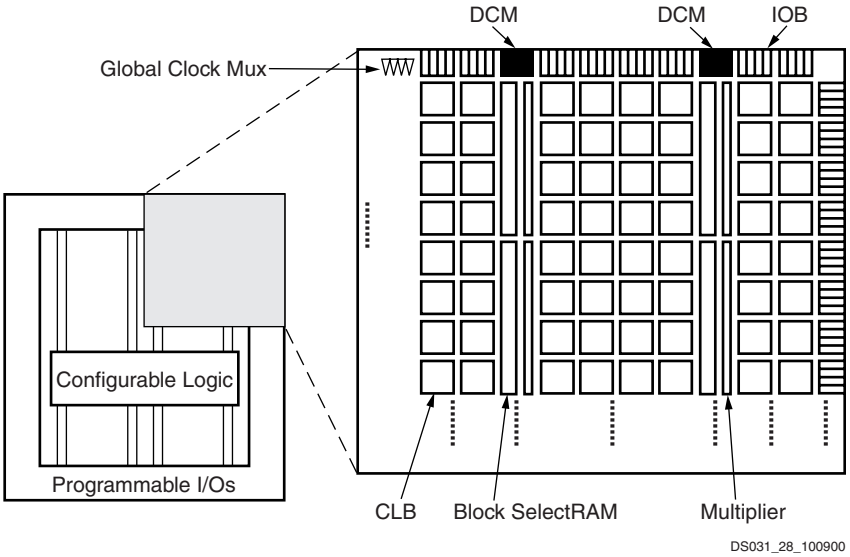

Figure 1: **Virtex-II Architecture Overview**

The internal configurable logic includes four major elements organized in a regular array.

- Configurable Logic Blocks (CLBs) provide functional elements for combinatorial and synchronous logic, including basic storage elements. BUFTs (3-state buffers) associated with each CLB element drive dedicated segmentable horizontal routing resources.
- Block SelectRAM memory modules provide large 18 Kbit storage elements of dual-port RAM.
- Multiplier blocks are 18-bit x 18-bit dedicated multipliers.
- DCM (Digital Clock Manager) blocks provide self-calibrating, fully digital solutions for clock distribution delay compensation, clock multiplication and division, coarse- and fine-grained clock phase shifting.

A new generation of programmable routing resources called Active Interconnect Technology interconnects all of these elements. The general routing matrix (GRM) is an array of routing switches. Each programmable element is tied to a switch matrix, allowing multiple connections to the general routing matrix. The overall programmable interconnection is hierarchical and designed to support high-speed designs.

All programmable elements, including the routing resources, are controlled by values stored in static memory cells. These values are loaded in the memory cells during configuration and can be reloaded to change the functions of the programmable elements.

Virtex-II Features

This section briefly describes Virtex-II features.

Input/Output Blocks (IOBs)

IOBs are programmable and can be categorized as follows:

- Input block with an optional single-data-rate or double-data-rate (DDR) register
- Output block with an optional single-data-rate or DDR register, and an optional 3-state buffer, to be driven directly or through a single or DDR register
- Bidirectional block (any combination of input and output configurations)

These registers are either edge-triggered D-type flip-flops or level-sensitive latches.

IOBs support the following single-ended I/O standards:

- LVTTL, LVCMOS (3.3V, 2.5V, 1.8V, and 1.5V)
- PCI-X compatible (133 MHz and 66 MHz) at 3.3V
- PCI compliant (66 MHz and 33 MHz) at 3.3V
- CardBus compliant (33 MHz) at 3.3V
- GTL and GTLP

3. "NO_CHANGE"

The "NO_CHANGE" option maintains the content of the output registers, regardless of the write operation. The clock edge during the write mode has no effect on the content of the data output register DO. When the port is configured as "NO_CHANGE", only a read operation loads a new value in the output register DO, as shown in Figure 33.

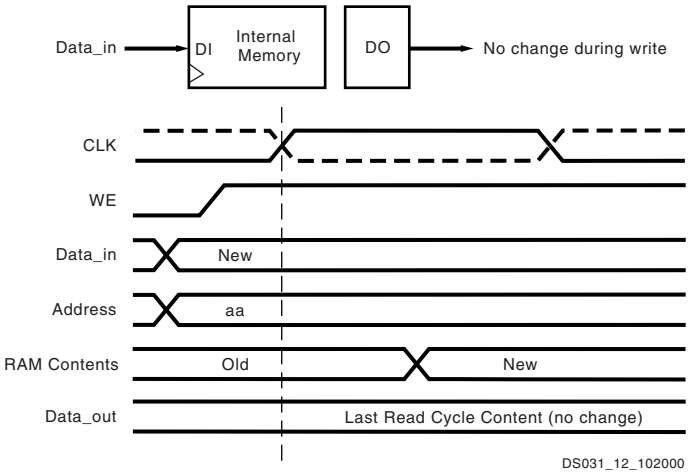

Figure 33: **NO_CHANGE Mode**

Control Pins and Attributes

Virtex-II SelectRAM memory has two independent ports with the control signals described in Table 17. All control inputs including the clock have an optional inversion.

Table 17: **Control Functions**

Control Signal	Function
CLK	Read and Write Clock
EN	Enable affects Read, Write, Set, Reset
WE	Write Enable
SSR	Set DO register to SRVAL (attribute)

Initial memory content is determined by the INIT_xx attributes. Separate attributes determine the output register value after device configuration (INIT) and SSR is asserted (SRVAL). Both attributes (INIT_B and SRVAL) are available for each port when a block SelectRAM resource is configured as dual-port RAM.

Locations

Virtex-II SelectRAM memory blocks are located in either four or six columns. The number of blocks per column depends of the device array size and is equivalent to the number of CLBs in a column divided by four. Column locations are shown in Table 18.

Table 18: **SelectRAM Memory Floor Plan**

Device	Columns	SelectRAM Blocks	
		Per Column	Total
XC2V40	2	2	4
XC2V80	2	4	8
XC2V250	4	6	24
XC2V500	4	8	32
XC2V1000	4	10	40
XC2V1500	4	12	48
XC2V2000	4	14	56
XC2V3000	6	16	96
XC2V4000	6	20	120
XC2V6000	6	24	144
XC2V8000	6	28	168

Configuration

Virtex-II devices are configured by loading application specific configuration data into the internal configuration memory. Configuration is carried out using a subset of the device pins, some of which are dedicated, while others can be re-used as general purpose inputs and outputs once configuration is complete.

Depending on the system design, several configuration modes are supported, selectable via mode pins. The mode pins M2, M1 and M0 are dedicated pins. The M2, M1, and M0 mode pins should be set at a constant DC voltage level, either through pull-up or pull-down resistors, or tied directly to ground or V_{CCAUX}. The mode pins should not be toggled during and after configuration.

An additional pin, HSWAP_EN is used in conjunction with the mode pins to select whether user I/O pins have pull-ups during configuration. By default, HSWAP_EN is tied High (internal pull-up) which shuts off the pull-ups on the user I/O pins during configuration. When HSWAP_EN is tied Low, user I/Os have pull-ups during configuration. Other dedicated pins are CCLK (the configuration clock pin), DONE, PROG_B, and the Boundary-Scan pins: TDI, TDO, TMS, and TCK. Depending on the configuration mode chosen, CCLK can be an output generated by the FPGA, or an input accepting an externally generated clock. The configuration pins and Boundary-Scan pins are independent of the V_{CCO}. The auxiliary power supply (V_{CCAUX}) of 3.3V is used for these pins. All configuration pins are LVTTL 12 mA. (See Virtex-II DC Characteristics in Module 3.)

A persist option is available which can be used to force the configuration pins to retain their configuration function even after device configuration is complete. If the persist option is not selected then the configuration pins with the exception of CCLK, PROG_B, and DONE can be used as user I/O in normal operation. The persist option does not apply to the Boundary-Scan related pins. The persist feature is valuable in applications which employ partial reconfiguration or reconfiguration on the fly.

Configuration Modes

Virtex-II supports the following five configuration modes:

- Slave-Serial Mode
- Master-Serial Mode
- Slave SelectMAP Mode
- Master SelectMAP Mode
- Boundary-Scan (JTAG, IEEE 1532) Mode

A detailed description of configuration modes is provided in the Virtex-II *User Guide*.

Slave-Serial Mode

In slave-serial mode, the FPGA receives configuration data in bit-serial form from a serial PROM or other serial source of configuration data. The CCLK pin on the FPGA is an input in this mode. The serial bitstream must be setup at the DIN input pin a short time before each rising edge of the externally generated CCLK.

Multiple FPGAs can be daisy-chained for configuration from a single source. After a particular FPGA has been configured, the data for the next device is routed internally to the DOUT pin. The data on the DOUT pin changes on the falling edge of CCLK.

Slave-serial mode is selected by applying <111> to the mode pins (M2, M1, M0). A weak pull-up on the mode pins makes slave serial the default mode if the pins are left unconnected.

Master-Serial Mode

In master-serial mode, the CCLK pin is an output pin. It is the Virtex-II FPGA device that drives the configuration clock on the CCLK pin to a Xilinx Serial PROM which in turn feeds bit-serial data to the DIN input. The FPGA accepts this data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the falling CCLK edge.

The interface is identical to slave serial except that an internal oscillator is used to generate the configuration clock (CCLK). A wide range of frequencies can be selected for CCLK which always starts at a slow default frequency. Configuration bits then switch CCLK to a higher frequency for the remainder of the configuration.

Slave SelectMAP Mode

The SelectMAP mode is the fastest configuration option. Byte-wide data is written into the Virtex-II FPGA device with a BUSY flag controlling the flow of data. An external data source provides a byte stream, CCLK, an active Low Chip Select (CS_B) signal and a Write signal (RDWR_B). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low. Data can also be read using the SelectMAP mode. If RDWR_B is asserted, configuration data is read out of the FPGA as part of a readback operation.

After configuration, the pins of the SelectMAP port can be used as additional user I/O. Alternatively, the port can be retained to permit high-speed 8-bit readback using the persist option.

Multiple Virtex-II FPGAs can be configured using the SelectMAP mode, and be made to start-up simultaneously. To configure multiple devices in this way, wire the individual CCLK, Data, RDWR_B, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by deasserting the CS_B pin of each device in turn and writing the appropriate data.

Master SelectMAP Mode

This mode is a master version of the SelectMAP mode. The device is configured byte-wide on a CCLK supplied by the

Table 5: **Minimum Power On Current Required for Virtex-II Devices**

	Device (mA)							
	XC2V40, XC2V80, XC2V250, XC2V500	XC2V1000	XC2V1500	XC2V2000	XC2V3000	XC2V4000	XC2V6000	XC2V8000
$I_{CCINTMIN}$	200	250	350	400	500	650	800	1100
$I_{CCAUXMIN}$	100	100	100	100	100	100	100	100
I_{CCOMIN}	50	50	100	100	100	100	100	100

Notes:
1. Values specified for power on current parameters are Commercial Grade. For Industrial Grade values, multiply Commercial Grade values by 1.25.
2. I_{CCOMIN} values listed here apply to the entire device (all banks).

General Power Supply Requirements

Proper decoupling of all FPGA power supplies is sessential. Consult Xilinx Application Note **XAPP623** for detailed information on power distribution system design.

V_{CCAUX} powers critical resources in the FPGA. Thus, V_{CCAUX} is especially susceptible to power supply noise.

Changes in V_{CCAUX} voltage outside of 200 mV peak to peak should take place at a rate no faster than 10 mV per millisecond. Techniques to help reduce jitter and period distortion are provided in Xilinx Answer Record 13756, available at **www.support.xilinx.com**.

V_{CCAUX} can share a power plane with 3.3V V_{CCO}, but only if V_{CCO} does not have excessive noise. Using simultaneously switching output (SSO) limits are essential for keeping power supply noise to a minimum. Refer to **XAPP689**, "Managing Ground Bounce in Large FPGAs," to determine the number of simultaneously switching outputs allowed per bank at the package level.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 6: **DC Input and Output Levels**

Input/Output	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
Standard	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTL(1)	– 0.5	0.8	2.0	3.6	0.4	2.4	24	– 24
LVCMOS33	– 0.5	0.8	2.0	3.6	0.4	V_{CCO} – 0.4	24	– 24
LVCMOS25	– 0.5	0.7	1.7	2.7	0.4	V_{CCO} – 0.4	24	– 24
LVCMOS18	– 0.5	35% V_{CCO}	65% V_{CCO}	1.95	0.4	V_{CCO} – 0.4	16	– 16
LVCMOS15	– 0.5	35% V_{CCO}	65% V_{CCO}	1.7	0.4	V_{CCO} – 0.4	16	– 16
PCI33_3	– 0.5	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
PCI66_3	– 0.5	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
PCI–X	– 0.5	Note 2	Note 2	Note 2	Note 2	Note 2	Note 2	Note 2
GTLP	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.5	0.6	n/a	36	n/a
GTL	– 0.5	V_{REF} – 0.05	V_{REF} + 0.05	V_{CCO} + 0.5	0.4	n/a	40	n/a
HSTL I	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.5	0.4	V_{CCO} – 0.4	8	– 8
HSTL II	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.5	0.4	V_{CCO} – 0.4	16	– 16
HSTL III	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.5	0.4	V_{CCO} – 0.4	24	– 8
HSTL IV	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.5	0.4	V_{CCO} – 0.4	48	– 8

Multiplier Switching Characteristics

Table 24: **Multiplier Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Propagation Delay to Output Pin					
Input to Pin 35	T_{MULT_P35}	4.66	8.50	10.36	ns, Max
Input to Pin 34	T_{MULT_P34}	4.57	8.33	10.15	ns, Max
Input to Pin 33	T_{MULT_P33}	4.47	8.16	9.95	ns, Max
Input to Pin 32	T_{MULT_P32}	4.37	7.99	9.74	ns, Max
Input to Pin 31	T_{MULT_P31}	4.28	7.82	9.53	ns, Max
Input to Pin 30	T_{MULT_P30}	4.18	7.65	9.33	ns, Max
Input to Pin 29	T_{MULT_P29}	4.08	7.48	9.12	ns, Max
Input to Pin 28	T_{MULT_P28}	3.99	7.31	8.91	ns, Max
Input to Pin 27	T_{MULT_P27}	3.89	7.14	8.70	ns, Max
Input to Pin 26	T_{MULT_P26}	3.79	6.97	8.50	ns, Max
Input to Pin 25	T_{MULT_P25}	3.69	6.80	8.29	ns, Max
Input to Pin 24	T_{MULT_P24}	3.60	6.63	8.08	ns, Max
Input to Pin 23	T_{MULT_P23}	3.50	6.46	7.88	ns, Max
Input to Pin 22	T_{MULT_P22}	3.40	6.29	7.67	ns, Max
Input to Pin 21	T_{MULT_P21}	3.31	6.12	7.46	ns, Max
Input to Pin 20	T_{MULT_P20}	3.21	5.95	7.26	ns, Max
Input to Pin 19	T_{MULT_P19}	3.11	5.78	7.05	ns, Max
Input to Pin 18	T_{MULT_P18}	3.02	5.61	6.84	ns, Max
Input to Pin 17	T_{MULT_P17}	2.92	5.44	6.63	ns, Max
Input to Pin 16	T_{MULT_P16}	2.82	5.27	6.43	ns, Max
Input to Pin 15	T_{MULT_P15}	2.72	5.10	6.22	ns, Max
Input to Pin 14	T_{MULT_P14}	2.63	4.93	6.01	ns, Max
Input to Pin 13	T_{MULT_P13}	2.53	4.76	5.81	ns, Max
Input to Pin 12	T_{MULT_P12}	2.43	4.59	5.60	ns, Max
Input to Pin 11	T_{MULT_P11}	2.34	4.42	5.39	ns, Max
Input to Pin 10	T_{MULT_P10}	2.24	4.25	5.19	ns, Max
Input to Pin 9	T_{MULT_P9}	2.14	4.08	4.98	ns, Max
Input to Pin 8	T_{MULT_P8}	2.05	3.91	4.77	ns, Max
Input to Pin 7	T_{MULT_P7}	1.95	3.74	4.56	ns, Max
Input to Pin 6	T_{MULT_P6}	1.85	3.57	4.36	ns, Max
Input to Pin 5	T_{MULT_P5}	1.75	3.40	4.15	ns, Max
Input to Pin 4	T_{MULT_P4}	1.66	3.23	3.94	ns, Max
Input to Pin 3	T_{MULT_P3}	1.56	3.06	3.74	ns, Max
Input to Pin 2	T_{MULT_P2}	1.46	2.89	3.53	ns, Max
Input to Pin 1	T_{MULT_P1}	1.37	2.72	3.32	ns, Max
Input to Pin 0	T_{MULT_P0}	1.27	2.55	3.12	ns, Max

Table 25: **Pipelined Multiplier Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Setup and Hold Times Before/After Clock					
Data Inputs	$T_{MULIDCK}/T_{MULCKID}$	3.00/ 0.00	3.45/ 0.00	3.89/ 0.00	ns, Max
Clock Enable	$T_{MULIDCK\_CE}/T_{MULCKID\_CE}$	0.72/ 0.00	0.80/ 0.00	0.86/ 0.00	ns, Max
Reset	$T_{MULIDCK\_RST}/T_{MULCKID\_RST}$	0.72/ 0.00	0.80/ 0.00	0.86/ 0.00	ns, Max
Clock to Output Pin					
Clock to Pin 35	T_{MULTCK_P35}	3.05	6.91	8.12	ns, Max
Clock to Pin 34	T_{MULTCK_P34}	2.95	6.75	7.93	ns, Max
Clock to Pin 33	T_{MULTCK_P33}	2.85	6.59	7.74	ns, Max
Clock to Pin 32	T_{MULTCK_P32}	2.76	6.43	7.56	ns, Max
Clock to Pin 31	T_{MULTCK_P31}	2.66	6.27	7.37	ns, Max
Clock to Pin 30	T_{MULTCK_P30}	2.56	6.11	7.19	ns, Max
Clock to Pin 29	T_{MULTCK_P29}	2.47	5.95	7.00	ns, Max
Clock to Pin 28	T_{MULTCK_P28}	2.37	5.79	6.81	ns, Max
Clock to Pin 27	T_{MULTCK_P27}	2.27	5.63	6.63	ns, Max
Clock to Pin 26	T_{MULTCK_P26}	2.17	5.47	6.44	ns, Max
Clock to Pin 25	T_{MULTCK_P25}	2.08	5.31	6.26	ns, Max
Clock to Pin 24	T_{MULTCK_P24}	1.98	5.15	6.07	ns, Max
Clock to Pin 23	T_{MULTCK_P23}	1.88	4.99	5.88	ns, Max
Clock to Pin 22	T_{MULTCK_P22}	1.79	4.83	5.70	ns, Max
Clock to Pin 21	T_{MULTCK_P21}	1.69	4.67	5.51	ns, Max
Clock to Pin 20	T_{MULTCK_P20}	1.59	4.51	5.33	ns, Max
Clock to Pin 19	T_{MULTCK_P19}	1.50	4.35	5.14	ns, Max
Clock to Pin 18	T_{MULTCK_P18}	1.40	4.19	4.95	ns, Max
Clock to Pin 17	T_{MULTCK_P17}	1.30	4.03	4.77	ns, Max
Clock to Pin 16	T_{MULTCK_P16}	1.20	3.87	4.58	ns, Max
Clock to Pin 15	T_{MULTCK_P15}	1.11	3.71	4.40	ns, Max
Clock to Pin 14	T_{MULTCK_P14}	1.01	3.55	4.21	ns, Max
Clock to Pin 13	T_{MULTCK_P13}	0.91	3.39	4.02	ns, Max
Clock to Pin 12	T_{MULTCK_P12}	0.91	3.23	3.84	ns, Max
Clock to Pin 11	T_{MULTCK_P11}	0.91	3.07	3.65	ns, Max
Clock to Pin 10	T_{MULTCK_P10}	0.91	2.91	3.47	ns, Max
Clock to Pin 9	T_{MULTCK_P9}	0.91	2.75	3.28	ns, Max
Clock to Pin 8	T_{MULTCK_P8}	0.91	2.59	3.09	ns, Max
Clock to Pin 7	T_{MULTCK_P7}	0.91	2.43	2.91	ns, Max
Clock to Pin 6	T_{MULTCK_P6}	0.91	2.27	2.72	ns, Max
Clock to Pin 5	T_{MULTCK_P5}	0.91	2.11	2.54	ns, Max
Clock to Pin 4	T_{MULTCK_P4}	0.91	1.95	2.35	ns, Max
Clock to Pin 3	T_{MULTCK_P3}	0.91	1.79	2.16	ns, Max
Clock to Pin 2	T_{MULTCK_P2}	0.91	1.63	1.98	ns, Max
Clock to Pin 1	T_{MULTCK_P1}	0.91	1.47	1.79	ns, Max
Clock to Pin 0	T_{MULTCK_P0}	0.91	1.31	1.61	ns, Max

Table 27: **Enhanced Pipelined Multiplier Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Setup and Hold Times Before/After Clock					
Data Inputs	$T_{MULIDCK}/T_{MULCKID}$	3.00/0.00	3.45/0.00	3.89/0.00	ns, Max
Clock Enable	$T_{MULIDCK\_CE}/T_{MULCKID\_CE}$	0.72/0.00	0.80/0.00	0.86/0.00	ns, Max
Reset	$T_{MULIDCK\_RST}/T_{MULCKID\_RST}$	0.72/0.00	0.80/0.00	0.86/0.00	ns, Max
Clock to Output Pin					
Clock to Pin 35	$T_{MULTCK1\_P35}$	3.05	3.25	3.74	ns, Max
Clock to Pin 34	$T_{MULTCK1\_P34}$	2.95	3.14	3.61	ns, Max
Clock to Pin 33	$T_{MULTCK1\_P33}$	2.85	3.04	3.49	ns, Max
Clock to Pin 32	$T_{MULTCK1\_P32}$	2.76	2.93	3.37	ns, Max
Clock to Pin 31	$T_{MULTCK1\_P31}$	2.66	2.82	3.25	ns, Max
Clock to Pin 30	$T_{MULTCK1\_P30}$	2.56	2.72	3.12	ns, Max
Clock to Pin 29	$T_{MULTCK1\_P29}$	2.47	2.61	3.00	ns, Max
Clock to Pin 28	$T_{MULTCK1\_P28}$	2.37	2.50	2.88	ns, Max
Clock to Pin 27	$T_{MULTCK1\_P27}$	2.27	2.40	2.75	ns, Max
Clock to Pin 26	$T_{MULTCK1\_P26}$	2.17	2.29	2.63	ns, Max
Clock to Pin 25	$T_{MULTCK1\_P25}$	2.08	2.18	2.51	ns, Max
Clock to Pin 24	$T_{MULTCK1\_P24}$	1.98	2.07	2.38	ns, Max
Clock to Pin 23	$T_{MULTCK1\_P23}$	1.88	1.97	2.26	ns, Max
Clock to Pin 22	$T_{MULTCK1\_P22}$	1.79	1.86	2.14	ns, Max
Clock to Pin 21	$T_{MULTCK1\_P21}$	1.69	1.75	2.02	ns, Max
Clock to Pin 20	$T_{MULTCK1\_P20}$	1.59	1.65	1.89	ns, Max
Clock to Pin 19	$T_{MULTCK1\_P19}$	1.50	1.54	1.77	ns, Max
Clock to Pin 18	$T_{MULTCK1\_P18}$	1.40	1.43	1.65	ns, Max
Clock to Pin 17	$T_{MULTCK1\_P17}$	1.30	1.33	1.52	ns, Max
Clock to Pin 16	$T_{MULTCK1\_P16}$	1.20	1.22	1.40	ns, Max
Clock to Pin 15	$T_{MULTCK1\_P15}$	1.11	1.11	1.28	ns, Max
Clock to Pin 14	$T_{MULTCK1\_P14}$	1.01	1.00	1.15	ns, Max
Clock to Pin 13	$T_{MULTCK1\_P13}$	0.91	1.00	1.15	ns, Max
Clock to Pin 12	$T_{MULTCK1\_P12}$	0.91	1.00	1.15	ns, Max
Clock to Pin 11	$T_{MULTCK1\_P11}$	0.91	1.00	1.15	ns, Max
Clock to Pin 10	$T_{MULTCK1\_P10}$	0.91	1.00	1.15	ns, Max
Clock to Pin 9	$T_{MULTCK1\_P9}$	0.91	1.00	1.15	ns, Max
Clock to Pin 8	$T_{MULTCK1\_P8}$	0.91	1.00	1.15	ns, Max
Clock to Pin 7	$T_{MULTCK1\_P7}$	0.91	1.00	1.15	ns, Max
Clock to Pin 6	$T_{MULTCK1\_P6}$	0.91	1.00	1.15	ns, Max
Clock to Pin 5	$T_{MULTCK1\_P5}$	0.91	1.00	1.15	ns, Max
Clock to Pin 4	$T_{MULTCK1\_P4}$	0.91	1.00	1.15	ns, Max
Clock to Pin 3	$T_{MULTCK1\_P3}$	0.91	1.00	1.15	ns, Max
Clock to Pin 2	$T_{MULTCK1\_P2}$	0.91	1.00	1.15	ns, Max
Clock to Pin 1	$T_{MULTCK1\_P1}$	0.91	1.00	1.15	ns, Max
Clock to Pin 0	$T_{MULTCK1\_P0}$	0.91	1.00	1.15	ns, Max

Virtex-II Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Setup and Hold for LVTTL Standard, *With* DCM

Table 36: **Global Clock Setup and Hold for LVTTL Standard, *With* DCM**

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in IOB Input Switching Characteristics Standard Adjustments, page 11.						
No Delay Global Clock and IFF with DCM	T_{PSDCM}/T_{PHDCM}	XC2V40	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		XC2V80	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		XC2V250	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		XC2V500	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		XC2V1000	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		XC2V1500	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		XC2V2000	1.70/–0.90	1.70/–0.90	1.96/–0.76	ns
		XC2V3000	1.70/–0.90	1.70/–0.90	1.96/–0.76	ns
		XC2V4000	1.70/–0.90	1.70/–0.90	1.96/–0.76	ns
		XC2V6000	1.70/–0.90	1.70/–0.90	1.96/–0.76	ns
		XC2V8000		1.70/–0.90	1.96/–0.76	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.

Table 5: **CS144/CSG144 — XC2V40, XC2V80, and XC2V250**

Bank	Pin Description	Pin Number	No Connect in the XC2V40
6	IO_L01P_6	L3	
6	IO_L01N_6	L2	
6	IO_L02P_6/VRN_6	L1	
6	IO_L02N_6/VRP_6	K3	
6	IO_L03P_6	K2	
6	IO_L03N_6/VREF_6	K1	
6	IO_L94P_6	J2	
6	IO_L94N_6	H4	
6	IO_L96P_6	H3	
6	IO_L96N_6	H1	
7	IO_L96P_7	G4	
7	IO_L96N_7	G3	
7	IO_L94P_7	G1	
7	IO_L94N_7	F1	
7	IO_L93P_7/VREF_7	F2	NC
7	IO_L93N_7	F4	NC
7	IO_L03P_7/VREF_7	E2	
7	IO_L03N_7	E3	
7	IO_L02P_7/VRN_7	E4	
7	IO_L02N_7/VRP_7	D1	
7	IO_L01P_7	D2	
7	IO_L01N_7	D3	
0	VCCO_0	B5	
0	VCCO_0	C3	
1	VCCO_1	A11	
1	VCCO_1	A9	
2	VCCO_2	F10	
2	VCCO_2	C12	
3	VCCO_3	L12	
3	VCCO_3	J12	
4	VCCO_4	M9	
4	VCCO_4	L11	
5	VCCO_5	N3	
5	VCCO_5	N5	
6	VCCO_6	J3	
6	VCCO_6	M1	
7	VCCO_7	D4	
7	VCCO_7	F3	

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
2	IO_L69P_2/VREF_2	L18	NC	
2	IO_L70N_2	K23	NC	
2	IO_L70P_2	L24	NC	
2	IO_L72N_2	K22	NC	
2	IO_L72P_2	L22	NC	
2	IO_L73N_2	L21	NC	NC
2	IO_L73P_2	L20	NC	NC
2	IO_L91N_2	M23		
2	IO_L91P_2	N24		
2	IO_L93N_2	M21		
2	IO_L93P_2/VREF_2	M22		
2	IO_L94N_2	M19		
2	IO_L94P_2	M20		
2	IO_L96N_2	M17		
2	IO_L96P_2	M18		
3	IO_L96N_3	N23		
3	IO_L96P_3	N22		
3	IO_L94N_3	N20		
3	IO_L94P_3	N21		
3	IO_L93N_3/VREF_3	N19		
3	IO_L93P_3	N18		
3	IO_L91N_3	N17		
3	IO_L91P_3	P17		
3	IO_L73N_3	P24	NC	NC
3	IO_L73P_3	R24	NC	NC
3	IO_L72N_3	R23	NC	
3	IO_L72P_3	R22	NC	
3	IO_L70N_3	P22	NC	
3	IO_L70P_3	P21	NC	
3	IO_L69N_3/VREF_3	P20	NC	
3	IO_L69P_3	P18	NC	
3	IO_L67N_3	T24	NC	
3	IO_L67P_3	U24	NC	
3	IO_L54N_3	T23		
3	IO_L54P_3	T22		

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
2	IO_L19P_2	F26
2	IO_L21N_2	F27
2	IO_L21P_2/VREF_2	G27
2	IO_L22N_2	G23
2	IO_L22P_2	H23
2	IO_L24N_2	G25
2	IO_L24P_2	G26
2	IO_L25N_2	H21
2	IO_L25P_2	J21
2	IO_L27N_2	H22
2	IO_L27P_2/VREF_2	J22
2	IO_L28N_2	H24
2	IO_L28P_2	H25
2	IO_L30N_2	H27
2	IO_L30P_2	J27
2	IO_L43N_2	J23
2	IO_L43P_2	J24
2	IO_L45N_2	J25
2	IO_L45P_2/VREF_2	J26
2	IO_L46N_2	K20
2	IO_L46P_2	K21
2	IO_L48N_2	K22
2	IO_L48P_2	K23
2	IO_L49N_2	K24
2	IO_L49P_2	K25
2	IO_L51N_2	K26
2	IO_L51P_2/VREF_2	K27
2	IO_L52N_2	L20
2	IO_L52P_2	M20
2	IO_L54N_2	L21
2	IO_L54P_2	L22
2	IO_L67N_2	L24
2	IO_L67P_2	L25
2	IO_L69N_2	L26
2	IO_L69P_2/VREF_2	L27
2	IO_L70N_2	M19

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
NA	GND	T12
NA	GND	R16
NA	GND	R15
NA	GND	R14
NA	GND	R13
NA	GND	R12
NA	GND	P27
NA	GND	P24
NA	GND	P19
NA	GND	P16
NA	GND	P15
NA	GND	P14
NA	GND	P13
NA	GND	P12
NA	GND	P9
NA	GND	P4
NA	GND	P1
NA	GND	N16
NA	GND	N15
NA	GND	N14
NA	GND	N13
NA	GND	N12
NA	GND	M16
NA	GND	M15
NA	GND	M14
NA	GND	M13
NA	GND	M12
NA	GND	L23
NA	GND	L5
NA	GND	J14
NA	GND	H26
NA	GND	H20
NA	GND	H8
NA	GND	H2
NA	GND	G21
NA	GND	G7

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
6	IO_L20P_6	AE26		
6	IO_L20N_6	AD26		
6	IO_L21P_6	AG30		
6	IO_L21N_6/VREF_6	AF30		
6	IO_L22P_6	AD25		
6	IO_L22N_6	AC25		
6	IO_L23P_6	AE28		
6	IO_L23N_6	AD28		
6	IO_L24P_6	AD29		
6	IO_L24N_6	AE29		
6	IO_L43P_6	AC24		
6	IO_L43N_6	AB24		
6	IO_L44P_6	AD27		
6	IO_L44N_6	AC27		
6	IO_L45P_6	AC26		
6	IO_L45N_6/VREF_6	AB26		
6	IO_L46P_6	AA23		
6	IO_L46N_6	Y23		
6	IO_L47P_6	AC28		
6	IO_L47N_6	AB28		
6	IO_L48P_6	AD30		
6	IO_L48N_6	AE30		
6	IO_L49P_6	AB25		
6	IO_L49N_6	AA25		
6	IO_L50P_6	AA24		
6	IO_L50N_6	Y24		
6	IO_L51P_6	AC29		
6	IO_L51N_6/VREF_6	AB30		
6	IO_L52P_6	Y25		
6	IO_L52N_6	W25		
6	IO_L53P_6	AB27		
6	IO_L53N_6	AA27		
6	IO_L54P_6	AA29		
6	IO_L54N_6	AB29		
6	IO_L67P_6	W23	NC	
6	IO_L67N_6	V23	NC	
6	IO_L68P_6	AA26	NC	

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
7	IO_L95N_7	R24		
7	IO_L94P_7	R29		
7	IO_L94N_7	T29		
7	IO_L93P_7/VREF_7	R27		
7	IO_L93N_7	P27		
7	IO_L92P_7	R23		
7	IO_L92N_7	P23		
7	IO_L91P_7	N30		
7	IO_L91N_7	P30		
7	IO_L78P_7	P26	NC	NC
7	IO_L78N_7	R26	NC	NC
7	IO_L77P_7	R22	NC	NC
7	IO_L77N_7	P22	NC	NC
7	IO_L76P_7	N29	NC	NC
7	IO_L76N_7	P29	NC	NC
7	IO_L75P_7/VREF_7	N27	NC	NC
7	IO_L75N_7	N26	NC	NC
7	IO_L74P_7	P25	NC	NC
7	IO_L74N_7	N25	NC	NC
7	IO_L73P_7	L30	NC	NC
7	IO_L73N_7	M30	NC	NC
7	IO_L72P_7	L28	NC	
7	IO_L72N_7	M28	NC	
7	IO_L71P_7	N24	NC	
7	IO_L71N_7	M24	NC	
7	IO_L70P_7	L29	NC	
7	IO_L70N_7	M29	NC	
7	IO_L69P_7/VREF_7	M27	NC	
7	IO_L69N_7	L27	NC	
7	IO_L68P_7	N23	NC	
7	IO_L68N_7	M23	NC	
7	IO_L67P_7	J30	NC	
7	IO_L67N_7	K30	NC	
7	IO_L54P_7	K26		
7	IO_L54N_7	L26		
7	IO_L53P_7	M25		
7	IO_L53N_7	L25		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
NA	GND	M5		
NA	GND	K28		
NA	GND	K3		
NA	GND	H30		
NA	GND	H1		
NA	GND	G17		
NA	GND	G14		
NA	GND	F25		
NA	GND	F6		
NA	GND	E26		
NA	GND	E19		
NA	GND	E12		
NA	GND	E5		
NA	GND	D27		
NA	GND	D4		
NA	GND	C28		
NA	GND	C21		
NA	GND	C10		
NA	GND	C3		
NA	GND	B29		
NA	GND	B2		
NA	GND	A23		
NA	GND	A8		

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
1	IO_L69P_1	F13	
1	IO_L68N_1	C11	
1	IO_L68P_1	C12	
1	IO_L67N_1	B11	
1	IO_L67P_1	B12	
1	IO_L60N_1	F11	NC
1	IO_L60P_1	F12	NC
1	IO_L54N_1	D10	
1	IO_L54P_1	D11	
1	IO_L53N_1	G12	
1	IO_L53P_1	G13	
1	IO_L52N_1	B9	
1	IO_L52P_1	B10	
1	IO_L51N_1/VREF_1	B8	
1	IO_L51P_1	A9	
1	IO_L50N_1	K14	
1	IO_L50P_1	K13	
1	IO_L49N_1	A6	
1	IO_L49P_1	A7	
1	IO_L30N_1	D9	
1	IO_L30P_1	C9	
1	IO_L29N_1	H13	
1	IO_L29P_1	H12	
1	IO_L28N_1	C7	
1	IO_L28P_1	C8	
1	IO_L27N_1/VREF_1	E11	
1	IO_L27P_1	E10	
1	IO_L26N_1	J13	
1	IO_L26P_1	K12	
1	IO_L25N_1	B6	
1	IO_L25P_1	B7	
1	IO_L24N_1	E8	
1	IO_L24P_1	E9	
1	IO_L23N_1	G10	
1	IO_L23P_1	G11	
1	IO_L22N_1	A4	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
6	IO_L71P_6	AD34	
6	IO_L71N_6	AC34	
6	IO_L72P_6	AC31	
6	IO_L72N_6	AD31	
6	IO_L73P_6	Y27	
6	IO_L73N_6	W27	
6	IO_L74P_6	AB29	
6	IO_L74N_6	AA29	
6	IO_L75P_6	AB31	
6	IO_L75N_6/VREF_6	AA31	
6	IO_L76P_6	Y28	
6	IO_L76N_6	Y29	
6	IO_L77P_6	AB33	
6	IO_L77N_6	AA33	
6	IO_L78P_6	AA30	
6	IO_L78N_6	AB30	
6	IO_L79P_6	W24	NC
6	IO_L79N_6	V24	NC
6	IO_L80P_6	AB34	NC
6	IO_L80N_6	AA34	NC
6	IO_L81P_6	W33	NC
6	IO_L81N_6/VREF_6	Y34	NC
6	IO_L82P_6	W25	NC
6	IO_L82N_6	V25	NC
6	IO_L83P_6	Y32	NC
6	IO_L83N_6	AA32	NC
6	IO_L84P_6	W29	NC
6	IO_L84N_6	V29	NC
6	IO_L91P_6	W28	
6	IO_L91N_6	V28	
6	IO_L92P_6	V33	
6	IO_L92N_6	V34	
6	IO_L93P_6	Y31	
6	IO_L93N_6/VREF_6	W31	
6	IO_L94P_6	V26	
6	IO_L94N_6	V27	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
7	IO_L03N_7	F30	
7	IO_L02P_7/VRN_7	K25	
7	IO_L02N_7/VRP_7	J25	
7	IO_L01P_7	D33	
7	IO_L01N_7	E33	
0	VCCO_0	M22	
0	VCCO_0	M21	
0	VCCO_0	M20	
0	VCCO_0	M19	
0	VCCO_0	M18	
0	VCCO_0	L23	
0	VCCO_0	L22	
0	VCCO_0	L21	
0	VCCO_0	L20	
0	VCCO_0	E20	
0	VCCO_0	D28	
0	VCCO_0	A25	
0	VCCO_0	A19	
1	VCCO_1	M17	
1	VCCO_1	M16	
1	VCCO_1	M15	
1	VCCO_1	M14	
1	VCCO_1	M13	
1	VCCO_1	L15	
1	VCCO_1	L14	
1	VCCO_1	L13	
1	VCCO_1	L12	
1	VCCO_1	E15	
1	VCCO_1	D7	
1	VCCO_1	A16	
1	VCCO_1	A10	
2	VCCO_2	U12	
2	VCCO_2	T12	
2	VCCO_2	T1	
2	VCCO_2	R12	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
NA	GND	V19	
NA	GND	V18	
NA	GND	V17	
NA	GND	V16	
NA	GND	V15	
NA	GND	V14	
NA	GND	U21	
NA	GND	U20	
NA	GND	U19	
NA	GND	U18	
NA	GND	U17	
NA	GND	U16	
NA	GND	U15	
NA	GND	U14	
NA	GND	T26	
NA	GND	T21	
NA	GND	T20	
NA	GND	T19	
NA	GND	T18	
NA	GND	T17	
NA	GND	T16	
NA	GND	T15	
NA	GND	T14	
NA	GND	T9	
NA	GND	R33	
NA	GND	R21	
NA	GND	R20	
NA	GND	R19	
NA	GND	R18	
NA	GND	R17	
NA	GND	R16	
NA	GND	R15	
NA	GND	R14	
NA	GND	R2	
NA	GND	P28	
NA	GND	P21	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
7	IO_L74P_7	U31		
7	IO_L74N_7	T31		
7	IO_L73P_7	R38		
7	IO_L73N_7	T38		
7	IO_L72P_7	T33		
7	IO_L72N_7	U33		
7	IO_L71P_7	U30		
7	IO_L71N_7	T30		
7	IO_L70P_7	R37		
7	IO_L70N_7	T37		
7	IO_L69P_7/VREF_7	R36		
7	IO_L69N_7	T36		
7	IO_L68P_7	T32		
7	IO_L68N_7	R32		
7	IO_L67P_7	P39		
7	IO_L67N_7	R39		
7	IO_L60P_7	R35		
7	IO_L60N_7	T35		
7	IO_L59P_7	U28		
7	IO_L59N_7	T28		
7	IO_L58P_7	N37		
7	IO_L58N_7	P37		
7	IO_L57P_7/VREF_7	R34		
7	IO_L57N_7	T34		
7	IO_L56P_7	T29		
7	IO_L56N_7	R29		
7	IO_L55P_7	M39		
7	IO_L55N_7	N39		
7	IO_L54P_7	N36		
7	IO_L54N_7	P36		
7	IO_L53P_7	R30		
7	IO_L53N_7	P30		
7	IO_L52P_7	M38		
7	IO_L52N_7	N38		
7	IO_L51P_7/VREF_7	P33		
7	IO_L51N_7	R33		