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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	8448
Number of Logic Elements/Cells	-
Total RAM Bits	2654208
Number of I/O	684
Number of Gates	6000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	957-BBGA, FCBGA
Supplier Device Package	957-FCBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v6000-5bfg957i

Table 2: **Supported Differential Signal I/O Standards**

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Output V_{OD}
LVPECL_33	3.3	N/R(1)	N/R	0.490 - 1.220
LDT_25	2.5	N/R	N/R	0.500 - 0.700
LVDS_33	3.3	N/R	N/R	0.250 - 0.400
LVDS_25	2.5	N/R	N/R	0.250 - 0.400
LVDSEXT_33	3.3	N/R	N/R	0.440 - 0.820
LVDSEXT_25	2.5	N/R	N/R	0.440 - 0.820
BLVDS_25	2.5	N/R	N/R	0.250 - 0.450
ULVDS_25	2.5	N/R	N/R	0.500 - 0.700

Notes:
1. N/R = no requirement.

Table 3: **Supported DCI I/O Standards**

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Termination Type
LVDCI_33(1)	3.3	3.3	N/R(4)	Series
LVDCI_DV2_33(1)	3.3	3.3	N/R	Series
LVDCI_25(1)	2.5	2.5	N/R	Series
LVDCI_DV2_25(1)	2.5	2.5	N/R	Series
LVDCI_18(1)	1.8	1.8	N/R	Series
LVDCI_DV2_18(1)	1.8	1.8	N/R	Series
LVDCI_15(1)	1.5	1.5	N/R	Series
LVDCI_DV2_15(1)	1.5	1.5	N/R	Series
GTL_DCI	1.2	1.2	0.8	Single
GTLP_DCI	1.5	1.5	1.0	Single
HSTL_I_DCI	1.5	1.5	0.75	Split
HSTL_II_DCI	1.5	1.5	0.75	Split
HSTL_III_DCI	1.5	1.5	0.9	Single
HSTL_IV_DCI	1.5	1.5	0.9	Single
HSTL_I_DCI_18	1.8	1.8	0.9	Split
HSTL_II_DCI_18	1.8	1.8	0.9	Split
HSTL_III_DCI_18	1.8	1.8	1.1	Single
HSTL_IV_DCI_18	1.8	1.8	1.1	Single
SSTL18_I_DCI(3)	1.8	1.8	0.9	Split
SSTL18_II_DCI	1.8	1.8	0.9	Split
SSTL2_I_DCI(2)	2.5	2.5	1.25	Split
SSTL2_II_DCI(2)	2.5	2.5	1.25	Split
SSTL3_I_DCI(2)	3.3	3.3	1.5	Split
SSTL3_II_DCI(2)	3.3	3.3	1.5	Split
LVDS_25_DCI	2.5	2.5	N/R	Split
LVDSEXT_25_DCI	2.5	2.5	N/R	Split

Notes:
1. LVDCI_XX and LVDCI_DV2_XX are LVCMOS controlled impedance buffers, matching the reference resistors or half of the reference resistors.
2. These are SSTL compatible.
3. SSTL18_I is not a JEDEC-supported standard.
4. N/R = no requirement.

Logic Resources

IOB blocks include six storage elements, as shown in Figure 2.

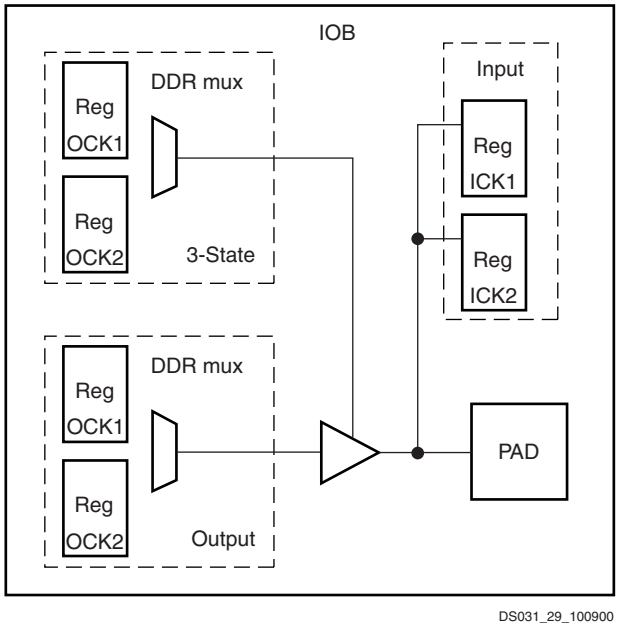

Figure 2: **Virtex-II IOB Block**

Each storage element can be configured either as an edge-triggered D-type flip-flop or as a level-sensitive latch. On the input, output, and 3-state path, one or two DDR registers can be used.

Double data rate is directly accomplished by the two registers on each path, clocked by the rising edges (or falling edges) from two different clock nets. The two clock signals are generated by the DCM and must be 180 degrees out of phase, as shown in Figure 3. There are two input, output, and 3-state data signals, each being alternately clocked out.

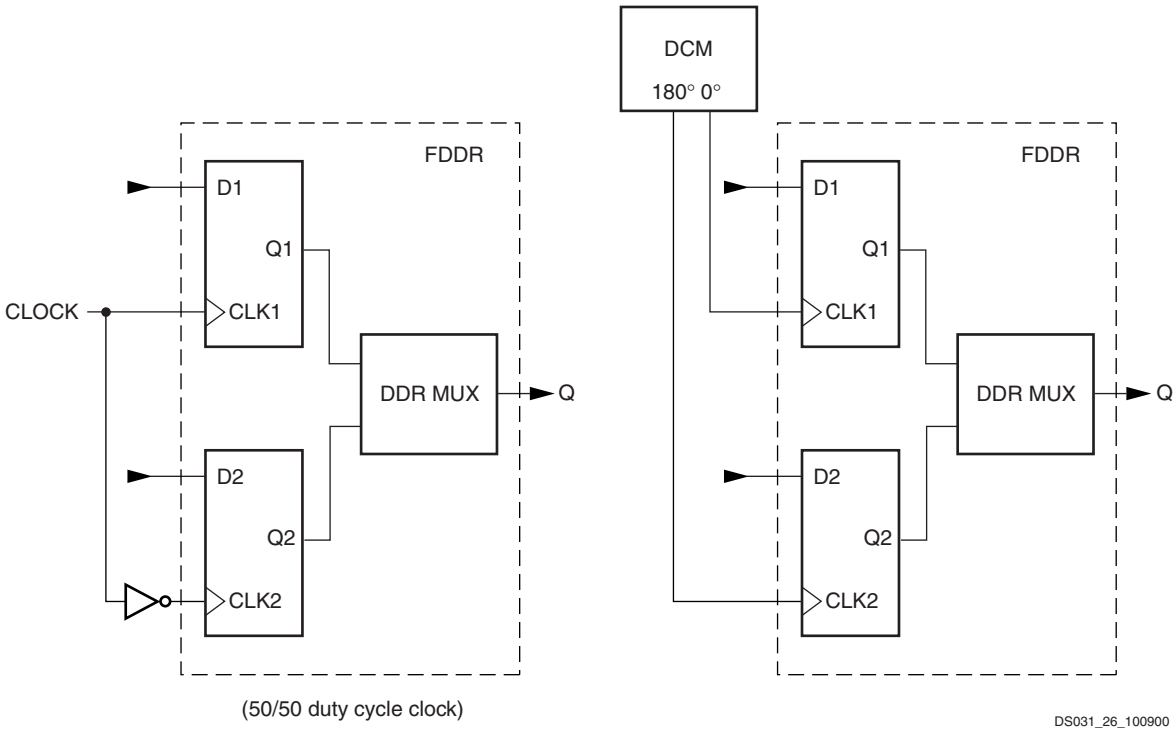

Figure 3: **Double Data Rate Registers**

The DDR mechanism shown in Figure 3 can be used to mirror a copy of the clock on the output. This is useful for propagating a clock along the data that has an identical delay. It is also useful for multiple clock generation, where there is a unique clock driver for every clock load. Virtex-II devices can produce many copies of a clock with very little skew.

Each group of two registers has a clock enable signal (ICE for the input registers, OCE for the output registers, and TCE for the 3-state registers). The clock enable signals are active High by default. If left unconnected, the clock enable for that storage element defaults to the active state.

Each IOB block has common synchronous or asynchronous set and reset (SR and REV signals).

SR forces the storage element into the state specified by the SRHIGH or SRLOW attribute. SRHIGH forces a logic “1”. SRLOW forces a logic “0”. When SR is used, a second input (REV) forces the storage element into the opposite state. The reset condition predominates over the set condition. The initial state after configuration or global initialization state is defined by a separate INIT0 and INIT1 attribute. By default, the SRLOW attribute forces INIT0, and the SRHIGH attribute forces INIT1.

For each storage element, the SRHIGH, SRLOW, INIT0, and INIT1 attributes are independent. Synchronous or asynchronous set / reset is consistent in an IOB block.

All the control signals have independent polarity. Any inverter placed on a control input is automatically absorbed.

Each register or latch (independent of all other registers or latches) (see Figure 4) can be configured as follows:

- No set or reset
- Synchronous set
- Synchronous reset
- Synchronous set and reset
- Asynchronous set (preset)
- Asynchronous reset (clear)
- Asynchronous set and reset (preset and clear)

The synchronous reset overrides a set, and an asynchronous clear overrides a preset.

3-State Buffers

Introduction

Each Virtex-II CLB contains two 3-state drivers (TBUFs) that can drive on-chip busses. Each 3-state buffer has its own 3-state control pin and its own input pin.

Each of the four slices have access to the two 3-state buffers through the switch matrix, as shown in Figure 27. TBUFs in neighboring CLBs can access slice outputs by direct connects. The outputs of the 3-state buffers drive horizontal routing resources used to implement 3-state busses.

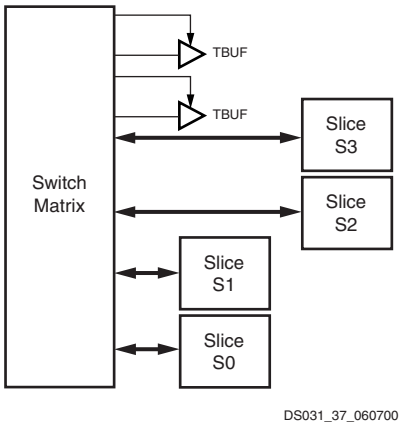

Figure 27: **Virtex-II 3-State Buffers**

The 3-state buffer logic is implemented using AND-OR logic rather than 3-state drivers, so that timing is more predictable and less load dependant especially with larger devices.

Locations / Organization

Four horizontal routing resources per CLB are provided for on-chip 3-state busses. Each 3-state buffer has access alternately to two horizontal lines, which can be partitioned as shown in Figure 28. The switch matrices corresponding to SelectRAM memory and multiplier or I/O blocks are skipped.

Number of 3-State Buffers

Table 11 shows the number of 3-state buffers available in each Virtex-II device. The number of 3-state buffers is twice the number of CLB elements.

Table 11: **Virtex-II 3-State Buffers**

Device	3-State Buffers per Row	Total Number of 3-State Buffers
XC2V40	16	128
XC2V80	16	256
XC2V250	32	768
XC2V500	48	1,536
XC2V1000	64	2,560
XC2V1500	80	3,840
XC2V2000	96	5,376
XC2V3000	112	7,168
XC2V4000	144	11,520
XC2V6000	176	16,896
XC2V8000	208	23,296

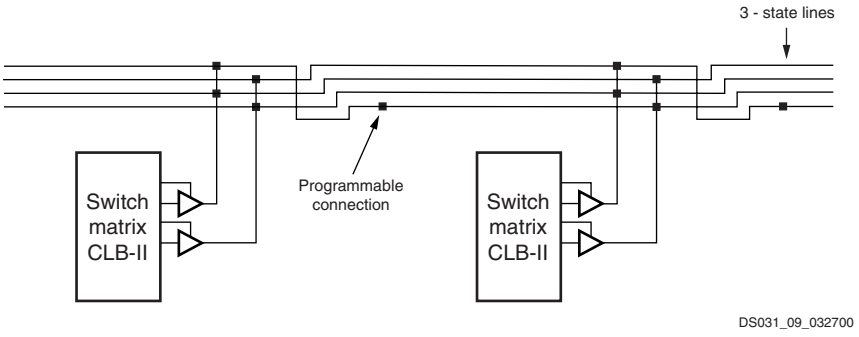

Figure 28: **3-State Buffer Connection to Horizontal Lines**

CLB/Slice Configurations

Table 12 summarizes the logic resources in one CLB. All of the CLBs are identical and each CLB or slice can be implemented in one of the configurations listed. Table 13 shows the available resources in all CLBs.

Table 12: **Logic Resources in One CLB**

Slices	LUTs	Flip-Flops	MULT_ANDs	Arithmetic & Carry-Chains	SOP Chains	Distributed SelectRAM	Shift Registers	TBUF
4	8	8	8	2	2	128 bits	128 bits	2

Table 2: **Recommended Operating Conditions**

Symbol	Description	Temperature Range and Grade		Min	Max	Units
V_{CCINT}	Internal supply voltage relative to GND	T_J = 0 °C to +85°C	Commercial	1.425	1.575	V
		T_J = –40°C to +100°C	Industrial	1.425	1.575	V
V_{CCAUX}	Auxiliary supply voltage relative to GND	T_J = 0 °C to +85°C	Commercial	3.135	3.465	V
		T_J = –40°C to +100°C	Industrial	3.135	3.465	V
V_{CCO}	Supply voltage relative to GND	T_J = 0 °C to +85°C	Commercial	1.2	3.6	V
		T_J = –40°C to +100°C	Industrial	1.2	3.6	V
V_{BATT}(1)	Battery voltage relative to GND	T_J = 0 °C to +85°C	Commercial	1.0	3.6	V
		T_J = –40°C to +100°C	Industrial	1.0	3.6	V

Notes:
1. If battery is not used, connect V_{BATT} to GND or V_{CCAUX}.
2. Recommended maximum voltage droop for V_{CCAUX} is 10 mV/ms.
3. The thresholds for Power On Reset are V_{CCINT} > 1.2V, V_{CCAUX} > 2.5V, and V_{CCO} (Bank 4) > 1.5 V.
4. Limit the noise at the power supply to be within 200 mV peak-to-peak.
5. For power bypassing guidelines, see XAPP623 at www.xilinx.com.

Table 3: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Device	Min	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage	All	1.2		V
V_{DRI}	Data retention V_{CCAUX} voltage	All	2.5		V
I_{REF}	V_{REF} current per pin	All	–10	+10	µA
I_L	Input leakage current	All	–10	+10	µA
C_{IN}	Input capacitance	All		10	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0 V, V_{CCO} = 3.3 V (sample tested)	All	Note (1)	250	µA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 3.6 V (sample tested)	All	Note (1)	250	µA
I_{BATT}	Battery supply current	All	(Note 2)		nA

Notes:
1. Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits.
2. Battery supply current (I_{BATT}):

	Device Unpowered	Device Powered	Units
25°C:	< 50	< 10	nA
85°C:	N/A	< 10	nA

Table 6: **DC Input and Output Levels *(Continued)***

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
SSTL3 I	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	V_{CCO} + 0.5	V_{REF} – 0.6	V_{REF} + 0.6	8	– 8
SSTL3 II	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	V_{CCO} + 0.5	V_{REF} – 0.8	V_{REF} + 0.8	16	– 16
SSTL2 I	– 0.5	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.5	V_{REF} – 0.65	V_{REF} + 0.65	7.6	– 7.6
SSTL2 II	– 0.5	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.5	V_{REF} – 0.80	V_{REF} + 0.80	15.2	– 15.2
AGP	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2

Notes:
1. V_{OL} and V_{OH} for lower drive currents are sample tested. The DONE pin is always LVTTL 12 mA.
2. Tested according to the relevant specifications.
3. LVTTL and LVCMOS inputs have approximately 100 mV of hysteresis.

LDT Differential Signal DC Specifications (LDT_25)

Table 7: **LDT DC Specifications**

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Differential Output Voltage	V_{OD}	R_T = 100 Ω across Q and $\overline{Q}$ signals	500	600	700	mV
Change in V_{OD} Magnitude	ΔV_{OD}		–15		15	mV
Output Common Mode Voltage	V_{OCM}	R_T = 100 Ω across Q and $\overline{Q}$ signals	560	600	640	mV
Change in V_{OS} Magnitude	ΔV_{OCM}		–15		15	mV
Input Differential Voltage	V_{ID}		200	600	1000	mV
Change in V_{ID} Magnitude	ΔV_{ID}		–15		15	mV
Input Common Mode Voltage	V_{ICM}		500	600	700	mV
Change in V_{ICM} Magnitude	ΔV_{ICM}		–15		15	mV

LVDS DC Specifications (LVDS_33 & LVDS_25)

Table 8: **LVDS DC Specifications**

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}			3.3 or 2.5		V
Output High Voltage for Q and $\overline{Q}$	V_{OH}	R_T = 100 Ω across Q and $\overline{Q}$ signals			1.575	V
Output Low Voltage for Q and $\overline{Q}$	V_{OL}	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.925			V
Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{ODIFF}	R_T = 100 Ω across Q and $\overline{Q}$ signals	250	350	400	mV
Output Common-Mode Voltage	V_{OCM}	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.2	1.375	V
Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{IDIFF}	Common-mode input voltage = 1.25 V	100	350	N/A	mV
Input Common-Mode Voltage	V_{ICM}	Differential input voltage = ±350 mV	0.2	1.25	V_{CCO} – 0.5	V

Clock Distribution Switching Characteristics

Table 20: **Clock Distribution Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Global Clock Buffer I input to O output	T_{GIO}	0.47	0.52	0.59	ns, Max
Global Clock Buffer S input Setup/Hold to I1 an I2 inputs	T_{GSI}/T_{GIS}	0.55/ 0	0.61/ 0	0.70/ 0	ns, Max

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used (see Figure 16 in Module 2). The values listed below are worst-case. Precise values are provided by the timing analyzer.

Table 21: **CLB Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Combinatorial Delays					
4-input function: F/G inputs to X/Y outputs	T_{ILO}	0.35	0.39	0.44	ns, Max
5-input function: F/G inputs to F5 output	T_{IF5}	0.57	0.63	0.72	ns, Max
5-input function: F/G inputs to X output	T_{IF5X}	0.76	0.83	0.95	ns, Max
FXINA or FXINB inputs to Y output via MUXFX	T_{IFXY}	0.36	0.39	0.45	ns, Max
FXINA input to FX output via MUXFX	T_{INAFX}	0.26	0.28	0.32	ns, Max
FXINB input to FX output via MUXFX	T_{INBFX}	0.26	0.28	0.32	ns, Max
SOPIN input to SOPOUT output via ORCY	T_{SOPSOP}	0.35	0.38	0.44	ns, Max
Incremental delay routing through transparent latch to XQ/YQ outputs	T_{IFNCTL}	0.41	0.45	0.51	ns, Max
Sequential Delays					
FF Clock CLK to XQ/YQ outputs	T_{CKO}	0.45	0.50	0.57	ns, Max
Latch Clock CLK to XQ/YQ outputs	T_{CKLO}	0.54	0.59	0.68	ns, Max
Setup and Hold Times Before/After Clock CLK					
BX/BY inputs	T_{DICK}/T_{CKDI}	0.30/–0.07	0.33/–0.08	0.37/–0.09	ns, Min
DY inputs	T_{DYCK}/T_{CKDY}	0.30/–0.07	0.33/–0.08	0.37/–0.09	ns, Min
DX inputs	T_{DXCK}/T_{CKDX}	0.30/–0.07	0.33/–0.08	0.37/–0.09	ns, Min
CE input	T_{CECK}/T_{CKCE}	0.19/–0.06	0.21/–0.07	0.24/–0.08	ns, Min
SR/BY inputs (synchronous)	T_{SRCK}/T_{SCKR}	0.21/–0.02	0.23/–0.03	0.26/–0.03	ns, Min
Clock CLK					
Minimum Pulse Width, High	T_{CH}	0.61	0.67	0.77	ns, Min
Minimum Pulse Width, Low	T_{CL}	0.61	0.67	0.77	ns, Min
Set/Reset					
Minimum Pulse Width, SR/BY inputs (asynchronous)	T_{RPW}	0.61	0.67	0.77	ns, Min
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	T_{RQ}	1.06	1.17	1.34	ns, Max
Toggle Frequency (MHz) (for export control)	F_{TOG}	820	750	650	MHz

Virtex-II Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Setup and Hold for LVTTL Standard, *With* DCM

Table 36: **Global Clock Setup and Hold for LVTTL Standard, *With* DCM**

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in IOB Input Switching Characteristics Standard Adjustments, page 11.						
No Delay Global Clock and IFF with DCM	T_{PSDCM}/T_{PHDCM}	XC2V40	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		XC2V80	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		XC2V250	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		XC2V500	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		XC2V1000	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		XC2V1500	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		XC2V2000	1.70/–0.90	1.70/–0.90	1.96/–0.76	ns
		XC2V3000	1.70/–0.90	1.70/–0.90	1.96/–0.76	ns
		XC2V4000	1.70/–0.90	1.70/–0.90	1.96/–0.76	ns
		XC2V6000	1.70/–0.90	1.70/–0.90	1.96/–0.76	ns
		XC2V8000		1.70/–0.90	1.96/–0.76	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.

Date	Version	Revision
03/01/05 (*cont'd*)	3.4 (*cont'd*)	• Table 15, Table 17, Table 18, and Table 19: Restructured these I/O-related tables to include descriptions, as well as the actual IOSTANDARD attributes (used in Xilinx ISE™ software) for all I/O standards. • Table 15: Added data for the following I/O standards: SSTL18_I, SSTL18_II, SSTL18_I_DCI, SSTL18_II_DCI, HSTL_I_18, HSTL_II_18, HSTL_III_18, HSTL_IV_18, LVDSEXT_25, LVDSEXT_33, BLVDS_25, LVDS_25_DCI, LVDS_33_DCI, LVDSEXT_25_DCI, LVDSEXT_33_DCI, HSLVDCI_15, HSLVDCI_18, HSLVDCI_25, HSLVDCI_33. Rearranged I/O standards in a more logical order. • Table 16: Added parameter T_{RPW} (Minimum Pulse Width, SR Input). • Table 17: Added data for the following I/O standards: SSTL18_I, SSTL18_II, SSTL18_I_DCI, SSTL18_II_DCI, HSLVDCI_15, HSLVDCI_18, HSLVDCI_25, HSLVDCI_33. Changed "Csl" to "C_{REF}" to agree with Figure 1 and Table 19. Rearranged I/O standards in a more logical order. • Table 18: Added data for the following I/O standards: SSTL18_I, SSTL18_II, HSTL_I_18, HSTL_II_18, HSTL_III_18, HSTL_IV_18. Added footnote defining equivalents for DCI standards. • Table 19: Added Footnotes (2) and (3) to PCI/PCI-X capacitive load (C_{REF}) values. Added HSLVDCI callouts to LVDCI parameter rows (same values). • Table 28: Added parameter T_{BCCS}, CLKA to CLKB Setup Time. • Table 31: Added Footnote (1) indicating that F_{CC_SERIAL} should not exceed $F_{CC\_STARTUP}$ if no provision is made to adjust the speed of CCLK. • Table 33: T_{TCKTDO} corrected from a "Min" to a "Max" specification.
11/05/07	3.5	• Updated copyright notice and legal disclaimer.

Notice of Disclaimer

Virtex-II Data Sheet

The Virtex-II Data Sheet contains the following modules:

- Virtex-II Platform FPGAs: Introduction and Overview (Module 1)
- Virtex-II Platform FPGAs: Functional Description (Module 2)
- Virtex-II Platform FPGAs: DC and Switching Characteristics (Module 3)
- Virtex-II Platform FPGAs: Pinout Information (Module 4)

Pin Definitions

Table 4 provides a description of each pin type listed in Virtex-II pinout tables.

Table 4: **Virtex-II Pin Definitions**

Pin Name	Direction	Description
User I/O Pins		
IO_LXXY_#	Input/Output/ Bidirectional	All user I/O pins are capable of differential signalling and can implement LVDS, ULVDS, BLVDS, LVPECL, or LDT pairs. Each user I/O is labeled "**IO_LXXY_#**", where: **IO** indicates a user I/O pin. **LXXY** indicates a differential pair, with **XX** a unique pair in the bank and **Y = P/N** for the positive and negative sides of the differential pair. **#** indicates the bank number (0 through 7)
Dual-Function Pins		
IO_LXXY_#/ZZZ		The dual-function pins are labelled "**IO_LXXY_#/ZZZ**", where **ZZZ** can be one of the following pins: Per Bank - **VRP, VRN,** or **VREF** Globally - **GCLKX(S/P), BUSY/DOUT, INIT_B, D0/DIN – D7, RDWR_B,** or **CS_B**
With /ZZZ:		
D0/DIN, D1, D2, D3, D4, D5, D6, D7	Input/Output	• *In* SelectMAP *mode,* D0 through D7 are configuration data pins. These pins become user I/Os after configuration, unless the SelectMAP port is retained. • *In bit-serial modes,* DIN (D0) is the single-data input. This pin becomes a user I/O after configuration.
CS_B	Input	In SelectMAP mode, this is the active-low Chip Select signal. The pin becomes a user I/O after configuration, unless the SelectMAP port is retained.
RDWR_B	Input	In SelectMAP mode, this is the active-low Write Enable signal. The pin becomes a user I/O after configuration, unless the SelectMAP port is retained.
BUSY/DOUT	Output	• *In* SelectMAP *mode,* BUSY controls the rate at which configuration data is loaded. The pin becomes a user I/O after configuration, unless the SelectMAP port is retained. • *In bit-serial modes,* DOUT provides preamble and configuration data to downstream devices in a daisy-chain. The pin becomes a user I/O after configuration.
INIT_B	Bidirectional (open-drain)	When Low, this pin indicates that the configuration memory is being cleared. When held Low, the start of configuration is delayed. During configuration, a Low on this output indicates that a configuration data error has occurred. The pin becomes a user I/O after configuration.
GCLKx (S/P)	Input/Output	These are clock input pins that connect to Global Clock Buffers. These pins become regular user I/Os when not needed for clocks.
VRP	Input	This pin is for the DCI voltage reference resistor of P transistor (per bank).
VRN	Input	This pin is for the DCI voltage reference resistor of N transistor (per bank).
ALT_VRP	Input	This is the alternative pin for the DCI voltage reference resistor of P transistor.
ALT_VRN	Input	This is the alternative pin for the DCI voltage reference resistor of N transistor.
V_{REF}	Input	These are input threshold voltage pins. They become user I/Os when an external threshold voltage is not needed (per bank).
Dedicated Pins(1)		
CCLK	Input/Output	Configuration clock. Output in Master mode or Input in Slave mode.

Table 4: **Virtex-II Pin Definitions *(Continued)***

Pin Name	Direction	Description
PROG_B	Input	Active Low asynchronous reset to configuration logic. This pin has a permanent weak pull-up resistor.
DONE	Input/Output	DONE is a bidirectional signal with an optional internal pull-up resistor. As an output, this pin indicates completion of the configuration process. As an input, a Low level on DONE can be configured to delay the start-up sequence.
M2, M1, M0	Input	Configuration mode selection.
HSWAP_EN	Input	Enable I/O pull-ups during configuration.
TCK	Input	Boundary Scan Clock.
TDI	Input	Boundary Scan Data Input.
TDO	Output	Boundary Scan Data Output.
TMS	Input	Boundary Scan Mode Select.
PWRDWN_B	Input *(unsupported)*	Active Low power-down pin (unsupported). *Driving this pin Low can adversely affect device operation and configuration.* PWRDWN_B is internally pulled High, which is its default state. It does not require an external pull-up.
Other Pins		
DXN, DXP	N/A	Temperature-sensing diode pins (Anode: DXP, Cathode: DXN).
V_{BATT}	Input	Decryptor key memory backup supply. Connect V_{BATT} to V_{CCAUX} or GND if battery is not used.
RSVD	N/A	Reserved pin - do not connect.
V_{CCO}	Input	Power-supply pins for the output drivers (per bank).
V_{CCAUX}	Input	Power-supply pins for auxiliary circuits.
V_{CCINT}	Input	Power-supply pins for the internal core logic.
GND	Input	Ground.

Notes:
1. All dedicated pins (JTAG and configuration) are powered by V_{CCAUX} (independent of the bank V_{CCO} voltage).

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
2	IO_L45N_2	H23		
2	IO_L45P_2/VREF_2	H24		
2	IO_L46N_2	J21		
2	IO_L46P_2	J20		
2	IO_L48N_2	H25		
2	IO_L48P_2	H26		
2	IO_L49N_2	J22		
2	IO_L49P_2	J23		
2	IO_L51N_2	K21		
2	IO_L51P_2/VREF_2	K22		
2	IO_L52N_2	K20		
2	IO_L52P_2	L20		
2	IO_L54N_2	J24		
2	IO_L54P_2	J25		
2	IO_L67N_2	K23		
2	IO_L67P_2	K24		
2	IO_L69N_2	J26		
2	IO_L69P_2/VREF_2	K26		
2	IO_L70N_2	L22		
2	IO_L70P_2	L21		
2	IO_L72N_2	L25		
2	IO_L72P_2	L26		
2	IO_L73N_2	L19	NC	
2	IO_L73P_2	M19	NC	
2	IO_L75N_2	L23	NC	
2	IO_L75P_2/VREF_2	L24	NC	
2	IO_L76N_2	M22	NC	
2	IO_L76P_2	M21	NC	
2	IO_L78N_2	M23	NC	
2	IO_L78P_2	M24	NC	
2	IO_L91N_2	M25		
2	IO_L91P_2	M26		
2	IO_L93N_2	M20		
2	IO_L93P_2/VREF_2	N20		
2	IO_L94N_2	N22		
2	IO_L94P_2	N21		
2	IO_L96N_2	N24		

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
NA	VCCINT	H19		
NA	VCCINT	H8		
NA	GND	AF26		
NA	GND	AF1		
NA	GND	AE25		
NA	GND	AE14		
NA	GND	AE13		
NA	GND	AE2		
NA	GND	AD24		
NA	GND	AD3		
NA	GND	AC23		
NA	GND	AC4		
NA	GND	AB22		
NA	GND	AB5		
NA	GND	AA21		
NA	GND	AA6		
NA	GND	U17		
NA	GND	U16		
NA	GND	U15		
NA	GND	U14		
NA	GND	U13		
NA	GND	U12		
NA	GND	U11		
NA	GND	U10		
NA	GND	T17		
NA	GND	T16		
NA	GND	T15		
NA	GND	T14		
NA	GND	T13		
NA	GND	T12		
NA	GND	T11		
NA	GND	T10		
NA	GND	R17		
NA	GND	R16		
NA	GND	R15		
NA	GND	R14		
NA	GND	R13		

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
1	IO_L94N_1	C15
1	IO_L94P_1/VREF_1	D15
1	IO_L93N_1	E15
1	IO_L93P_1	F15
1	IO_L92N_1	G15
1	IO_L92P_1	H15
1	IO_L91N_1	J15
1	IO_L91P_1/VREF_1	J16
1	IO_L78N_1	A16
1	IO_L78P_1	B16
1	IO_L76N_1	D16
1	IO_L76P_1	E16
1	IO_L75N_1/VREF_1	F16
1	IO_L75P_1	F17
1	IO_L73N_1	H16
1	IO_L73P_1	H17
1	IO_L72N_1	A17
1	IO_L72P_1	B17
1	IO_L70N_1	C17
1	IO_L70P_1	D17
1	IO_L69N_1/VREF_1	G18
1	IO_L69P_1	G17
1	IO_L67N_1	A18
1	IO_L67P_1	B18
1	IO_L54N_1	C18
1	IO_L54P_1	D18
1	IO_L52N_1	E18
1	IO_L52P_1	F18
1	IO_L51N_1/VREF_1	H19
1	IO_L51P_1	H18
1	IO_L49N_1	A19
1	IO_L49P_1	A20
1	IO_L30N_1	B19
1	IO_L30P_1	C19
1	IO_L28N_1	D19
1	IO_L28P_1	E19

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
4	IO_L67N_4	AN12	
4	IO_L67P_4	AN11	
4	IO_L68N_4	AE14	
4	IO_L68P_4	AE15	
4	IO_L69N_4	AJ13	
4	IO_L69P_4/VREF_4	AJ14	
4	IO_L70N_4	AL13	
4	IO_L70P_4	AL12	
4	IO_L71N_4	AF14	
4	IO_L71P_4	AF15	
4	IO_L72N_4	AM13	
4	IO_L72P_4	AM12	
4	IO_L73N_4	AP12	
4	IO_L73P_4	AP11	
4	IO_L74N_4	AG15	
4	IO_L74P_4	AG16	
4	IO_L75N_4	AN14	
4	IO_L75P_4/VREF_4	AN13	
4	IO_L76N_4	AP14	
4	IO_L76P_4	AP13	
4	IO_L77N_4	AD16	
4	IO_L77P_4	AD17	
4	IO_L78N_4	AK14	
4	IO_L78P_4	AK13	
4	IO_L79N_4	AN16	NC
4	IO_L79P_4	AP15	NC
4	IO_L80N_4	AE16	NC
4	IO_L80P_4	AE17	NC
4	IO_L81N_4	AH15	NC
4	IO_L81P_4/VREF_4	AJ15	NC
4	IO_L82N_4	AP17	NC
4	IO_L82P_4	AN17	NC
4	IO_L83N_4	AH17	NC
4	IO_L83P_4	AH16	NC
4	IO_L84N_4	AL15	NC
4	IO_L84P_4	AL14	NC

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
1	IO_L69N_1/VREF_1	E15		
1	IO_L69P_1	E16		
1	IO_L68N_1	K17		
1	IO_L68P_1	K16		
1	IO_L67N_1	C15		
1	IO_L67P_1	B15		
1	IO_L60N_1	F15		
1	IO_L60P_1	F16		
1	IO_L59N_1	H16		
1	IO_L59P_1	H15		
1	IO_L58N_1	C13		
1	IO_L58P_1	C14		
1	IO_L57N_1/VREF_1	D13		
1	IO_L57P_1	D14		
1	IO_L56N_1	M17		
1	IO_L56P_1	M16		
1	IO_L55N_1	A12		
1	IO_L55P_1	A13		
1	IO_L54N_1	B12		
1	IO_L54P_1	B13		
1	IO_L53N_1	G15		
1	IO_L53P_1	G14		
1	IO_L52N_1	C11		
1	IO_L52P_1	C12		
1	IO_L51N_1/VREF_1	F13		
1	IO_L51P_1	F14		
1	IO_L50N_1	L16		
1	IO_L50P_1	L15		
1	IO_L49N_1	A10		
1	IO_L49P_1	A11		
1	IO_L36N_1	E12	NC	
1	IO_L36P_1	E13	NC	
1	IO_L35N_1	K15	NC	
1	IO_L35P_1	J14	NC	
1	IO_L34N_1	B9	NC	
1	IO_L34P_1	B10	NC	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
3	IO_L34N_3	AH6	NC	
3	IO_L34P_3	AJ6	NC	
3	IO_L33N_3/VREF_3	AJ8	NC	
3	IO_L33P_3	AH8	NC	
3	IO_L32N_3	AL1	NC	
3	IO_L32P_3	AM1	NC	
3	IO_L31N_3	AH7	NC	
3	IO_L31P_3	AJ7	NC	
3	IO_L30N_3	AH10		
3	IO_L30P_3	AG10		
3	IO_L29N_3	AK3		
3	IO_L29P_3	AL3		
3	IO_L28N_3	AK4		
3	IO_L28P_3	AL4		
3	IO_L27N_3/VREF_3	AJ9		
3	IO_L27P_3	AH9		
3	IO_L26N_3	AM2		
3	IO_L26P_3	AN2		
3	IO_L25N_3	AK5		
3	IO_L25P_3	AL5		
3	IO_L24N_3	AK9		
3	IO_L24P_3	AK8		
3	IO_L23N_3	AN1		
3	IO_L23P_3	AP1		
3	IO_L22N_3	AK6		
3	IO_L22P_3	AL6		
3	IO_L21N_3/VREF_3	AH12		
3	IO_L21P_3	AG12		
3	IO_L20N_3	AM3		
3	IO_L20P_3	AN3		
3	IO_L19N_3	AM4		
3	IO_L19P_3	AN4		
3	IO_L12N_3	AJ12	NC	
3	IO_L12P_3	AH11	NC	
3	IO_L11N_3	AP2	NC	
3	IO_L11P_3	AR2	NC	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
6	VCCO_6	AG33		
6	VCCO_6	AF38		
6	VCCO_6	AF27		
6	VCCO_6	AE31		
6	VCCO_6	AE27		
6	VCCO_6	AE26		
6	VCCO_6	AD27		
6	VCCO_6	AD26		
6	VCCO_6	AC29		
6	VCCO_6	AC27		
6	VCCO_6	AC26		
6	VCCO_6	AB37		
6	VCCO_6	AB27		
6	VCCO_6	AB26		
6	VCCO_6	AA27		
6	VCCO_6	AA26		
7	VCCO_7	W27		
7	VCCO_7	W26		
7	VCCO_7	V37		
7	VCCO_7	V27		
7	VCCO_7	V26		
7	VCCO_7	U29		
7	VCCO_7	U27		
7	VCCO_7	U26		
7	VCCO_7	T27		
7	VCCO_7	T26		
7	VCCO_7	R31		
7	VCCO_7	R27		
7	VCCO_7	R26		
7	VCCO_7	P38		
7	VCCO_7	P27		
7	VCCO_7	N33		
7	VCCO_7	L35		
NA	CCLK	AT5		
NA	PROG_B	H31		

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
4	IO_L29N_4	AL6	NC
4	IO_L29P_4	AL7	NC
4	IO_L30N_4	AJ9	NC
4	IO_L30P_4	AJ10	NC
4	IO_L49N_4	AE11	
4	IO_L49P_4	AE12	
4	IO_L50N_4	AG10	
4	IO_L50P_4	AG11	
4	IO_L51N_4	AL8	
4	IO_L51P_4/VREF_4	AL9	
4	IO_L52N_4	AF12	
4	IO_L52P_4	AF13	
4	IO_L53N_4	AK9	
4	IO_L53P_4	AK10	
4	IO_L54N_4	AH11	
4	IO_L54P_4	AH12	
4	IO_L67N_4	AC12	
4	IO_L67P_4	AC13	
4	IO_L68N_4	AG12	
4	IO_L68P_4	AG13	
4	IO_L69N_4	AL10	
4	IO_L69P_4/VREF_4	AL11	
4	IO_L70N_4	AD13	
4	IO_L70P_4	AD15	
4	IO_L71N_4	AJ11	
4	IO_L71P_4	AJ12	
4	IO_L72N_4	AK11	
4	IO_L72P_4	AK12	
4	IO_L73N_4	AE14	
4	IO_L73P_4	AE15	
4	IO_L74N_4	AF14	
4	IO_L74P_4	AF15	
4	IO_L75N_4	AL12	
4	IO_L75P_4/VREF_4	AL13	
4	IO_L76N_4	AB14	
4	IO_L76P_4	AC14	
4	IO_L77N_4	AH13	
4	IO_L77P_4	AH14	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
6	IO_L20P_6	AD25	
6	IO_L20N_6	AC24	
6	IO_L21P_6	AG30	
6	IO_L21N_6/VREF_6	AF30	
6	IO_L22P_6	AD26	
6	IO_L22N_6	AC26	
6	IO_L23P_6	AF29	
6	IO_L23N_6	AD29	
6	IO_L24P_6	AE28	
6	IO_L24N_6	AD28	
6	IO_L25P_6	AB24	NC
6	IO_L25N_6	AA24	NC
6	IO_L27P_6	AC25	NC
6	IO_L27N_6/VREF_6	AB25	NC
6	IO_L43P_6	AF31	
6	IO_L43N_6	AE31	
6	IO_L44P_6	AA23	
6	IO_L44N_6	Y23	
6	IO_L45P_6	AE30	
6	IO_L45N_6/VREF_6	AC30	
6	IO_L46P_6	AC28	
6	IO_L46N_6	AA28	
6	IO_L47P_6	AD27	
6	IO_L47N_6	AC27	
6	IO_L48P_6	AA25	
6	IO_L48N_6	Y25	
6	IO_L49P_6	AC29	
6	IO_L49N_6	AB29	
6	IO_L50P_6	AB27	
6	IO_L50N_6	AA27	
6	IO_L51P_6	AA26	
6	IO_L51N_6/VREF_6	Y26	
6	IO_L52P_6	AD31	
6	IO_L52N_6	AC31	
6	IO_L53P_6	W22	
6	IO_L53N_6	V22	
6	IO_L54P_6	Y27	
6	IO_L54N_6	W27	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
NA	GND	D10	
NA	GND	D16	
NA	GND	D22	
NA	GND	D28	
NA	GND	E5	
NA	GND	E27	
NA	GND	F6	
NA	GND	F26	
NA	GND	G7	
NA	GND	G13	
NA	GND	G16	
NA	GND	G19	
NA	GND	G25	
NA	GND	H2	
NA	GND	H8	
NA	GND	H24	
NA	GND	H30	
NA	GND	J9	
NA	GND	J23	
NA	GND	K4	
NA	GND	K16	
NA	GND	K28	
NA	GND	N7	
NA	GND	N25	
NA	GND	P14	
NA	GND	P15	
NA	GND	P16	
NA	GND	P17	
NA	GND	P18	
NA	GND	R14	
NA	GND	R15	
NA	GND	R16	
NA	GND	R17	
NA	GND	R18	
NA	GND	T1	
NA	GND	T4	
NA	GND	T7	
NA	GND	T10	