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Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	8448
Number of Logic Elements/Cells	-
Total RAM Bits	2654208
Number of I/O	824
Number of Gates	6000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v6000-5ffg1152c

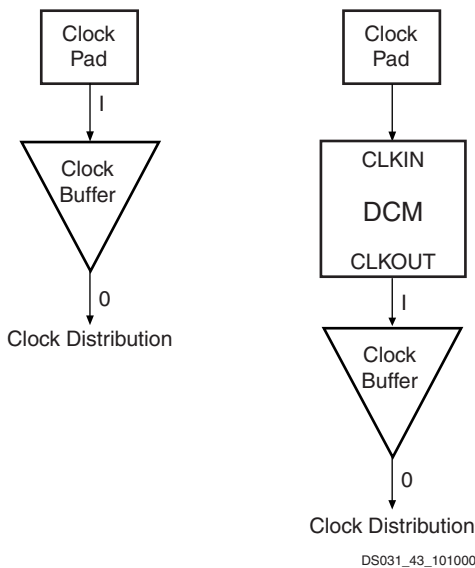


Figure 39: Virtex-II Clock Distribution Configurations

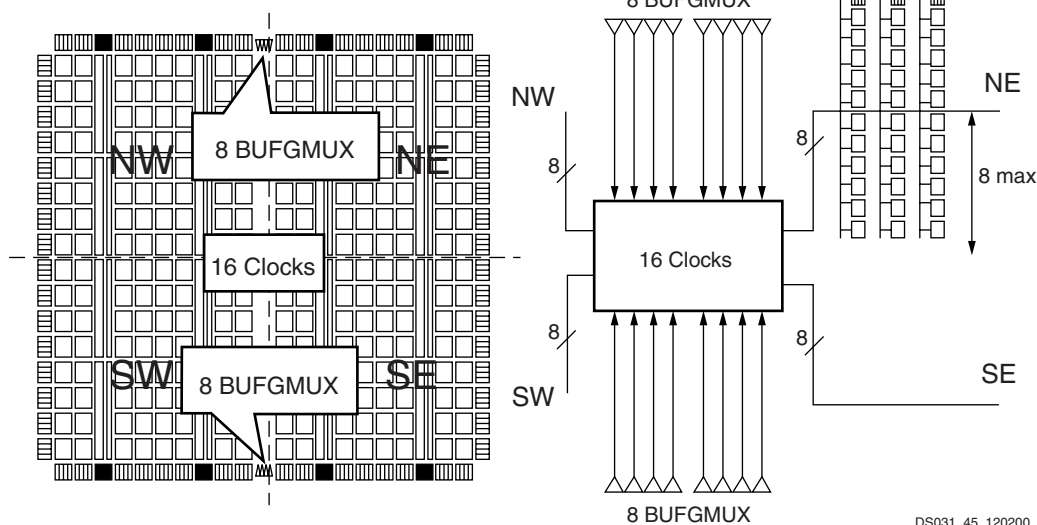


Figure 40: Virtex-II Clock Distribution

The most common configuration option of this element is as a buffer. A BUFG function in this (global buffer) mode, is shown in Figure 41.

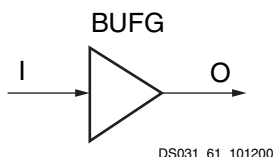


Figure 41: Virtex-II BUFG Function

The Virtex-II global clock buffer BUFG can also be configured as a clock enable/disable circuit (Figure 42), as well as a two-input clock multiplexer (Figure 43). A functional description of these two options is provided below. Each of

Global clock buffers are used to distribute the clock to some or all synchronous logic elements (such as registers in CLBs and IOBs, and SelectRAM blocks).

Eight global clocks can be used in each quadrant of the Virtex-II device. Designers should consider the clock distribution detail of the device prior to pin-locking and floorplanning (see the Virtex-II User Guide).

Figure 40 shows clock distribution in Virtex-II devices.

In each quadrant, up to eight clocks are organized in clock rows. A clock row supports up to 16 CLB rows (eight up and eight down). For the largest devices a new clock row is added, as necessary.

To reduce power consumption, any unused clock branches remain static.

Global clocks are driven by dedicated clock buffers (BUFG), which can also be used to gate the clock (BUFGCE) or to multiplex between two independent clock inputs (BUFGMUX).

them can be used in either of two modes, selected by configuration: rising clock edge or falling clock edge.

This section describes the rising clock edge option. For the opposite option, falling clock edge, just change all "rising" references to "falling" and all "High" references to "Low", except for the description of the CE or S levels. The rising clock edge option uses the BUFGCE and BUFGMUX primitives. The falling clock edge option uses the BUFGCE_1 and BUFGMUX_1 primitives.

BUFGCE

If the CE input is active (High) prior to the incoming rising clock edge, this Low-to-High-to-Low clock pulse passes through the clock buffer. Any level change of CE during the incoming clock High time has no effect.

This document provides Virtex-II™ Device/Package Combinations, Maximum I/Os Available, and Virtex-II Pin Definitions, followed by pinout tables for the following packages:

- CS144/CSG144 Chip-Scale BGA Package
- FG256/FGG256 Fine-Pitch BGA Package
- FG456/FGG456 Fine-Pitch BGA Package
- FG676/FGG676 Fine-Pitch BGA Package
- BG575/BGG575 Standard BGA Package

- BG728/BGG728 Standard BGA Package
- FF896 Flip-Chip Fine-Pitch BGA Package
- FF1152 Flip-Chip Fine-Pitch BGA Package
- FF1517 Flip-Chip Fine-Pitch BGA Package
- BF957 Flip-Chip BGA Package

For device pinout diagrams and layout guidelines, refer to the [Virtex-II Platform FPGA User Guide](#). ASCII package pinout files are also available for download from the Xilinx website (www.xilinx.com).

Virtex-II Device/Package Combinations and Maximum I/Os Available

Wire-bond and flip-chip packages are available. [Table 1](#) and [Table 2](#) show the maximum number of user I/Os possible in wire-bond and flip-chip packages, respectively.

[Table 3](#) shows the number of user I/Os available for all device/package combinations.

- CS denotes wire-bond chip-scale ball grid array (BGA) (0.80 mm pitch).
- CSG denotes Pb-free wire-bond chip-scale ball grid array (BGA) (0.80 mm pitch).
- FG denotes wire-bond fine-pitch BGA (1.00 mm pitch).

- FGG denotes Pb-free wire-bond fine-pitch BGA (1.00 mm pitch).
- BG denotes standard BGA (1.27 mm pitch).
- BGG denotes Pb-free standard BGA (1.27 mm pitch).
- FF denotes flip-chip fine-pitch BGA (1.00 mm pitch).
- BF denotes flip-chip BGA (1.27 mm pitch).

The number of I/Os per package include all user I/Os except the 15 control pins (CCLK, DONE, M0, M1, M2, PROG_B, PWRDWN_B, TCK, TDI, TDO, TMS, HSWAP_EN, DXN, DXP, AND RSVD).

Table 1: Wire-Bond Packages Information

Package ⁽¹⁾	CS144/ CSG144	FG256/ FGG256	FG456/ FGG456	FG676/ FGG676	BG575/ BGG575	BG728/ BGG728
Pitch (mm)	0.80	1.00	1.00	1.00	1.27	1.27
Size (mm)	12 x 12	17 x 17	23 x 23	27 x 27	31 x 31	35 x 35
I/Os	92	172	324	484	408	516

Notes:

1. Wire-bond packages include FGGnnn Pb-free versions. See [Virtex-II Ordering Examples \(Module 1\)](#).

Table 2: Flip-Chip Packages Information

Package	FF896	FF1152	FF1517	BF957
Pitch (mm)	1.00	1.00	1.00	1.27
Size (mm)	31 x 31	35 x 35	40 x 40	40 x 40
I/Os	624	824	1,108	684

Table 6: FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
NA	GND	T16		
NA	GND	T1		
NA	GND	R15		
NA	GND	R2		
NA	GND	P14		
NA	GND	P3		
NA	GND	L11		
NA	GND	L6		
NA	GND	K10		
NA	GND	K9		
NA	GND	K8		
NA	GND	K7		
NA	GND	J10		
NA	GND	J9		
NA	GND	J8		
NA	GND	J7		
NA	GND	H10		
NA	GND	H9		
NA	GND	H8		
NA	GND	H7		
NA	GND	G10		
NA	GND	G9		
NA	GND	G8		
NA	GND	G7		
NA	GND	F11		
NA	GND	F6		
NA	GND	C14		
NA	GND	C3		
NA	GND	B15		
NA	GND	B2		
NA	GND	A16		
NA	GND	A1		

Notes:

1. See Table 4 for an explanation of the signals available on this pin.

FG456/FGG456 Fine-Pitch BGA Package

As shown in Table 7, XC2V250, XC2V500, and XC2V1000 Virtex-II devices are available in the FG456/FGG456 fine-pitch BGA package. Pins in the XC2V250, XC2V500, and XC2V1000 devices are the same, except for the pin differences in the XC2V250 and XC2V500 devices shown in the No Connect columns. Following this table are the **FG456/FGG456 Fine-Pitch BGA Package Specifications (1.00mm pitch)**.

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
0	IO_L01N_0	B4		
0	IO_L01P_0	A4		
0	IO_L02N_0	C4		
0	IO_L02P_0	C5		
0	IO_L03N_0/VRP_0	B5		
0	IO_L03P_0/VRN_0	A5		
0	IO_L04N_0/VREF_0	D6		
0	IO_L04P_0	C6		
0	IO_L05N_0	B6		
0	IO_L05P_0	A6		
0	IO_L06N_0	E7		
0	IO_L06P_0	E8		
0	IO_L21N_0	D7	NC	NC
0	IO_L21P_0/VREF_0	C7	NC	NC
0	IO_L22N_0	B7	NC	NC
0	IO_L22P_0	A7	NC	NC
0	IO_L24N_0	D8	NC	NC
0	IO_L24P_0	C8	NC	NC
0	IO_L49N_0	B8	NC	
0	IO_L49P_0	A8	NC	
0	IO_L51N_0	E9	NC	
0	IO_L51P_0/VREF_0	F9	NC	
0	IO_L52N_0	D9	NC	
0	IO_L52P_0	C9	NC	
0	IO_L54N_0	B9	NC	
0	IO_L54P_0	A9	NC	
0	IO_L91N_0/VREF_0	E10		
0	IO_L91P_0	F10		
0	IO_L92N_0	D10		
0	IO_L92P_0	C10		

Table 9: BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
2	IO_L69P_2/VREF_2	L18	NC	
2	IO_L70N_2	K23	NC	
2	IO_L70P_2	L24	NC	
2	IO_L72N_2	K22	NC	
2	IO_L72P_2	L22	NC	
2	IO_L73N_2	L21	NC	NC
2	IO_L73P_2	L20	NC	NC
2	IO_L91N_2	M23		
2	IO_L91P_2	N24		
2	IO_L93N_2	M21		
2	IO_L93P_2/VREF_2	M22		
2	IO_L94N_2	M19		
2	IO_L94P_2	M20		
2	IO_L96N_2	M17		
2	IO_L96P_2	M18		
3	IO_L96N_3	N23		
3	IO_L96P_3	N22		
3	IO_L94N_3	N20		
3	IO_L94P_3	N21		
3	IO_L93N_3/VREF_3	N19		
3	IO_L93P_3	N18		
3	IO_L91N_3	N17		
3	IO_L91P_3	P17		
3	IO_L73N_3	P24	NC	NC
3	IO_L73P_3	R24	NC	NC
3	IO_L72N_3	R23	NC	
3	IO_L72P_3	R22	NC	
3	IO_L70N_3	P22	NC	
3	IO_L70P_3	P21	NC	
3	IO_L69N_3/VREF_3	P20	NC	
3	IO_L69P_3	P18	NC	
3	IO_L67N_3	T24	NC	
3	IO_L67P_3	U24	NC	
3	IO_L54N_3	T23		
3	IO_L54P_3	T22		

Table 10: BG728 BGA — XC2V3000

Bank	Pin Description	Pin Number
0	IO_L52P_0	E10
0	IO_L54N_0	D10
0	IO_L54P_0	C10
0	IO_L67N_0	B10
0	IO_L67P_0	A10
0	IO_L69N_0	G11
0	IO_L69P_0/VREF_0	H11
0	IO_L70N_0	F11
0	IO_L70P_0	F12
0	IO_L72N_0	D11
0	IO_L72P_0	C11
0	IO_L73N_0	B11
0	IO_L73P_0	A11
0	IO_L75N_0	H12
0	IO_L75P_0/VREF_0	J12
0	IO_L76N_0	E12
0	IO_L76P_0	D12
0	IO_L78N_0	B12
0	IO_L78P_0	A12
0	IO_L91N_0/VREF_0	J13
0	IO_L91P_0	H13
0	IO_L92N_0	G13
0	IO_L92P_0	F13
0	IO_L93N_0	E13
0	IO_L93P_0	D13
0	IO_L94N_0/VREF_0	B13
0	IO_L94P_0	A13
0	IO_L95N_0/GCLK7P	C13
0	IO_L95P_0/GCLK6S	C14
0	IO_L96N_0/GCLK5P	F14
0	IO_L96P_0/GCLK4S	E14
1	IO_L96N_1/GCLK3P	G14
1	IO_L96P_1/GCLK2S	H14
1	IO_L95N_1/GCLK1P	A15
1	IO_L95P_1/GCLK0S	B15

Table 11: FF896 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
1	IO_L68P_1	G12	NC	
1	IO_L67N_1	A9	NC	
1	IO_L67P_1	A10	NC	
1	IO_L54N_1	E10		
1	IO_L54P_1	E11		
1	IO_L53N_1	H12		
1	IO_L53P_1	H11		
1	IO_L52N_1	D9		
1	IO_L52P_1	D10		
1	IO_L51N_1/VREF_1	C9		
1	IO_L51P_1	C8		
1	IO_L50N_1	F11		
1	IO_L50P_1	F10		
1	IO_L49N_1	B8		
1	IO_L49P_1	B9		
1	IO_L24N_1	E8		
1	IO_L24P_1	E9		
1	IO_L23N_1	G11		
1	IO_L23P_1	H10		
1	IO_L22N_1	B7		
1	IO_L22P_1	A7		
1	IO_L21N_1/VREF_1	D8		
1	IO_L21P_1	E7		
1	IO_L20N_1	G10		
1	IO_L20P_1	G9		
1	IO_L19N_1	A5		
1	IO_L19P_1	A6		
1	IO_L06N_1	C6		
1	IO_L06P_1	C7		
1	IO_L05N_1	F9		
1	IO_L05P_1	G8		
1	IO_L04N_1	B6		
1	IO_L04P_1/VREF_1	C5		
1	IO_L03N_1/VRP_1	D7		
1	IO_L03P_1/VRN_1	D6		
1	IO_L02N_1	F8		
1	IO_L02P_1	F7		

Table 11: FF896 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
3	IO_L24N_3	AC8		
3	IO_L24P_3	AB8		
3	IO_L23N_3	AE2		
3	IO_L23P_3	AF3		
3	IO_L22N_3	AD3		
3	IO_L22P_3	AE3		
3	IO_L21N_3/VREF_3	AD6		
3	IO_L21P_3	AD7		
3	IO_L20N_3	AF1		
3	IO_L20P_3	AG1		
3	IO_L19N_3	AD4		
3	IO_L19P_3	AE4		
3	IO_L06N_3	AD8		
3	IO_L06P_3	AE7		
3	IO_L05N_3	AG2		
3	IO_L05P_3	AH2		
3	IO_L04N_3	AD5		
3	IO_L04P_3	AE5		
3	IO_L03N_3/VREF_3	AC9		
3	IO_L03P_3	AD9		
3	IO_L02N_3/VRP_3	AH1		
3	IO_L02P_3/VRN_3	AJ1		
3	IO_L01N_3	AF4		
3	IO_L01P_3	AG3		
4	IO_L01N_4/BUSY/DOUT ⁽¹⁾	AK2		
4	IO_L01P_4/INIT_B	AJ3		
4	IO_L02N_4/D0/DIN ⁽¹⁾	AE8		
4	IO_L02P_4/D1	AF9		
4	IO_L03N_4/D2/ALT_VRP_4	AH5		
4	IO_L03P_4/D3/ALT_VRN_4	AH6		
4	IO_L04N_4/VREF_4	AJ4		
4	IO_L04P_4	AK4		
4	IO_L05N_4/VRP_4	AC10		
4	IO_L05P_4/VRN_4	AC11		
4	IO_L06N_4	AH7		
4	IO_L06P_4	AG6		

Table 11: FF896 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
6	VCCO_6	AF29		
6	VCCO_6	AA22		
6	VCCO_6	Y22		
6	VCCO_6	Y21		
6	VCCO_6	W22		
6	VCCO_6	W21		
6	VCCO_6	V28		
6	VCCO_6	V22		
6	VCCO_6	V21		
6	VCCO_6	U21		
6	VCCO_6	T21		
7	VCCO_7	R21		
7	VCCO_7	P21		
7	VCCO_7	N28		
7	VCCO_7	N22		
7	VCCO_7	N21		
7	VCCO_7	M22		
7	VCCO_7	M21		
7	VCCO_7	L22		
7	VCCO_7	L21		
7	VCCO_7	K22		
7	VCCO_7	E29		
NA	CCLK	AF6		
NA	PROG_B	B28		
NA	DONE	AG5		
NA	M0	AF25		
NA	M1	AG26		
NA	M2	AH27		
NA	HSWAP_EN	C27		
NA	TCK	D5		
NA	TDI	A29		
NA	TDO	B3		
NA	TMS	C4		
NA	PWRDWN_B	AH4		
NA	DXN	D26		
NA	DXP	E25		

Table 11: FF896 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
NA	GND	AC1		
NA	GND	AA28		
NA	GND	AA3		
NA	GND	W26		
NA	GND	W19		
NA	GND	W18		
NA	GND	W17		
NA	GND	W16		
NA	GND	W15		
NA	GND	W14		
NA	GND	W13		
NA	GND	W12		
NA	GND	W5		
NA	GND	V19		
NA	GND	V18		
NA	GND	V17		
NA	GND	V16		
NA	GND	V15		
NA	GND	V14		
NA	GND	V13		
NA	GND	V12		
NA	GND	U24		
NA	GND	U19		
NA	GND	U18		
NA	GND	U17		
NA	GND	U16		
NA	GND	U15		
NA	GND	U14		
NA	GND	U13		
NA	GND	U12		
NA	GND	U7		
NA	GND	T19		
NA	GND	T18		
NA	GND	T17		
NA	GND	T16		
NA	GND	T15		
NA	GND	T14		

Table 12: FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
1	IO_L69P_1	F13	
1	IO_L68N_1	C11	
1	IO_L68P_1	C12	
1	IO_L67N_1	B11	
1	IO_L67P_1	B12	
1	IO_L60N_1	F11	NC
1	IO_L60P_1	F12	NC
1	IO_L54N_1	D10	
1	IO_L54P_1	D11	
1	IO_L53N_1	G12	
1	IO_L53P_1	G13	
1	IO_L52N_1	B9	
1	IO_L52P_1	B10	
1	IO_L51N_1/VREF_1	B8	
1	IO_L51P_1	A9	
1	IO_L50N_1	K14	
1	IO_L50P_1	K13	
1	IO_L49N_1	A6	
1	IO_L49P_1	A7	
1	IO_L30N_1	D9	
1	IO_L30P_1	C9	
1	IO_L29N_1	H13	
1	IO_L29P_1	H12	
1	IO_L28N_1	C7	
1	IO_L28P_1	C8	
1	IO_L27N_1/VREF_1	E11	
1	IO_L27P_1	E10	
1	IO_L26N_1	J13	
1	IO_L26P_1	K12	
1	IO_L25N_1	B6	
1	IO_L25P_1	B7	
1	IO_L24N_1	E8	
1	IO_L24P_1	E9	
1	IO_L23N_1	G10	
1	IO_L23P_1	G11	
1	IO_L22N_1	A4	

Table 12: FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
3	IO_L83P_3	Y4	NC
3	IO_L82N_3	W11	NC
3	IO_L82P_3	V11	NC
3	IO_L81N_3/VREF_3	W8	NC
3	IO_L81P_3	Y8	NC
3	IO_L80N_3	W2	NC
3	IO_L80P_3	Y1	NC
3	IO_L79N_3	AA3	NC
3	IO_L79P_3	AB3	NC
3	IO_L78N_3	Y6	
3	IO_L78P_3	AA6	
3	IO_L77N_3	AA4	
3	IO_L77P_3	AB4	
3	IO_L76N_3	Y7	
3	IO_L76P_3	AA8	
3	IO_L75N_3/VREF_3	Y10	
3	IO_L75P_3	AA10	
3	IO_L74N_3	AA1	
3	IO_L74P_3	AB1	
3	IO_L73N_3	AA5	
3	IO_L73P_3	AB5	
3	IO_L72N_3	AA9	
3	IO_L72P_3	Y9	
3	IO_L71N_3	AA2	
3	IO_L71P_3	AB2	
3	IO_L70N_3	AB6	
3	IO_L70P_3	AC6	
3	IO_L69N_3/VREF_3	AD1	
3	IO_L69P_3	AC1	
3	IO_L68N_3	AC3	
3	IO_L68P_3	AD3	
3	IO_L67N_3	AC4	
3	IO_L67P_3	AD4	
3	IO_L54N_3	AB7	
3	IO_L54P_3	AC7	
3	IO_L53N_3	AC2	

Table 12: FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
3	IO_L23P_3	AJ3	
3	IO_L22N_3	AF7	
3	IO_L22P_3	AG7	
3	IO_L21N_3/VREF_3	AL1	
3	IO_L21P_3	AK1	
3	IO_L20N_3	AH2	
3	IO_L20P_3	AJ2	
3	IO_L19N_3	AJ4	
3	IO_L19P_3	AK4	
3	IO_L06N_3	AE10	
3	IO_L06P_3	AD10	
3	IO_L05N_3	AK2	
3	IO_L05P_3	AL2	
3	IO_L04N_3	AH6	
3	IO_L04P_3	AJ5	
3	IO_L03N_3/VREF_3	AE11	
3	IO_L03P_3	AF11	
3	IO_L02N_3/VRP_3	AK3	
3	IO_L02P_3/VRN_3	AL3	
3	IO_L01N_3	AF10	
3	IO_L01P_3	AG9	
4	IO_L01N_4/BUSY/DOUT ⁽¹⁾	AM4	
4	IO_L01P_4/INIT_B	AL5	
4	IO_L02N_4/D0/DIN ⁽¹⁾	AG10	
4	IO_L02P_4/D1	AH11	
4	IO_L03N_4/D2/ALT_VRP_4	AK7	
4	IO_L03P_4/D3/ALT_VRN_4	AK8	
4	IO_L04N_4/VREF_4	AL6	
4	IO_L04P_4	AM6	
4	IO_L05N_4/VRP_4	AK9	
4	IO_L05P_4/VRN_4	AJ8	
4	IO_L06N_4	AM8	
4	IO_L06P_4	AM7	
4	IO_L19N_4	AN3	
4	IO_L19P_4	AM2	

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
1	IO_L33N_1/VREF_1	D11	NC	
1	IO_L33P_1	D12	NC	
1	IO_L32N_1	H14	NC	
1	IO_L32P_1	H13	NC	
1	IO_L31N_1	A8	NC	
1	IO_L31P_1	A9	NC	
1	IO_L30N_1	F11		
1	IO_L30P_1	F12		
1	IO_L29N_1	K14		
1	IO_L29P_1	L14		
1	IO_L28N_1	C9		
1	IO_L28P_1	C10		
1	IO_L27N_1/VREF_1	G11		
1	IO_L27P_1	G12		
1	IO_L26N_1	M15		
1	IO_L26P_1	M14		
1	IO_L25N_1	B7		
1	IO_L25P_1	B8		
1	IO_L24N_1	D9		
1	IO_L24P_1	D10		
1	IO_L23N_1	J13		
1	IO_L23P_1	J12		
1	IO_L22N_1	A6		
1	IO_L22P_1	A7		
1	IO_L21N_1/VREF_1	E9		
1	IO_L21P_1	E10		
1	IO_L20N_1	D8		
1	IO_L20P_1	E7		
1	IO_L19N_1	C7		
1	IO_L19P_1	C8		
1	IO_L12N_1	F9	NC	
1	IO_L12P_1	F10	NC	
1	IO_L11N_1	H12	NC	
1	IO_L11P_1	H11	NC	
1	IO_L10N_1	B5	NC	
1	IO_L10P_1	B6	NC	

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
5	IO_L55N_5	AV28		
5	IO_L55P_5	AV27		
5	IO_L54N_5	AP27		
5	IO_L54P_5	AP26		
5	IO_L53N_5	AN25		
5	IO_L53P_5	AN26		
5	IO_L52N_5	AU29		
5	IO_L52P_5	AU28		
5	IO_L51N_5/VREF_5	AR28		
5	IO_L51P_5	AR27		
5	IO_L50N_5	AJ24		
5	IO_L50P_5	AJ25		
5	IO_L49N_5	AW30		
5	IO_L49P_5	AW29		
5	IO_L36N_5	AT29	NC	
5	IO_L36P_5	AT28	NC	
5	IO_L35N_5	AK25	NC	
5	IO_L35P_5	AL26	NC	
5	IO_L34N_5	AV31	NC	
5	IO_L34P_5	AV30	NC	
5	IO_L33N_5/VREF_5	AP29	NC	
5	IO_L33P_5	AP28	NC	
5	IO_L32N_5	AK26	NC	
5	IO_L32P_5	AJ26	NC	
5	IO_L31N_5	AW32	NC	
5	IO_L31P_5	AW31	NC	
5	IO_L30N_5	AM27		
5	IO_L30P_5	AM26		
5	IO_L29N_5	AN28		
5	IO_L29P_5	AN29		
5	IO_L28N_5	AU31		
5	IO_L28P_5	AU30		
5	IO_L27N_5/VREF_5	AT31		
5	IO_L27P_5	AT30		
5	IO_L26N_5	AH25		
5	IO_L26P_5	AH26		

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
6	IO_L71N_6	AE39		
6	IO_L72P_6	AD36		
6	IO_L72N_6	AE36		
6	IO_L73P_6	AB29		
6	IO_L73N_6	AA29		
6	IO_L74P_6	AE38		
6	IO_L74N_6	AD38		
6	IO_L75P_6	AC33		
6	IO_L75N_6/VREF_6	AD33		
6	IO_L76P_6	AB30		
6	IO_L76N_6	AA30		
6	IO_L77P_6	AD37		
6	IO_L77N_6	AC37		
6	IO_L78P_6	AB34		
6	IO_L78N_6	AC34		
6	IO_L79P_6	AB31		
6	IO_L79N_6	AA31		
6	IO_L80P_6	AD39		
6	IO_L80N_6	AC39		
6	IO_L81P_6	AB35		
6	IO_L81N_6/VREF_6	AC35		
6	IO_L82P_6	AB32		
6	IO_L82N_6	AA32		
6	IO_L83P_6	AC38		
6	IO_L83N_6	AB38		
6	IO_L84P_6	AA33		
6	IO_L84N_6	AB33		
6	IO_L91P_6	Y28		
6	IO_L91N_6	Y29		
6	IO_L92P_6	AB39		
6	IO_L92N_6	AA39		
6	IO_L93P_6	AA36		
6	IO_L93N_6/VREF_6	AB36		
6	IO_L94P_6	Y31		
6	IO_L94N_6	Y32		
6	IO_L95P_6	AA37		

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	GND	U4		
NA	GND	T23		
NA	GND	T22		
NA	GND	T21		
NA	GND	T20		
NA	GND	T19		
NA	GND	T18		
NA	GND	T17		
NA	GND	P35		
NA	GND	P5		
NA	GND	L38		
NA	GND	L29		
NA	GND	L11		
NA	GND	L2		
NA	GND	K30		
NA	GND	K20		
NA	GND	K10		
NA	GND	J31		
NA	GND	J9		
NA	GND	H32		
NA	GND	H23		
NA	GND	H17		
NA	GND	H8		
NA	GND	G33		
NA	GND	G20		
NA	GND	G7		
NA	GND	F34		
NA	GND	F6		
NA	GND	E35		
NA	GND	E26		
NA	GND	E14		
NA	GND	E5		
NA	GND	D36		
NA	GND	D23		
NA	GND	D20		
NA	GND	D17		

Table 14: BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000

Bank	Pin Description	Pin Number	No Connect in XC2V2000
0	IO_L92N_0	F17	
0	IO_L92P_0	F16	
0	IO_L93N_0	B18	
0	IO_L93P_0	B17	
0	IO_L94N_0/VREF_0	J17	
0	IO_L94P_0	J16	
0	IO_L95N_0/GCLK7P	E17	
0	IO_L95P_0/GCLK6S	E16	
0	IO_L96N_0/GCLK5P	A18	
0	IO_L96P_0/GCLK4S	A17	
1	IO_L96N_1/GCLK3P	C16	
1	IO_L96P_1/GCLK2S	C15	
1	IO_L95N_1/GCLK1P	H16	
1	IO_L95P_1/GCLK0S	H15	
1	IO_L94N_1	A15	
1	IO_L94P_1/VREF_1	A14	
1	IO_L93N_1	F15	
1	IO_L93P_1	F14	
1	IO_L92N_1	G15	
1	IO_L92P_1	G14	
1	IO_L91N_1	B15	
1	IO_L91P_1/VREF_1	B14	
1	IO_L78N_1	D15	
1	IO_L78P_1	E15	
1	IO_L77N_1	J15	
1	IO_L77P_1	K14	
1	IO_L76N_1	D14	
1	IO_L76P_1	D13	
1	IO_L75N_1/VREF_1	E14	
1	IO_L75P_1	E13	
1	IO_L74N_1	A13	
1	IO_L74P_1	A12	
1	IO_L73N_1	F13	
1	IO_L73P_1	F12	
1	IO_L72N_1	J14	
1	IO_L72P_1	J13	
1	IO_L71N_1	B13	

Table 14: BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000

Bank	Pin Description	Pin Number	No Connect in XC2V2000
2	VCCO_2	N12	
2	VCCO_2	P3	
2	VCCO_2	P8	
2	VCCO_2	P11	
2	VCCO_2	P12	
2	VCCO_2	R11	
2	VCCO_2	R12	
3	VCCO_3	U11	
3	VCCO_3	U12	
3	VCCO_3	V3	
3	VCCO_3	V8	
3	VCCO_3	V11	
3	VCCO_3	V12	
3	VCCO_3	W11	
3	VCCO_3	W12	
3	VCCO_3	Y11	
3	VCCO_3	AB6	
3	VCCO_3	AE3	
4	VCCO_4	Y13	
4	VCCO_4	Y14	
4	VCCO_4	Y15	
4	VCCO_4	AA12	
4	VCCO_4	AA13	
4	VCCO_4	AA14	
4	VCCO_4	AA15	
4	VCCO_4	AD14	
4	VCCO_4	AF10	
4	VCCO_4	AJ7	
4	VCCO_4	AJ14	
5	VCCO_5	Y17	
5	VCCO_5	Y18	
5	VCCO_5	Y19	
5	VCCO_5	AA17	
5	VCCO_5	AA18	
5	VCCO_5	AA19	
5	VCCO_5	AA20	
5	VCCO_5	AD18	
5	VCCO_5	AF22	

BF957 Flip-Chip BGA Package Specifications (1.27mm pitch)

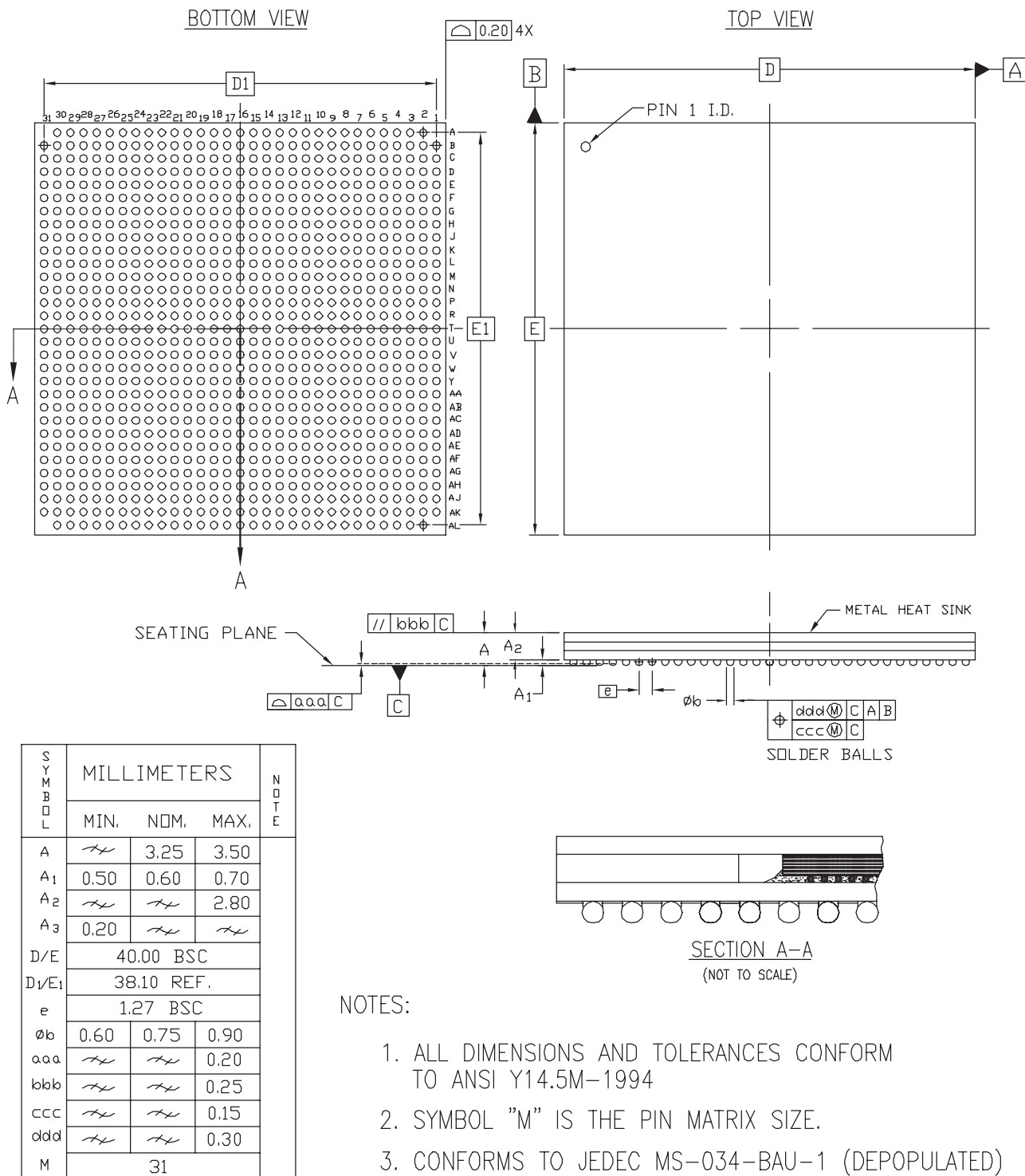


Figure 10: BF957 Flip-Chip BGA Package Specifications