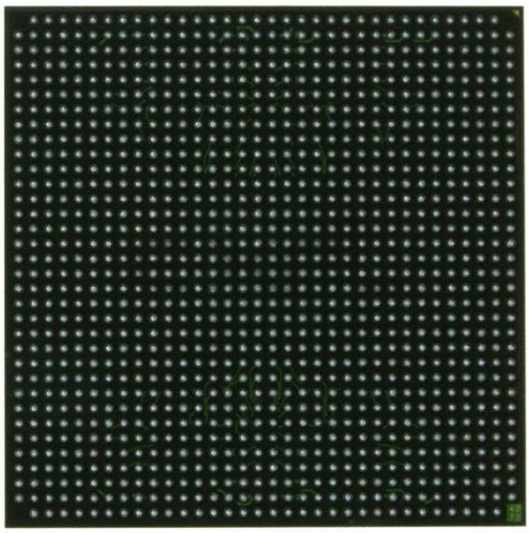

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

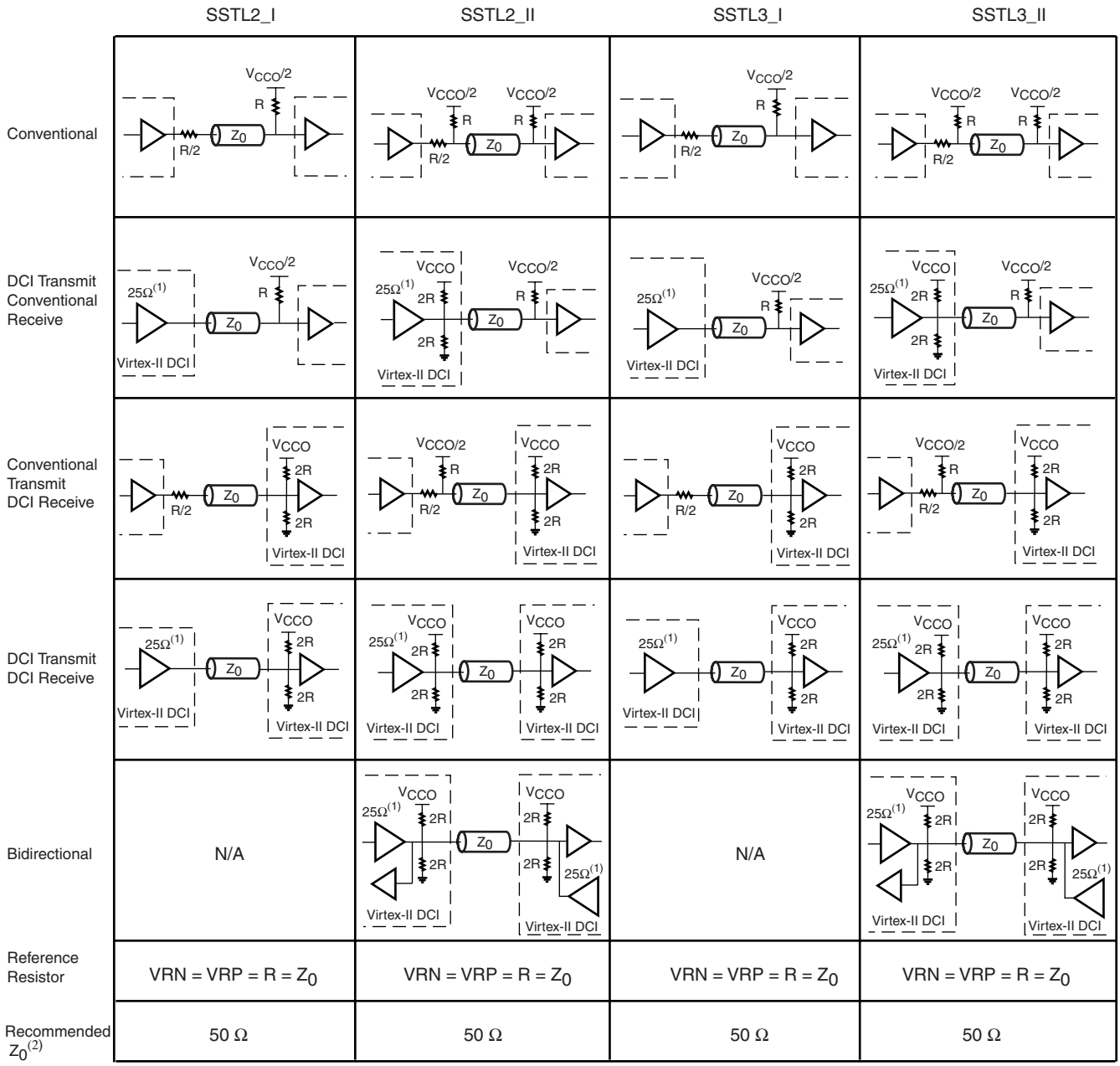
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	8448
Number of Logic Elements/Cells	-
Total RAM Bits	2654208
Number of I/O	824
Number of Gates	6000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v6000-5ffg1152i

Figure 12 provides examples illustrating the use of the SSTL2_I_DCI, SSTL2_II_DCI, SSTL3_I_DCI, and SSTL3_II_DCI I/O standards. For a complete list, see the **Virtex-II Platform FPGA User Guide**.



Notes:
1. The SSTL-compatible 25Ω series resistor is accounted for in the DCI buffer, and it is not DCI controlled.
2. Z_0 is the recommended PCB trace impedance.

DS031_65b_112502

Figure 12: **SSTL DCI Usage Examples**

Figure 18, Figure 19, and Figure 20 illustrate various example configurations.

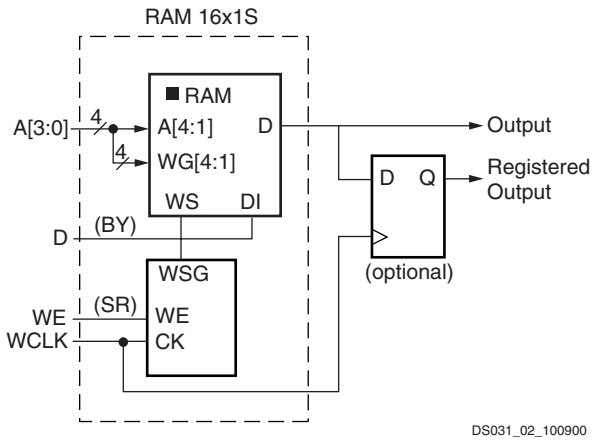


Figure 18: **Distributed SelectRAM (RAM16x1S)**

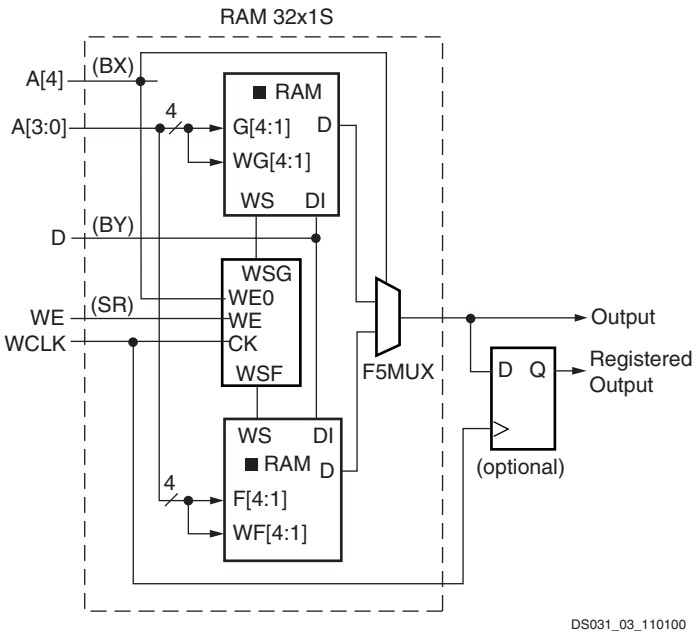


Figure 19: **Single-Port Distributed SelectRAM (RAM32x1S)**

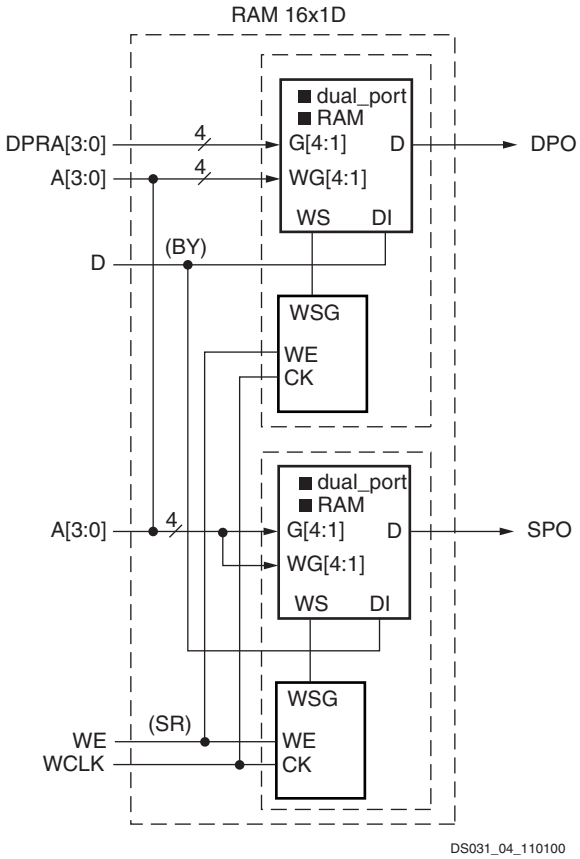


Figure 20: **Dual-Port Distributed SelectRAM (RAM16x1D)**

Similar to the RAM configuration, each function generator (LUT) can implement a 16 x 1-bit ROM. Five configurations are available: ROM16x1, ROM32x1, ROM64x1, ROM128x1, and ROM256x1. The ROM elements are cascadable to implement wider or/and deeper ROM. ROM contents are loaded at configuration. Table 10 shows the number of LUTs occupied by each configuration.

Table 10: **ROM Configuration**

ROM	Number of LUTs
16 x 1	1
32 x 1	2
64 x 1	4
128 x 1	8 (1 CLB)
256 x 1	16 (2 CLBs)

Multiplexers

Virtex-II function generators and associated multiplexers can implement the following:

- 4:1 multiplexer in one slice
- 8:1 multiplexer in two slices
- 16:1 multiplexer in one CLB element (4 slices)
- 32:1 multiplexer in two CLB elements (8 slices)

Each Virtex-II slice has one MUXF5 multiplexer and one MUXFX multiplexer. The MUXFX multiplexer implements the MUXF6, MUXF7, or MUXF8, as shown in Figure 23. Each CLB element has two MUXF6 multiplexers, one MUXF7 multiplexer and one MUXF8 multiplexer. Examples of multiplexers are shown in the *Virtex-II Platform FPGA User Guide*. Any LUT can implement a 2:1 multiplexer.

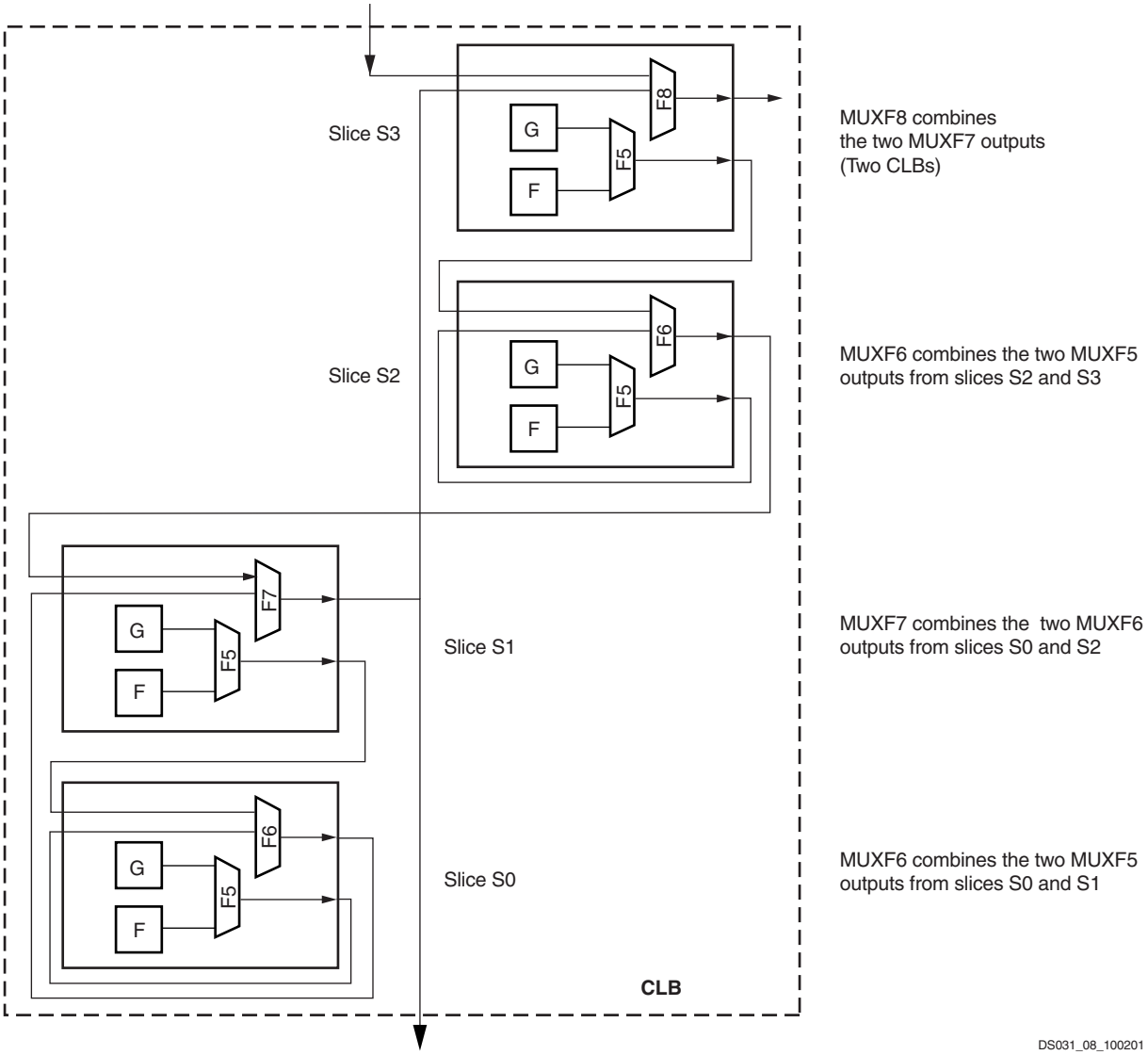


Figure 23: **MUXF5 and MUXFX multiplexers**

Fast Lookahead Carry Logic

Dedicated carry logic provides fast arithmetic addition and subtraction. The Virtex-II CLB has two separate carry chains, as shown in the Figure 24.

The height of the carry chains is two bits per slice. The carry chain in the Virtex-II device is running upward. The dedicated carry path and carry multiplexer (MUXCY) can also be used to cascade function generators for implementing wide logic functions.

Arithmetic Logic

The arithmetic logic includes an XOR gate that allows a 2-bit full adder to be implemented within a slice. In addition, a dedicated AND (MULT_AND) gate (shown in Figure 16) improves the efficiency of multiplier implementation.

Table 13: **Virtex-II Logic Resources Available in All CLBs**

Device	CLB Array: Row x Column	Number of Slices	Number of LUTs	Max Distributed SelectRAM or Shift Register (bits)	Number of Flip-Flops	Number of Carry-Chains(1)	Number of SOP Chains(1)
XC2V40	8 x 8	256	512	8,192	512	16	16
XC2V80	16 x 8	512	1,024	16,384	1,024	16	32
XC2V250	24 x 16	1,536	3,072	49,152	3,072	32	48
XC2V500	32 x 24	3,072	6,144	98,304	6,144	48	64
XC2V1000	40 x 32	5,120	10,240	163,840	10,240	64	80
XC2V1500	48 x 40	7,680	15,360	245,760	15,360	80	96
XC2V2000	56 x 48	10,752	21,504	344,064	21,504	96	112
XC2V3000	64 x 56	14,336	28,672	458,752	28,672	112	128
XC2V4000	80 x 72	23,040	46,080	737,280	46,080	144	160
XC2V6000	96 x 88	33,792	67,584	1,081,344	67,584	176	192
XC2V8000	112 x 104	46,592	93,184	1,490,944	93,184	208	224

Notes:
1. The carry-chains and SOP chains can be split or cascaded.

18 Kbit Block SelectRAM Resources

Introduction

Virtex-II devices incorporate large amounts of 18 Kbit block SelectRAM. These complement the distributed SelectRAM resources that provide shallow RAM structures implemented in CLBs. Each Virtex-II block SelectRAM is an 18 Kbit true dual-port RAM with two independently clocked and independently controlled synchronous ports that access a common storage area. Both ports are functionally identical. CLK, EN, WE, and SSR polarities are defined through configuration.

Each port has the following types of inputs: Clock and Clock Enable, Write Enable, Set/Reset, and Address, as well as separate Data/parity data inputs (for write) and Data/parity data outputs (for read).

Operation is synchronous; the block SelectRAM behaves like a register. Control, address and data inputs must (and need only) be valid during the set-up time window prior to a rising (or falling, a configuration option) clock edge. Data outputs change as a result of the same clock edge.

Configuration

The Virtex-II block SelectRAM supports various configurations, including single- and dual-port RAM and various data/address aspect ratios. Supported memory configurations for single- and dual-port modes are shown in Table 14.

Table 14: **Dual- and Single-Port Configurations**

16K x 1 bit	2K x 9 bits
8K x 2 bits	1K x 18 bits
4K x 4 bits	512 x 36 bits

Single-Port Configuration

As a single-port RAM, the block SelectRAM has access to the 18 Kbit memory locations in any of the 2K x 9-bit, 1K x 18-bit, or 512 x 36-bit configurations and to 16 Kbit memory locations in any of the 16K x 1-bit, 8K x 2-bit, or 4K x 4-bit configurations. The advantage of the 9-bit, 18-bit and 36-bit widths is the ability to store a parity bit for each eight bits. Parity bits must be generated or checked externally in user logic. In such cases, the width is viewed as 8 + 1, 16 + 2, or 32 + 4. These extra parity bits are stored and behave exactly as the other bits, including the timing parameters. Video applications can use the 9-bit ratio of Virtex-II block SelectRAM memory to advantage.

Each block SelectRAM cell is a fully synchronous memory as illustrated in Figure 29. Input data bus and output data bus widths are identical.

Configuration

Virtex-II devices are configured by loading application specific configuration data into the internal configuration memory. Configuration is carried out using a subset of the device pins, some of which are dedicated, while others can be re-used as general purpose inputs and outputs once configuration is complete.

Depending on the system design, several configuration modes are supported, selectable via mode pins. The mode pins M2, M1 and M0 are dedicated pins. The M2, M1, and M0 mode pins should be set at a constant DC voltage level, either through pull-up or pull-down resistors, or tied directly to ground or V_{CCAUX}. The mode pins should not be toggled during and after configuration.

An additional pin, HSWAP_EN is used in conjunction with the mode pins to select whether user I/O pins have pull-ups during configuration. By default, HSWAP_EN is tied High (internal pull-up) which shuts off the pull-ups on the user I/O pins during configuration. When HSWAP_EN is tied Low, user I/Os have pull-ups during configuration. Other dedicated pins are CCLK (the configuration clock pin), DONE, PROG_B, and the Boundary-Scan pins: TDI, TDO, TMS, and TCK. Depending on the configuration mode chosen, CCLK can be an output generated by the FPGA, or an input accepting an externally generated clock. The configuration pins and Boundary-Scan pins are independent of the V_{CCO}. The auxiliary power supply (V_{CCAUX}) of 3.3V is used for these pins. All configuration pins are LVTTL 12 mA. (See Virtex-II DC Characteristics in Module 3.)

A persist option is available which can be used to force the configuration pins to retain their configuration function even after device configuration is complete. If the persist option is not selected then the configuration pins with the exception of CCLK, PROG_B, and DONE can be used as user I/O in normal operation. The persist option does not apply to the Boundary-Scan related pins. The persist feature is valuable in applications which employ partial reconfiguration or reconfiguration on the fly.

Configuration Modes

Virtex-II supports the following five configuration modes:

- Slave-Serial Mode
- Master-Serial Mode
- Slave SelectMAP Mode
- Master SelectMAP Mode
- Boundary-Scan (JTAG, IEEE 1532) Mode

A detailed description of configuration modes is provided in the Virtex-II *User Guide*.

Slave-Serial Mode

In slave-serial mode, the FPGA receives configuration data in bit-serial form from a serial PROM or other serial source of configuration data. The CCLK pin on the FPGA is an input in this mode. The serial bitstream must be setup at the DIN input pin a short time before each rising edge of the externally generated CCLK.

Multiple FPGAs can be daisy-chained for configuration from a single source. After a particular FPGA has been configured, the data for the next device is routed internally to the DOUT pin. The data on the DOUT pin changes on the falling edge of CCLK.

Slave-serial mode is selected by applying <111> to the mode pins (M2, M1, M0). A weak pull-up on the mode pins makes slave serial the default mode if the pins are left unconnected.

Master-Serial Mode

In master-serial mode, the CCLK pin is an output pin. It is the Virtex-II FPGA device that drives the configuration clock on the CCLK pin to a Xilinx Serial PROM which in turn feeds bit-serial data to the DIN input. The FPGA accepts this data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the falling CCLK edge.

The interface is identical to slave serial except that an internal oscillator is used to generate the configuration clock (CCLK). A wide range of frequencies can be selected for CCLK which always starts at a slow default frequency. Configuration bits then switch CCLK to a higher frequency for the remainder of the configuration.

Slave SelectMAP Mode

The SelectMAP mode is the fastest configuration option. Byte-wide data is written into the Virtex-II FPGA device with a BUSY flag controlling the flow of data. An external data source provides a byte stream, CCLK, an active Low Chip Select (CS_B) signal and a Write signal (RDWR_B). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low. Data can also be read using the SelectMAP mode. If RDWR_B is asserted, configuration data is read out of the FPGA as part of a readback operation.

After configuration, the pins of the SelectMAP port can be used as additional user I/O. Alternatively, the port can be retained to permit high-speed 8-bit readback using the persist option.

Multiple Virtex-II FPGAs can be configured using the SelectMAP mode, and be made to start-up simultaneously. To configure multiple devices in this way, wire the individual CCLK, Data, RDWR_B, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by deasserting the CS_B pin of each device in turn and writing the appropriate data.

Master SelectMAP Mode

This mode is a master version of the SelectMAP mode. The device is configured byte-wide on a CCLK supplied by the

Notice of Disclaimer

Virtex-II Data Sheet

The Virtex-II Data Sheet contains the following modules:

- Virtex-II Platform FPGAs: Introduction and Overview (Module 1)
- Virtex-II Platform FPGAs: Functional Description (Module 2)
- Virtex-II Platform FPGAs: DC and Switching Characteristics (Module 3)
- Virtex-II Platform FPGAs: Pinout Information (Module 4)

Extended LVDS DC Specifications (LVDSEXT_33 & LVDSEXT_25)

Table 9: **Extended LVDS DC Specifications**

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}			3.3 or 2.5		V
Output High voltage for Q and $\overline{Q}$	V_{OH}	R_T = 100 Ω across Q and $\overline{Q}$ signals			1.785	V
Output Low voltage for Q and $\overline{Q}$	V_{OL}	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.705			V
Differential output voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{ODIFF}	R_T = 100 Ω across Q and $\overline{Q}$ signals	440		820	mV
Output common-mode voltage	V_{OCM}	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.200	1.375	V
Differential input voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{IDIFF}	Common-mode input voltage = 1.25 V	100	350	N/A	mV
Input common-mode voltage	V_{ICM}	Differential input voltage = ±350 mV	0.2	1.25	V_{CCO} – 0.5	V

LVPECL DC Specifications

These values are valid when driving a 100 Ω differential load only, i.e., a 100 Ω resistor between the two receiver pins. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. Table 10 summarizes the DC output specifications of LVPECL. For more information on using LVPECL, see the *Virtex-II User Guide*.

Table 10: **LVPECL DC Specifications**

DC Parameter	Min	Max	Min	Max	Min	Max	Units
V_{CCO}	3.0		3.3		3.6		V
V_{OH}	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{OL}	0.96	1.27	1.06	1.43	1.30	1.57	V
V_{IH}	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	0.86	2.125	0.86	2.125	0.86	2.125	V
Differential Input Voltage	0.3	–	0.3	–	0.3	–	V

CLB Distributed RAM Switching Characteristics

Table 22: **CLB Distributed RAM Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Sequential Delays					
Clock CLK to X/Y outputs (WE active) in 16 x 1 mode	$T_{SHCKO16}$	1.63	1.79	2.05	ns, Max
Clock CLK to X/Y outputs (WE active) in 32 x 1 mode	$T_{SHCKO32}$	1.97	2.17	2.49	ns, Max
Clock CLK to F5 output	$T_{SHCKOF5}$	1.77	1.94	2.23	ns, Max
Setup and Hold Times Before/After Clock CLK					
BX/BY data inputs (DIN)	T_{DS}/T_{DH}	0.53/–0.09	0.58/–0.10	0.67/–0.11	ns, Min
F/G address inputs	T_{AS}/T_{AH}	0.40/ 0.00	0.44/ 0.00	0.50/ 0.00	ns, Min
SR input (WS)	T_{WES}/T_{WEH}	0.42/–0.01	0.46/–0.01	0.53/–0.01	ns, Min
Clock CLK					
Minimum Pulse Width, High	T_{WPH}	0.57	0.63	0.72	ns, Min
Minimum Pulse Width, Low	T_{WPL}	0.57	0.63	0.72	ns, Min
Minimum clock period to meet address write cycle time	T_{WC}	1.14	1.25	1.44	ns, Min

CLB Shift Register Switching Characteristics

Table 23: **CLB Shift Register Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Sequential Delays					
Clock CLK to X/Y outputs	T_{REG}	2.31	2.54	2.92	ns, Max
Clock CLK to X/Y outputs	T_{REG32}	2.65	2.92	3.35	ns, Max
Clock CLK to XB output via MC15 LUT output	T_{REGXB}	2.23	2.46	2.82	ns, Max
Clock CLK to YB output via MC15 LUT output	T_{REGYB}	2.18	2.40	2.75	ns, Max
Clock CLK to Shiftout	T_{CKSH}	1.92	2.11	2.43	ns, Max
Clock CLK to F5 output	T_{REGF5}	2.45	2.69	3.09	ns, Max
Setup and Hold Times Before/After Clock CLK					
BX/BY data inputs (DIN)	T_{SRLDS}/T_{SRLDH}	0.53/–0.07	0.58/–0.08	0.67/–0.09	ns, Min
SR input (WS)	T_{WSS}/T_{WSH}	0.19/–0.06	0.21/–0.07	0.24/–0.08	ns, Min
Clock CLK					
Minimum Pulse Width, High	T_{SRPH}	0.57	0.63	0.72	ns, Min
Minimum Pulse Width, Low	T_{SRPL}	0.57	0.63	0.72	ns, Min

Source Synchronous Timing Budgets

This section describes how to use the parameters provided in the Source-Synchronous Switching Characteristics section to develop system-specific timing budgets. The following analysis provides information necessary for determining Virtex-II contributions to an overall system timing analysis; no assumptions are made about the effects of Inter-Symbol Interference or PCB skew.

Virtex-II Transmitter Data-Valid Window (T_X)

T_X is the minimum aggregate valid data period for a source-synchronous data bus at the pins of the device and is calculated as follows:

$$T_X = \text{Data Period} - [\text{Jitter}^{(1)} + \text{Duty Cycle Distortion}^{(2)} + \text{TCKSKEW}^{(3)} + \text{TPKGSKEW}^{(4)}]$$

Notes:

1. Jitter values and accumulation methodology to be provided in a future release of this document. The absolute period jitter values found in the DCM Timing Parameters section of the particular DCM output clock used to clock the IOB FF can be used for a best case analysis.
2. This value depends on the clocking methodology used. See Note1 for Table 45.
3. This value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.
4. These values represent the worst-case skew between any two balls of the package: shortest flight time to longest flight time from Pad to Ball.

Virtex-II Receiver Data-Valid Window (R_X)

R_X is the required minimum aggregate valid data period for a source-synchronous data bus at the pins of the device and is calculated as follows:

$$R_X = [\text{TSAMP}^{(1)} + \text{TCKSKEW}^{(2)} + \text{TPKGSKEW}^{(3)}]$$

Notes:

1. This parameter indicates the total sampling error of Virtex-II DDR input registers across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 and CLK180 DCM jitter in a quiet system
   - Worst-case duty-cycle distortion
   - DCM accuracy (phase offset)
   - DCM phase shift resolution.

   These measurements do not include package or clock tree skew.
2. This value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.
3. These values represent the worst-case skew between any two balls of the package: shortest flight time to longest flight time from Pad to Ball.

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
11/07/00	1.0	Early access draft.
12/06/00	1.1	Initial release.
01/15/01	1.2	Added values to the tables in the Virtex-II Performance Characteristics and Virtex-II Switching Characteristics sections.
01/25/01	1.3	• The data sheet was divided into four modules (per the current style standard). • Updated values in the Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables. • Table 18, "Delay Measurement Methodology"
04/23/01	1.5	• Updated values in the Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables. • Added T_{REG32} symbol to Table 23. • Skipped v1.4 to sync with other modules. Reverted to traditional double-column format.

Table 5: **CS144/CSG144 — XC2V40, XC2V80, and XC2V250**

Bank	Pin Description	Pin Number	No Connect in the XC2V40
2	IO_L96N_2	G11	
2	IO_L96P_2	G13	
3	IO_L96N_3	G12	
3	IO_L96P_3	H12	
3	IO_L94N_3	H11	
3	IO_L94P_3	J13	
3	IO_L03N_3/VREF_3	J10	
3	IO_L03P_3	K13	
3	IO_L02N_3/VRP_3	K12	
3	IO_L02P_3/VRN_3	K11	
3	IO_L01N_3	K10	
3	IO_L01P_3	L13	
4	IO_L01N_4/BUSY/DOUT(1)	M11	
4	IO_L01P_4/INIT_B	N11	
4	IO_L02N_4/D0/DIN(1)	L10	
4	IO_L02P_4/D1	M10	
4	IO_L03N_4/D2/ALT_VRP_4	N10	
4	IO_L03P_4/D3/ALT_VRN_4	K9	
4	IO_L94N_4/VREF_4	N9	
4	IO_L94P_4	K8	
4	IO_L95N_4/GCLK3S	L8	
4	IO_L95P_4/GCLK2P	M8	
4	IO_L96N_4/GCLK1S	N8	
4	IO_L96P_4/GCLK0P	K7	
5	IO_L96N_5/GCLK7S	N7	
5	IO_L96P_5/GCLK6P	M7	
5	IO_L95N_5/GCLK5S	N6	
5	IO_L95P_5/GCLK4P	M6	
5	IO_L94N_5	L6	
5	IO_L94P_5/VREF_5	K6	
5	IO_L03N_5/D4/ALT_VRP_5	L5	
5	IO_L03P_5/D5/ALT_VRN_5	K5	
5	IO_L02N_5/D6	N4	
5	IO_L02P_5/D7	M4	
5	IO_L01N_5/RDWR_B	L4	
5	IO_L01P_5/CS_B	K4	

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
NA	GND	M10		
NA	GND	M9		
NA	GND	L14		
NA	GND	L13		
NA	GND	L12		
NA	GND	L11		
NA	GND	L10		
NA	GND	L9		
NA	GND	K14		
NA	GND	K13		
NA	GND	K12		
NA	GND	K11		
NA	GND	K10		
NA	GND	K9		
NA	GND	J14		
NA	GND	J13		
NA	GND	J12		
NA	GND	J11		
NA	GND	J10		
NA	GND	J9		
NA	GND	D19		
NA	GND	D4		
NA	GND	C20		
NA	GND	C3		
NA	GND	B21		
NA	GND	B2		
NA	GND	A22		
NA	GND	A1		

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
4	IO_L78N_4	Y15	NC	
4	IO_L78P_4	AA15	NC	
4	IO_L91N_4/VREF_4	W15		
4	IO_L91P_4	W16		
4	IO_L92N_4	AB15		
4	IO_L92P_4	AC15		
4	IO_L93N_4	AD15		
4	IO_L93P_4	AE15		
4	IO_L94N_4/VREF_4	W14		
4	IO_L94P_4	Y14		
4	IO_L95N_4/GCLK3S	AA14		
4	IO_L95P_4/GCLK2P	AB14		
4	IO_L96N_4/GCLK1S	AC14		
4	IO_L96P_4/GCLK0P	AD14		
5	IO_L96N_5/GCLK7S	AC13		
5	IO_L96P_5/GCLK6P	AB13		
5	IO_L95N_5/GCLK5S	AA13		
5	IO_L95P_5/GCLK4P	Y13		
5	IO_L94N_5	W13		
5	IO_L94P_5/VREF_5	W12		
5	IO_L93N_5	AF15		
5	IO_L93P_5	AF14		
5	IO_L92N_5	AF13		
5	IO_L92P_5	AF12		
5	IO_L91N_5	AE12		
5	IO_L91P_5/VREF_5	AD12		
5	IO_L78N_5	AC12	NC	
5	IO_L78P_5	AB12	NC	
5	IO_L76N_5	AA12	NC	
5	IO_L76P_5	Y12	NC	
5	IO_L75N_5/VREF_5	AF11	NC	
5	IO_L75P_5	AF10	NC	
5	IO_L73N_5	AE11	NC	
5	IO_L73P_5	AD11	NC	
5	IO_L72N_5	AC11		
5	IO_L72P_5	AB11		

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
5	IO_L70N_5	W11		
5	IO_L70P_5	Y10		
5	IO_L69N_5/VREF_5	Y11		
5	IO_L69P_5	AA11		
5	IO_L67N_5	AF9		
5	IO_L67P_5	AF8		
5	IO_L54N_5	AE9		
5	IO_L54P_5	AD9		
5	IO_L52N_5	AB10		
5	IO_L52P_5	AA10		
5	IO_L51N_5/VREF_5	AD10		
5	IO_L51P_5	AC10		
5	IO_L49N_5	AE8		
5	IO_L49P_5	AF7		
5	IO_L28N_5	AD8	NC	NC
5	IO_L28P_5	AC8	NC	NC
5	IO_L27N_5/VREF_5	AB9	NC	NC
5	IO_L27P_5	AC9	NC	NC
5	IO_L25N_5	AA9	NC	NC
5	IO_L25P_5	Y9	NC	NC
5	IO_L24N_5	AF6		
5	IO_L24P_5	AE6		
5	IO_L22N_5	AB8		
5	IO_L22P_5	AA8		
5	IO_L21N_5/VREF_5	AC7		
5	IO_L21P_5	AD7		
5	IO_L19N_5	AF5		
5	IO_L19P_5	AE5		
5	IO_L06N_5	AF4		
5	IO_L06P_5	AE4		
5	IO_L05N_5/VRP_5	AF3		
5	IO_L05P_5/VRN_5	AE3		
5	IO_L04N_5	Y8		
5	IO_L04P_5/VREF_5	Y7		
5	IO_L03N_5/D4/ALT_VRP_5	AB7		
5	IO_L03P_5/D5/ALT_VRN_5	AA7		
5	IO_L02N_5/D6	AD6		

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
NA	GND	Y5		
NA	GND	W19		
NA	GND	W6		
NA	GND	V24		
NA	GND	V18		
NA	GND	V7		
NA	GND	V1		
NA	GND	R21		
NA	GND	R4		
NA	GND	P14		
NA	GND	P13		
NA	GND	P12		
NA	GND	P11		
NA	GND	N14		
NA	GND	N13		
NA	GND	N12		
NA	GND	N11		
NA	GND	M14		
NA	GND	M13		
NA	GND	M12		
NA	GND	M11		
NA	GND	L14		
NA	GND	L13		
NA	GND	L12		
NA	GND	L11		
NA	GND	K21		
NA	GND	K4		
NA	GND	G24		
NA	GND	G18		
NA	GND	G7		
NA	GND	G1		
NA	GND	F19		
NA	GND	F6		
NA	GND	E20		
NA	GND	E5		
NA	GND	D21		

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
3	IO_L19N_3	AB26
3	IO_L19P_3	AB25
3	IO_L06N_3	AB24
3	IO_L06P_3	AB23
3	IO_L04N_3	AC27
3	IO_L04P_3	AC26
3	IO_L03N_3/VREF_3	AC25
3	IO_L03P_3	AC24
3	IO_L02N_3/VRP_3	AD27
3	IO_L02P_3/VRN_3	AE27
3	IO_L01N_3	AD26
3	IO_L01P_3	AD25
4	IO_L01N_4/BUSY/DOUT(1)	AF25
4	IO_L01P_4/INIT_B	AG25
4	IO_L02N_4/D0/DIN(1)	AF24
4	IO_L02P_4/D1	AG24
4	IO_L03N_4/D2/ALT_VRP_4	AD23
4	IO_L03P_4/D3/ALT_VRN_4	AE23
4	IO_L04N_4/VREF_4	AF23
4	IO_L04P_4	AG23
4	IO_L05N_4/VRP_4	AD22
4	IO_L05P_4/VRN_4	AE22
4	IO_L06N_4	AF22
4	IO_L06P_4	AG22
4	IO_L19N_4	AC21
4	IO_L19P_4	AB21
4	IO_L21N_4	AE21
4	IO_L21P_4/VREF_4	AE20
4	IO_L22N_4	AF21
4	IO_L22P_4	AG21
4	IO_L24N_4	AB20
4	IO_L24P_4	AA20
4	IO_L25N_4	AC20
4	IO_L25P_4	AD20
4	IO_L27N_4	AG20

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
NA	VCCAUX	P26
NA	VCCAUX	P2
NA	VCCAUX	C26
NA	VCCAUX	C2
NA	VCCAUX	B14
NA	VCCINT	V18
NA	VCCINT	V14
NA	VCCINT	V10
NA	VCCINT	U17
NA	VCCINT	U16
NA	VCCINT	U15
NA	VCCINT	U14
NA	VCCINT	U13
NA	VCCINT	U12
NA	VCCINT	U11
NA	VCCINT	T17
NA	VCCINT	T11
NA	VCCINT	R17
NA	VCCINT	R11
NA	VCCINT	P18
NA	VCCINT	P17
NA	VCCINT	P11
NA	VCCINT	P10
NA	VCCINT	N17
NA	VCCINT	N11
NA	VCCINT	M17
NA	VCCINT	M11
NA	VCCINT	L17
NA	VCCINT	L16
NA	VCCINT	L15
NA	VCCINT	L14
NA	VCCINT	L13
NA	VCCINT	L12
NA	VCCINT	L11
NA	VCCINT	K18
NA	VCCINT	K14

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
1	IO_L69N_1/VREF_1	E15		
1	IO_L69P_1	E16		
1	IO_L68N_1	K17		
1	IO_L68P_1	K16		
1	IO_L67N_1	C15		
1	IO_L67P_1	B15		
1	IO_L60N_1	F15		
1	IO_L60P_1	F16		
1	IO_L59N_1	H16		
1	IO_L59P_1	H15		
1	IO_L58N_1	C13		
1	IO_L58P_1	C14		
1	IO_L57N_1/VREF_1	D13		
1	IO_L57P_1	D14		
1	IO_L56N_1	M17		
1	IO_L56P_1	M16		
1	IO_L55N_1	A12		
1	IO_L55P_1	A13		
1	IO_L54N_1	B12		
1	IO_L54P_1	B13		
1	IO_L53N_1	G15		
1	IO_L53P_1	G14		
1	IO_L52N_1	C11		
1	IO_L52P_1	C12		
1	IO_L51N_1/VREF_1	F13		
1	IO_L51P_1	F14		
1	IO_L50N_1	L16		
1	IO_L50P_1	L15		
1	IO_L49N_1	A10		
1	IO_L49P_1	A11		
1	IO_L36N_1	E12	NC	
1	IO_L36P_1	E13	NC	
1	IO_L35N_1	K15	NC	
1	IO_L35P_1	J14	NC	
1	IO_L34N_1	B9	NC	
1	IO_L34P_1	B10	NC	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
5	IO_L79N_5	AV24		
5	IO_L79P_5	AV23		
5	IO_L78N_5	AP23		
5	IO_L78P_5	AP22		
5	IO_L77N_5	AJ21		
5	IO_L77P_5	AJ22		
5	IO_L76N_5	AU24		
5	IO_L76P_5	AU23		
5	IO_L75N_5/VREF_5	AT25		
5	IO_L75P_5	AT24		
5	IO_L74N_5	AH21		
5	IO_L74P_5	AH22		
5	IO_L73N_5	AW26		
5	IO_L73P_5	AW25		
5	IO_L72N_5	AR25		
5	IO_L72P_5	AR24		
5	IO_L71N_5	AN23		
5	IO_L71P_5	AN24		
5	IO_L70N_5	AU25		
5	IO_L70P_5	AV25		
5	IO_L69N_5/VREF_5	AL24		
5	IO_L69P_5	AL23		
5	IO_L68N_5	AK23		
5	IO_L68P_5	AK24		
5	IO_L67N_5	AU27		
5	IO_L67P_5	AU26		
5	IO_L60N_5	AP25		
5	IO_L60P_5	AP24		
5	IO_L59N_5	AM24		
5	IO_L59P_5	AM25		
5	IO_L58N_5	AW28		
5	IO_L58P_5	AW27		
5	IO_L57N_5/VREF_5	AT27		
5	IO_L57P_5	AT26		
5	IO_L56N_5	AH23		
5	IO_L56P_5	AH24		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
5	IO_L01N_5/RDWR_B	AU36		
5	IO_L01P_5/CS_B	AV36		
6	IO_L01P_6	AJ27		
6	IO_L01N_6	AH27		
6	IO_L02P_6/VRN_6	AT38		
6	IO_L02N_6/VRP_6	AR37		
6	IO_L03P_6	AP36		
6	IO_L03N_6/VREF_6	AR36		
6	IO_L04P_6	AJ28		
6	IO_L04N_6	AH29		
6	IO_L05P_6	AT39		
6	IO_L05N_6	AR39		
6	IO_L06P_6	AN34		
6	IO_L06N_6	AP35		
6	IO_L07P_6	AH28	NC	
6	IO_L07N_6	AG28	NC	
6	IO_L08P_6	AR38	NC	
6	IO_L08N_6	AP38	NC	
6	IO_L09P_6	AM34	NC	
6	IO_L09N_6/VREF_6	AM33	NC	
6	IO_L10P_6	AL32	NC	
6	IO_L10N_6	AK32	NC	
6	IO_L11P_6	AP37	NC	
6	IO_L11N_6	AN37	NC	
6	IO_L12P_6	AM35	NC	
6	IO_L12N_6	AN35	NC	
6	IO_L19P_6	AK31		
6	IO_L19N_6	AJ30		
6	IO_L20P_6	AP39		
6	IO_L20N_6	AN39		
6	IO_L21P_6	AK33		
6	IO_L21N_6/VREF_6	AL33		
6	IO_L22P_6	AJ31		
6	IO_L22N_6	AH31		
6	IO_L23P_6	AN38		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	VCCINT	R19		
NA	VCCINT	R18		
NA	VCCINT	R17		
NA	VCCINT	R16		
NA	VCCINT	R15		
NA	VCCINT	P26		
NA	VCCINT	P20		
NA	VCCINT	P14		
NA	VCCINT	N27		
NA	VCCINT	N20		
NA	VCCINT	N13		
NA	GND	AW38		
NA	GND	AW37		
NA	GND	AW20		
NA	GND	AW3		
NA	GND	AW2		
NA	GND	AV39		
NA	GND	AV38		
NA	GND	AV37		
NA	GND	AV29		
NA	GND	AV11		
NA	GND	AV3		
NA	GND	AV2		
NA	GND	AV1		
NA	GND	AU39		
NA	GND	AU38		
NA	GND	AU37		
NA	GND	AU3		
NA	GND	AU2		
NA	GND	AU1		
NA	GND	AT36		
NA	GND	AT23		
NA	GND	AT20		
NA	GND	AT17		
NA	GND	AT4		
NA	GND	AR35		