AMD Xilinx - XC2V6000-5FFG1517C Datasheet

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	8448
Number of Logic Elements/Cells	-
Total RAM Bits	2654208
Number of I/O	1104
Number of Gates	6000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FCBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v6000-5ffg1517c

Multiplexers

Virtex-II function generators and associated multiplexers can implement the following:

- 4:1 multiplexer in one slice
- 8:1 multiplexer in two slices
- 16:1 multiplexer in one CLB element (4 slices)
- 32:1 multiplexer in two CLB elements (8 slices)

Each Virtex-II slice has one MUXF5 multiplexer and one MUXFX multiplexer. The MUXFX multiplexer implements the MUXF6, MUXF7, or MUXF8, as shown in Figure 23. Each CLB element has two MUXF6 multiplexers, one MUXF7 multiplexer and one MUXF8 multiplexer. Examples of multiplexers are shown in the *Virtex-II Platform FPGA User Guide*. Any LUT can implement a 2:1 multiplexer.

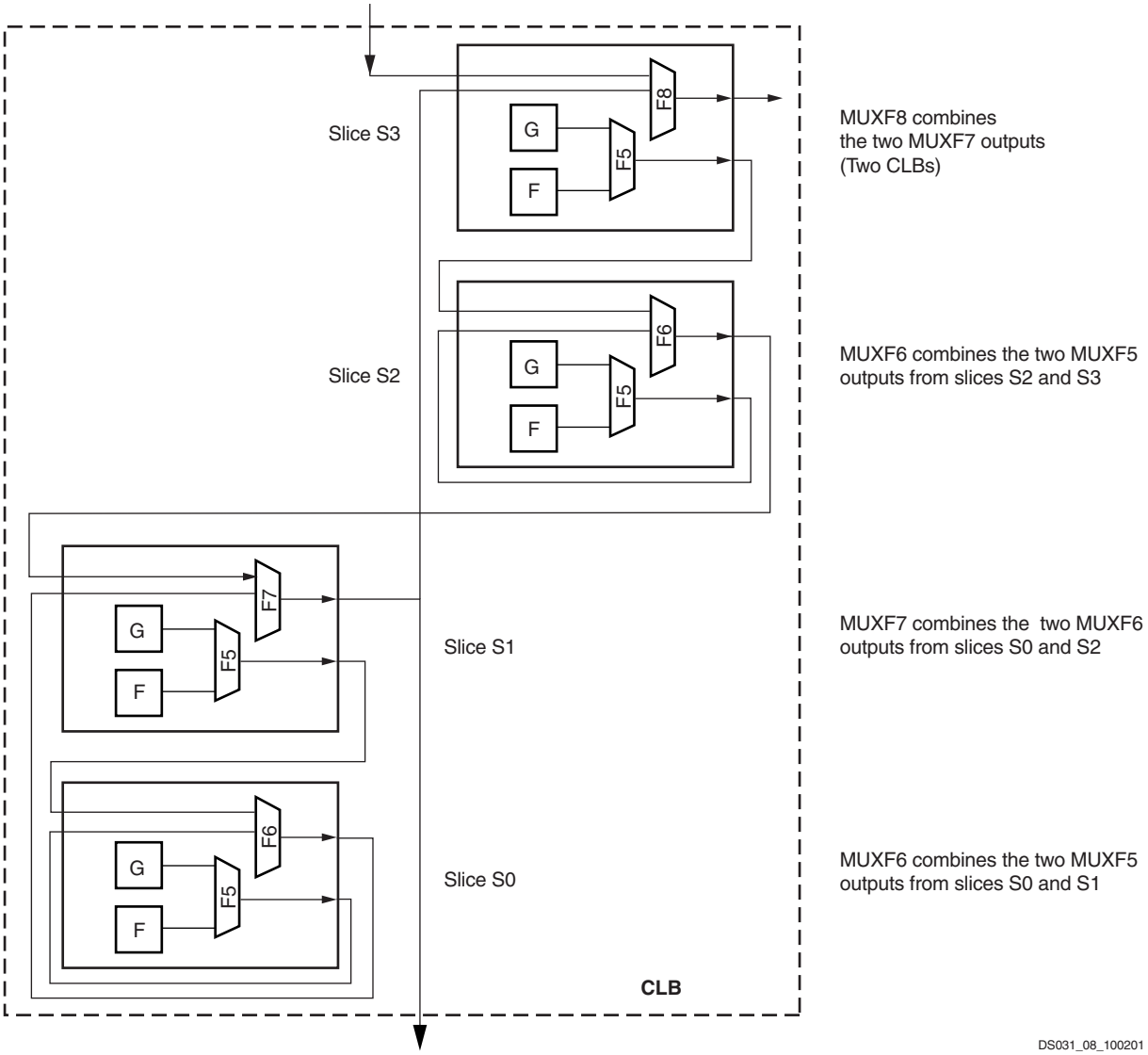


Figure 23: **MUXF5 and MUXFX multiplexers**

Fast Lookahead Carry Logic

Dedicated carry logic provides fast arithmetic addition and subtraction. The Virtex-II CLB has two separate carry chains, as shown in the Figure 24.

The height of the carry chains is two bits per slice. The carry chain in the Virtex-II device is running upward. The dedicated carry path and carry multiplexer (MUXCY) can also be used to cascade function generators for implementing wide logic functions.

Arithmetic Logic

The arithmetic logic includes an XOR gate that allows a 2-bit full adder to be implemented within a slice. In addition, a dedicated AND (MULT_AND) gate (shown in Figure 16) improves the efficiency of multiplier implementation.

3. "NO_CHANGE"

The "NO_CHANGE" option maintains the content of the output registers, regardless of the write operation. The clock edge during the write mode has no effect on the content of the data output register DO. When the port is configured as "NO_CHANGE", only a read operation loads a new value in the output register DO, as shown in Figure 33.

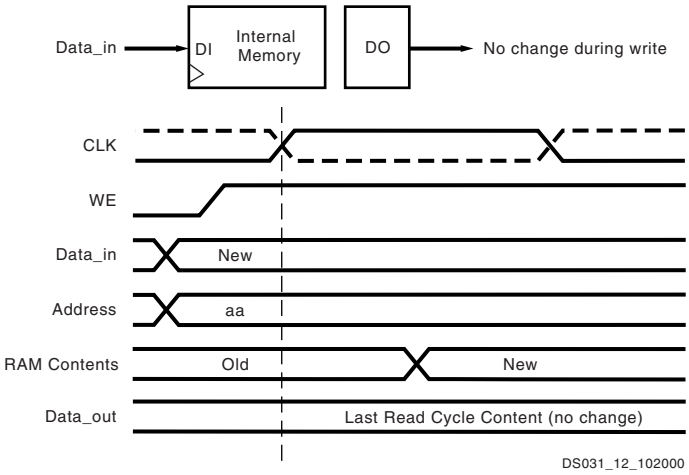


Figure 33: **NO_CHANGE Mode**

Control Pins and Attributes

Virtex-II SelectRAM memory has two independent ports with the control signals described in Table 17. All control inputs including the clock have an optional inversion.

Table 17: **Control Functions**

Control Signal	Function
CLK	Read and Write Clock
EN	Enable affects Read, Write, Set, Reset
WE	Write Enable
SSR	Set DO register to SRVAL (attribute)

Initial memory content is determined by the INIT_xx attributes. Separate attributes determine the output register value after device configuration (INIT) and SSR is asserted (SRVAL). Both attributes (INIT_B and SRVAL) are available for each port when a block SelectRAM resource is configured as dual-port RAM.

Locations

Virtex-II SelectRAM memory blocks are located in either four or six columns. The number of blocks per column depends of the device array size and is equivalent to the number of CLBs in a column divided by four. Column locations are shown in Table 18.

Table 18: **SelectRAM Memory Floor Plan**

Device	Columns	SelectRAM Blocks	
		Per Column	Total
XC2V40	2	2	4
XC2V80	2	4	8
XC2V250	4	6	24
XC2V500	4	8	32
XC2V1000	4	10	40
XC2V1500	4	12	48
XC2V2000	4	14	56
XC2V3000	6	16	96
XC2V4000	6	20	120
XC2V6000	6	24	144
XC2V8000	6	28	168

Clock Distribution Switching Characteristics

Table 20: **Clock Distribution Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Global Clock Buffer I input to O output	T_{GIO}	0.47	0.52	0.59	ns, Max
Global Clock Buffer S input Setup/Hold to I1 an I2 inputs	T_{GSI}/T_{GIS}	0.55/ 0	0.61/ 0	0.70/ 0	ns, Max

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used (see Figure 16 in Module 2). The values listed below are worst-case. Precise values are provided by the timing analyzer.

Table 21: **CLB Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Combinatorial Delays					
4-input function: F/G inputs to X/Y outputs	T_{ILO}	0.35	0.39	0.44	ns, Max
5-input function: F/G inputs to F5 output	T_{IF5}	0.57	0.63	0.72	ns, Max
5-input function: F/G inputs to X output	T_{IF5X}	0.76	0.83	0.95	ns, Max
FXINA or FXINB inputs to Y output via MUXFX	T_{IFXY}	0.36	0.39	0.45	ns, Max
FXINA input to FX output via MUXFX	T_{INAFX}	0.26	0.28	0.32	ns, Max
FXINB input to FX output via MUXFX	T_{INBFX}	0.26	0.28	0.32	ns, Max
SOPIN input to SOPOUT output via ORCY	T_{SOPSOP}	0.35	0.38	0.44	ns, Max
Incremental delay routing through transparent latch to XQ/YQ outputs	T_{IFNCTL}	0.41	0.45	0.51	ns, Max
Sequential Delays					
FF Clock CLK to XQ/YQ outputs	T_{CKO}	0.45	0.50	0.57	ns, Max
Latch Clock CLK to XQ/YQ outputs	T_{CKLO}	0.54	0.59	0.68	ns, Max
Setup and Hold Times Before/After Clock CLK					
BX/BY inputs	T_{DICK}/T_{CKDI}	0.30/–0.07	0.33/–0.08	0.37/–0.09	ns, Min
DY inputs	T_{DYCK}/T_{CKDY}	0.30/–0.07	0.33/–0.08	0.37/–0.09	ns, Min
DX inputs	T_{DXCK}/T_{CKDX}	0.30/–0.07	0.33/–0.08	0.37/–0.09	ns, Min
CE input	T_{CECK}/T_{CKCE}	0.19/–0.06	0.21/–0.07	0.24/–0.08	ns, Min
SR/BY inputs (synchronous)	T_{SRCK}/T_{SCKR}	0.21/–0.02	0.23/–0.03	0.26/–0.03	ns, Min
Clock CLK					
Minimum Pulse Width, High	T_{CH}	0.61	0.67	0.77	ns, Min
Minimum Pulse Width, Low	T_{CL}	0.61	0.67	0.77	ns, Min
Set/Reset					
Minimum Pulse Width, SR/BY inputs (asynchronous)	T_{RPW}	0.61	0.67	0.77	ns, Min
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	T_{RQ}	1.06	1.17	1.34	ns, Max
Toggle Frequency (MHz) (for export control)	F_{TOG}	820	750	650	MHz

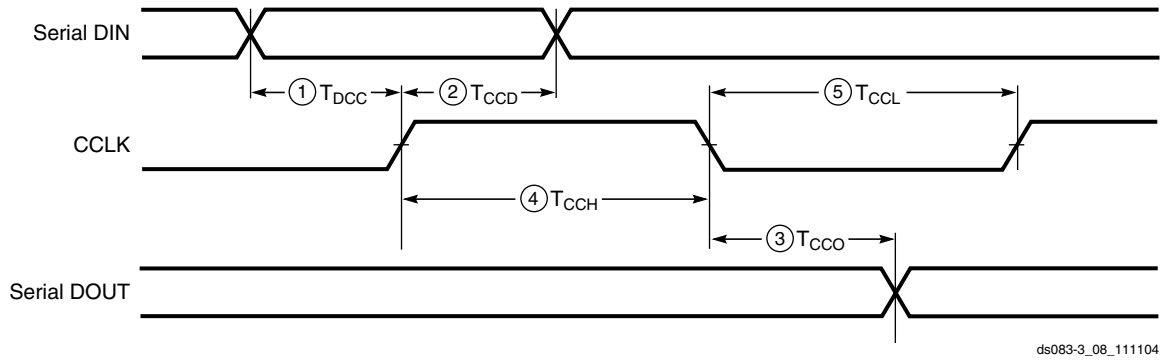


Figure 3: **Slave Serial Mode Timing Sequence**

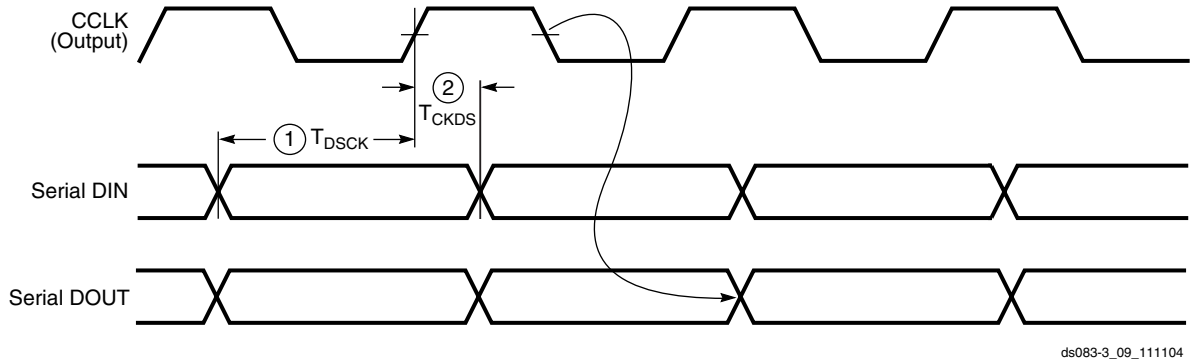


Figure 4: **Master Serial Mode Timing Sequence**

Table 31: **Master/Slave Serial Mode Timing Characteristics**

	Description	Figure References	Symbol	Value	Units
CCLK	DIN setup/hold, slave mode (Figure 3)	1/2	T_{DCC}/T_{CCD}	5.0/0.0	ns, min
	DIN setup/hold, master mode (Figure 4)	1/2	T_{DSCK}/T_{CKDS}	5.0/0.0	ns, min
	DOUT	3	T_{CCO}	12.0	ns, max
	High time	4	T_{CCH}	5.0	ns, min
	Low time	5	T_{CCL}	5.0	ns, min
	Maximum start-up frequency		$F_{CC\_STARTUP}$	50	MHz, max
	Maximum frequency		F_{CC_SERIAL}	66(1)	MHz, max
	Frequency tolerance, master mode with respect to nominal			+45% –30%	

Notes:
1. If no provision is made in the design to adjust the frequency of CCLK, F_{CC_SERIAL} should not exceed $F_{CC\_STARTUP}$.

Master/Slave SelectMAP Parameters

Figure 5 is a generic timing diagram for data loading using SelectMAP. For other data loading diagrams, refer to the ***Virtex-II Pro Platform FPGA User Guide***.

Virtex-II Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *With* DCM

Table 34: **Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *With* DCM**

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
LVTTL Global Clock Input to Output delay using Output flip-flop, 12 mA, Fast Slew Rate, *with* DCM. For data *output* with different standards, adjust the delays with the values shown in IOB Output Switching Characteristics Standard Adjustments, page 14.						
Global Clock and OFF with DCM	$T_{ICKOFDCM}$	XC2V40	1.10	1.28	1.48	ns
		XC2V80	1.10	1.28	1.48	ns
		XC2V250	1.10	1.28	1.48	ns
		XC2V500	1.10	1.28	1.48	ns
		XC2V1000	1.10	1.28	1.48	ns
		XC2V1500	1.10	1.28	1.48	ns
		XC2V2000	1.10	1.28	1.48	ns
		XC2V3000	1.19	1.38	1.59	ns
		XC2V4000	1.19	1.38	1.59	ns
		XC2V6000	1.64	1.88	2.17	ns
		XC2V8000		1.88	2.17	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with test setup shown in Figure 1. For other I/O standards, see Table 19.

Table 6: **FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
NA	GND	T16		
NA	GND	T1		
NA	GND	R15		
NA	GND	R2		
NA	GND	P14		
NA	GND	P3		
NA	GND	L11		
NA	GND	L6		
NA	GND	K10		
NA	GND	K9		
NA	GND	K8		
NA	GND	K7		
NA	GND	J10		
NA	GND	J9		
NA	GND	J8		
NA	GND	J7		
NA	GND	H10		
NA	GND	H9		
NA	GND	H8		
NA	GND	H7		
NA	GND	G10		
NA	GND	G9		
NA	GND	G8		
NA	GND	G7		
NA	GND	F11		
NA	GND	F6		
NA	GND	C14		
NA	GND	C3		
NA	GND	B15		
NA	GND	B2		
NA	GND	A16		
NA	GND	A1		

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
0	IO_L67P_0	C10		
0	IO_L69N_0	F10		
0	IO_L69P_0/VREF_0	G10		
0	IO_L70N_0	E10		
0	IO_L70P_0	D10		
0	IO_L72N_0	A10		
0	IO_L72P_0	A11		
0	IO_L73N_0	F11	NC	
0	IO_L73P_0	E11	NC	
0	IO_L75N_0	G11	NC	
0	IO_L75P_0/VREF_0	H11	NC	
0	IO_L76N_0	D11	NC	
0	IO_L76P_0	C11	NC	
0	IO_L78N_0	B11	NC	
0	IO_L78P_0	B12	NC	
0	IO_L91N_0/VREF_0	G12		
0	IO_L91P_0	H12		
0	IO_L92N_0	F12		
0	IO_L92P_0	E12		
0	IO_L93N_0	D12		
0	IO_L93P_0	C12		
0	IO_L94N_0/VREF_0	G13		
0	IO_L94P_0	H13		
0	IO_L95N_0/GCLK7P	F13		
0	IO_L95P_0/GCLK6S	E13		
0	IO_L96N_0/GCLK5P	D13		
0	IO_L96P_0/GCLK4S	C13		
1	IO_L96N_1/GCLK3P	H14		
1	IO_L96P_1/GCLK2S	H15		
1	IO_L95N_1/GCLK1P	G14		
1	IO_L95P_1/GCLK0S	F14		
1	IO_L94N_1	E14		
1	IO_L94P_1/VREF_1	D14		
1	IO_L93N_1	A12		
1	IO_L93P_1	A13		
1	IO_L92N_1	A14		

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
1	IO_L92P_1	A15		
1	IO_L91N_1	B15		
1	IO_L91P_1/VREF_1	C15		
1	IO_L78N_1	D15	NC	
1	IO_L78P_1	E15	NC	
1	IO_L76N_1	F15	NC	
1	IO_L76P_1	G15	NC	
1	IO_L75N_1/VREF_1	G16	NC	
1	IO_L75P_1	F16	NC	
1	IO_L73N_1	A16	NC	
1	IO_L73P_1	A17	NC	
1	IO_L72N_1	B16		
1	IO_L72P_1	C16		
1	IO_L70N_1	D16		
1	IO_L70P_1	E16		
1	IO_L69N_1/VREF_1	C17		
1	IO_L69P_1	D17		
1	IO_L67N_1	H16		
1	IO_L67P_1	G17		
1	IO_L54N_1	E17		
1	IO_L54P_1	F17		
1	IO_L52N_1	A18		
1	IO_L52P_1	A19		
1	IO_L51N_1/VREF_1	E18		
1	IO_L51P_1	D18		
1	IO_L49N_1	B18		
1	IO_L49P_1	C18		
1	IO_L27N_1/VREF_1	F19	NC	NC
1	IO_L27P_1	F18	NC	NC
1	IO_L25N_1	G18	NC	NC
1	IO_L25P_1	G19	NC	NC
1	IO_L24N_1	B19		
1	IO_L24P_1	C19		
1	IO_L22N_1	D19		
1	IO_L22P_1	E19		
1	IO_L21N_1/VREF_1	A20		
1	IO_L21P_1	A21		

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
2	IO_L01P_2	D23		
2	IO_L02N_2/VRP_2	E21		
2	IO_L02P_2/VRN_2	E22		
2	IO_L03N_2	F21		
2	IO_L03P_2/VREF_2	F20		
2	IO_L04N_2	G20		
2	IO_L04P_2	G19		
2	IO_L06N_2	H18		
2	IO_L06P_2	J17		
2	IO_L19N_2	D24		
2	IO_L19P_2	E23		
2	IO_L21N_2	E24		
2	IO_L21P_2/VREF_2	F24		
2	IO_L22N_2	F23		
2	IO_L22P_2	G23		
2	IO_L24N_2	G21		
2	IO_L24P_2	G22		
2	IO_L43N_2	H19		
2	IO_L43P_2	H20		
2	IO_L45N_2	J18		
2	IO_L45P_2/VREF_2	J19		
2	IO_L46N_2	K17		
2	IO_L46P_2	K18		
2	IO_L48N_2	H23		
2	IO_L48P_2	H24		
2	IO_L49N_2	H21		
2	IO_L49P_2	H22		
2	IO_L51N_2	J24		
2	IO_L51P_2/VREF_2	K24		
2	IO_L52N_2	J22		
2	IO_L52P_2	J23		
2	IO_L54N_2	J20		
2	IO_L54P_2	J21		
2	IO_L67N_2	K19	NC	
2	IO_L67P_2	K20	NC	
2	IO_L69N_2	L17	NC	

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
6	IO_L06N_6	V6		
6	IO_L19P_6	U7		
6	IO_L19N_6	T8		
6	IO_L21P_6	AA1		
6	IO_L21N_6/VREF_6	Y2		
6	IO_L22P_6	Y1		
6	IO_L22N_6	W1		
6	IO_L24P_6	W2		
6	IO_L24N_6	V2		
6	IO_L43P_6	V4		
6	IO_L43N_6	V3		
6	IO_L45P_6	U6		
6	IO_L45N_6/VREF_6	U5		
6	IO_L46P_6	T7		
6	IO_L46N_6	T6		
6	IO_L48P_6	R8		
6	IO_L48N_6	R7		
6	IO_L49P_6	U2		
6	IO_L49N_6	U1		
6	IO_L51P_6	U4		
6	IO_L51N_6/VREF_6	U3		
6	IO_L52P_6	T1		
6	IO_L52N_6	R1		
6	IO_L54P_6	T3		
6	IO_L54N_6	T2		
6	IO_L67P_6	T5	NC	
6	IO_L67N_6	T4	NC	
6	IO_L69P_6	R6	NC	
6	IO_L69N_6/VREF_6	R5	NC	
6	IO_L70P_6	P8	NC	
6	IO_L70N_6	P7	NC	
6	IO_L72P_6	R2	NC	
6	IO_L72N_6	P1	NC	
6	IO_L73P_6	R3	NC	NC
6	IO_L73N_6	P3	NC	NC
6	IO_L91P_6	P5		

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
4	IO_L94P_4	AE14
4	IO_L95N_4/GCLK3S	AF15
4	IO_L95P_4/GCLK2P	AG15
4	IO_L96N_4/GCLK1S	Y14
4	IO_L96P_4/GCLK0P	AA14
5	IO_L96N_5/GCLK7S	AC14
5	IO_L96P_5/GCLK6P	AB14
5	IO_L95N_5/GCLK5S	AG13
5	IO_L95P_5/GCLK4P	AF13
5	IO_L94N_5	AE13
5	IO_L94P_5/VREF_5	AD13
5	IO_L93N_5	AC13
5	IO_L93P_5	AB13
5	IO_L92N_5	AA13
5	IO_L92P_5	Y13
5	IO_L91N_5	W13
5	IO_L91P_5/VREF_5	W12
5	IO_L78N_5	AG12
5	IO_L78P_5	AF12
5	IO_L76N_5	AD12
5	IO_L76P_5	AC12
5	IO_L75N_5/VREF_5	AB12
5	IO_L75P_5	AB11
5	IO_L73N_5	Y12
5	IO_L73P_5	Y11
5	IO_L72N_5	AG11
5	IO_L72P_5	AF11
5	IO_L70N_5	AE11
5	IO_L70P_5	AD11
5	IO_L69N_5/VREF_5	AA10
5	IO_L69P_5	AA11
5	IO_L67N_5	AG10
5	IO_L67P_5	AF10
5	IO_L54N_5	AE10
5	IO_L54P_5	AD10

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
7	IO_L27P_7/VREF_7	H5
7	IO_L27N_7	H6
7	IO_L25P_7	J7
7	IO_L25N_7	J8
7	IO_L24P_7	G1
7	IO_L24N_7	F1
7	IO_L22P_7	G2
7	IO_L22N_7	G3
7	IO_L21P_7/VREF_7	F2
7	IO_L21N_7	F3
7	IO_L19P_7	G5
7	IO_L19N_7	G6
7	IO_L06P_7	F4
7	IO_L06N_7	F5
7	IO_L04P_7	E1
7	IO_L04N_7	E2
7	IO_L03P_7/VREF_7	D1
7	IO_L03N_7	C1
7	IO_L02P_7/VRN_7	E3
7	IO_L02N_7/VRP_7	E4
7	IO_L01P_7	D2
7	IO_L01N_7	D3
0	VCCO_0	K13
0	VCCO_0	K12
0	VCCO_0	K11
0	VCCO_0	J11
0	VCCO_0	J10
0	VCCO_0	G12
0	VCCO_0	D7
0	VCCO_0	C12
1	VCCO_1	K17
1	VCCO_1	K16
1	VCCO_1	K15
1	VCCO_1	J18
1	VCCO_1	J17

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
1	VCCO_1	G16
1	VCCO_1	D21
1	VCCO_1	C16
2	VCCO_2	N18
2	VCCO_2	M25
2	VCCO_2	M21
2	VCCO_2	M18
2	VCCO_2	L19
2	VCCO_2	L18
2	VCCO_2	K19
2	VCCO_2	G24
3	VCCO_3	AA24
3	VCCO_3	V19
3	VCCO_3	U19
3	VCCO_3	U18
3	VCCO_3	T25
3	VCCO_3	T21
3	VCCO_3	T18
3	VCCO_3	R18
4	VCCO_4	AE16
4	VCCO_4	AD21
4	VCCO_4	AA16
4	VCCO_4	W18
4	VCCO_4	W17
4	VCCO_4	V17
4	VCCO_4	V16
4	VCCO_4	V15
5	VCCO_5	AE12
5	VCCO_5	AD7
5	VCCO_5	AA12
5	VCCO_5	W11
5	VCCO_5	W10
5	VCCO_5	V13
5	VCCO_5	V12
5	VCCO_5	V11
6	VCCO_6	AA4

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
NA	GND	T12
NA	GND	R16
NA	GND	R15
NA	GND	R14
NA	GND	R13
NA	GND	R12
NA	GND	P27
NA	GND	P24
NA	GND	P19
NA	GND	P16
NA	GND	P15
NA	GND	P14
NA	GND	P13
NA	GND	P12
NA	GND	P9
NA	GND	P4
NA	GND	P1
NA	GND	N16
NA	GND	N15
NA	GND	N14
NA	GND	N13
NA	GND	N12
NA	GND	M16
NA	GND	M15
NA	GND	M14
NA	GND	M13
NA	GND	M12
NA	GND	L23
NA	GND	L5
NA	GND	J14
NA	GND	H26
NA	GND	H20
NA	GND	H8
NA	GND	H2
NA	GND	G21
NA	GND	G7

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
7	IO_L95N_7	R24		
7	IO_L94P_7	R29		
7	IO_L94N_7	T29		
7	IO_L93P_7/VREF_7	R27		
7	IO_L93N_7	P27		
7	IO_L92P_7	R23		
7	IO_L92N_7	P23		
7	IO_L91P_7	N30		
7	IO_L91N_7	P30		
7	IO_L78P_7	P26	NC	NC
7	IO_L78N_7	R26	NC	NC
7	IO_L77P_7	R22	NC	NC
7	IO_L77N_7	P22	NC	NC
7	IO_L76P_7	N29	NC	NC
7	IO_L76N_7	P29	NC	NC
7	IO_L75P_7/VREF_7	N27	NC	NC
7	IO_L75N_7	N26	NC	NC
7	IO_L74P_7	P25	NC	NC
7	IO_L74N_7	N25	NC	NC
7	IO_L73P_7	L30	NC	NC
7	IO_L73N_7	M30	NC	NC
7	IO_L72P_7	L28	NC	
7	IO_L72N_7	M28	NC	
7	IO_L71P_7	N24	NC	
7	IO_L71N_7	M24	NC	
7	IO_L70P_7	L29	NC	
7	IO_L70N_7	M29	NC	
7	IO_L69P_7/VREF_7	M27	NC	
7	IO_L69N_7	L27	NC	
7	IO_L68P_7	N23	NC	
7	IO_L68N_7	M23	NC	
7	IO_L67P_7	J30	NC	
7	IO_L67N_7	K30	NC	
7	IO_L54P_7	K26		
7	IO_L54N_7	L26		
7	IO_L53P_7	M25		
7	IO_L53N_7	L25		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
NA	VBATT	A2		
NA	RSVD	E6		
NA	VCCAUX	AK28		
NA	VCCAUX	AK16		
NA	VCCAUX	AK3		
NA	VCCAUX	T1		
NA	VCCAUX	R30		
NA	VCCAUX	A28		
NA	VCCAUX	A15		
NA	VCCAUX	A3		
NA	VCCINT	AB22		
NA	VCCINT	AB9		
NA	VCCINT	AA21		
NA	VCCINT	AA10		
NA	VCCINT	Y20		
NA	VCCINT	Y19		
NA	VCCINT	Y18		
NA	VCCINT	Y17		
NA	VCCINT	Y16		
NA	VCCINT	Y15		
NA	VCCINT	Y14		
NA	VCCINT	Y13		
NA	VCCINT	Y12		
NA	VCCINT	Y11		
NA	VCCINT	W20		
NA	VCCINT	W11		
NA	VCCINT	V20		
NA	VCCINT	V11		
NA	VCCINT	U20		
NA	VCCINT	U11		
NA	VCCINT	T20		
NA	VCCINT	T11		
NA	VCCINT	R20		
NA	VCCINT	R11		
NA	VCCINT	P20		
NA	VCCINT	P11		

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
2	IO_L21N_2	H7	
2	IO_L21P_2/VREF_2	J7	
2	IO_L22N_2	H6	
2	IO_L22P_2	G6	
2	IO_L23N_2	L10	
2	IO_L23P_2	L9	
2	IO_L24N_2	G3	
2	IO_L24P_2	F3	
2	IO_L25N_2	G2	
2	IO_L25P_2	F2	
2	IO_L26N_2	M10	
2	IO_L26P_2	N10	
2	IO_L27N_2	J6	
2	IO_L27P_2/VREF_2	K6	
2	IO_L28N_2	J5	
2	IO_L28P_2	H5	
2	IO_L29N_2	L7	
2	IO_L29P_2	K7	
2	IO_L30N_2	J4	
2	IO_L30P_2	H4	
2	IO_L43N_2	G1	
2	IO_L43P_2	F1	
2	IO_L44N_2	L8	
2	IO_L44P_2	M8	
2	IO_L45N_2	J1	
2	IO_L45P_2/VREF_2	H2	
2	IO_L46N_2	J3	
2	IO_L46P_2	H3	
2	IO_L47N_2	M9	
2	IO_L47P_2	N9	
2	IO_L48N_2	L5	
2	IO_L48P_2	K5	
2	IO_L49N_2	K2	
2	IO_L49P_2	J2	
2	IO_L50N_2	N7	
2	IO_L50P_2	M7	

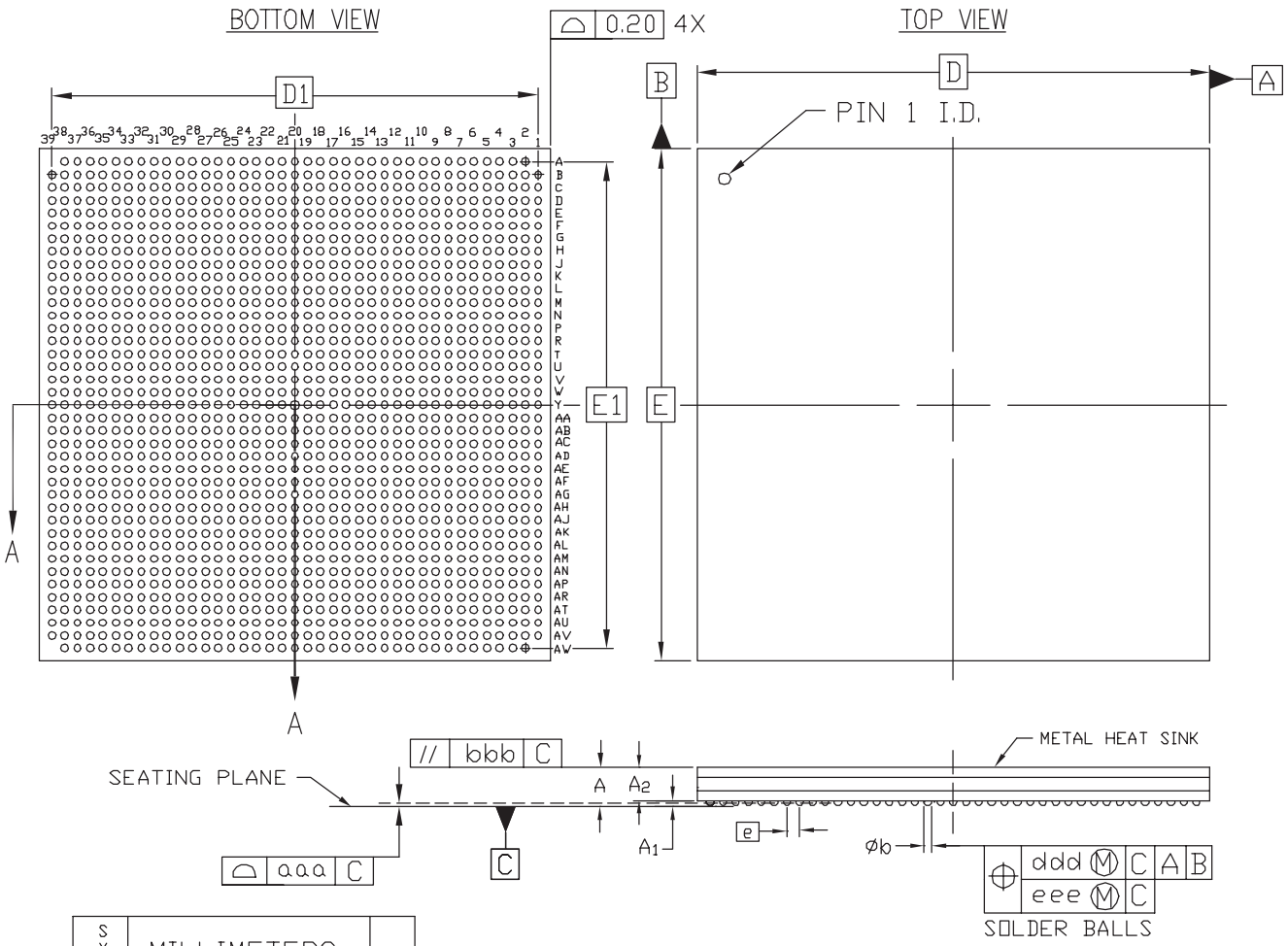
Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
1	IO_L93N_1	E19		
1	IO_L93P_1	E20		
1	IO_L92N_1	J19		
1	IO_L92P_1	J18		
1	IO_L91N_1	A18		
1	IO_L91P_1/VREF_1	A19		
1	IO_L84N_1	D18		
1	IO_L84P_1	D19		
1	IO_L83N_1	K19		
1	IO_L83P_1	K18		
1	IO_L82N_1	B18		
1	IO_L82P_1	B19		
1	IO_L81N_1/VREF_1	G18		
1	IO_L81P_1	G19		
1	IO_L80N_1	E18		
1	IO_L80P_1	E17		
1	IO_L79N_1	A16		
1	IO_L79P_1	A17		
1	IO_L78N_1	F17		
1	IO_L78P_1	F18		
1	IO_L77N_1	L19		
1	IO_L77P_1	L18		
1	IO_L76N_1	B16		
1	IO_L76P_1	B17		
1	IO_L75N_1/VREF_1	G16		
1	IO_L75P_1	G17		
1	IO_L74N_1	M19		
1	IO_L74P_1	M18		
1	IO_L73N_1	C16		
1	IO_L73P_1	C17		
1	IO_L72N_1	D15		
1	IO_L72P_1	D16		
1	IO_L71N_1	J17		
1	IO_L71P_1	J16		
1	IO_L70N_1	A14		
1	IO_L70P_1	A15		

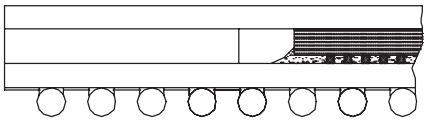
Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
2	IO_L57P_2/VREF_2	P7		
2	IO_L58N_2	R3		
2	IO_L58P_2	P3		
2	IO_L59N_2	T10		
2	IO_L59P_2	U10		
2	IO_L60N_2	P4		
2	IO_L60P_2	N4		
2	IO_L67N_2	T6		
2	IO_L67P_2	R6		
2	IO_L68N_2	T9		
2	IO_L68P_2	U9		
2	IO_L69N_2	T5		
2	IO_L69P_2/VREF_2	R5		
2	IO_L70N_2	R1		
2	IO_L70P_2	P1		
2	IO_L71N_2	V12		
2	IO_L71P_2	W12		
2	IO_L72N_2	T4		
2	IO_L72P_2	R4		
2	IO_L73N_2	T2		
2	IO_L73P_2	R2		
2	IO_L74N_2	V11		
2	IO_L74P_2	W11		
2	IO_L75N_2	U7		
2	IO_L75P_2/VREF_2	T7		
2	IO_L76N_2	U3		
2	IO_L76P_2	T3		
2	IO_L77N_2	V10		
2	IO_L77P_2	W10		
2	IO_L78N_2	V6		
2	IO_L78P_2	U6		
2	IO_L79N_2	U1		
2	IO_L79P_2	T1		
2	IO_L80N_2	V9		
2	IO_L80P_2	W9		
2	IO_L81N_2	V5		

FF1517 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A		3.20	3.40	
A_1	0.40	0.50	0.60	
A_2			2.80	
D/E	40.00 BASIC			
D_1/E_1	38.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
bbb			0.25	
ddd			0.25	
eee			0.10	
M		39		2



SECTION A–A
(NOT TO SCALE)

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAU–1 (DEPOPULATED)

Figure 9: **FF1517 Flip-Chip Fine-Pitch BGA Package Specifications**