AMD Xilinx - XC2V6000-5FFG1517I Datasheet

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	8448
Number of Logic Elements/Cells	-
Total RAM Bits	2654208
Number of I/O	1104
Number of Gates	6000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FCBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v6000-5ffg1517i

Boundary Scan

Boundary scan instructions and associated data registers support a standard methodology for accessing and configuring Virtex-II devices that complies with IEEE standards 1149.1 — 1993 and 1532. A system mode and a test mode are implemented. In system mode, a Virtex-II device performs its intended mission even while executing non-test boundary-scan instructions. In test mode, boundary-scan test instructions control the I/O pins for testing purposes. The Virtex-II Test Access Port (TAP) supports BYPASS, PRELOAD, SAMPLE, IDCODE, and USERCODE non-test instructions. The EXTEST, INTEST, and HIGHZ test instructions are also supported.

Configuration

Virtex-II devices are configured by loading data into internal configuration memory, using the following five modes:

- Slave-serial mode
- Master-serial mode
- Slave SelectMAP mode
- Master SelectMAP mode
- Boundary-Scan mode (IEEE 1532)

A Data Encryption Standard (DES) decryptor is available on-chip to secure the bitstreams. One or two triple-DES key sets can be used to optionally encrypt the configuration information.

Readback and Integrated Logic Analyzer

Configuration data stored in Virtex-II configuration memory can be read back for verification. Along with the configuration data, the contents of all flip-flops/latches, distributed SelectRAM, and block SelectRAM memory resources can be read back. This capability is useful for real-time debugging.

The Integrated Logic Analyzer (ILA) core and software provides a complete solution for accessing and verifying Virtex-II devices.

Virtex-II Device/Package Combinations and Maximum I/O

Wire-bond and flip-chip packages are available. Table 4 and Table 5 show the maximum possible number of user I/Os in wire-bond and flip-chip packages, respectively. Table 6 shows the number of available user I/Os for all device/package combinations.

- CS denotes wire-bond chip-scale ball grid array (BGA) (0.80 mm pitch).
- CSG denotes Pb-free wire-bond chip-scale ball grid array (BGA) (0.80 mm pitch).
- FG denotes wire-bond fine-pitch BGA (1.00 mm pitch).
- FGG denotes Pb-free wire-bond fine-pitch BGA (1.00 mm pitch).
- BG denotes standard BGA (1.27 mm pitch).
- BGG denotes Pb-free standard BGA (1.27 mm pitch).
- FF denotes flip-chip fine-pitch BGA (1.00 mm pitch).
- BF denotes flip-chip BGA (1.27 mm pitch).

The number of I/Os per package include all user I/Os except the 15 control pins (CCLK, DONE, M0, M1, M2, PROG_B, PWRDWN_B, TCK, TDI, TDO, TMS, HSWAP_EN, DXN, DXP, and RSVD) and VBATT.

Table 4: **Wire-Bond Packages Information**

Package[1]	CS144/ CSG144	FG256/ FGG256	FG456/ FGG456	FG676/ FGG676	BG575/ BGG575	BG728/ BGG728
Pitch (mm)	0.80	1.00	1.00	1.00	1.27	1.27
Size (mm)	12 x 12	17 x 17	23 x 23	27 x 27	31 x 31	35 x 35
I/Os	92	172	324	484	408	516

Notes:
1. Wire-bond packages include FGG*nnn* Pb-free versions. See Virtex-II Ordering Examples (Module 1).

Table 5: **Flip-Chip Packages Information**

Package	FF896	FF1152	FF1517	BF957
Pitch (mm)	1.00	1.00	1.00	1.27
Size (mm)	31 x 31	35 x 35	40 x 40	40 x 40
I/Os	624	824	1,108	684

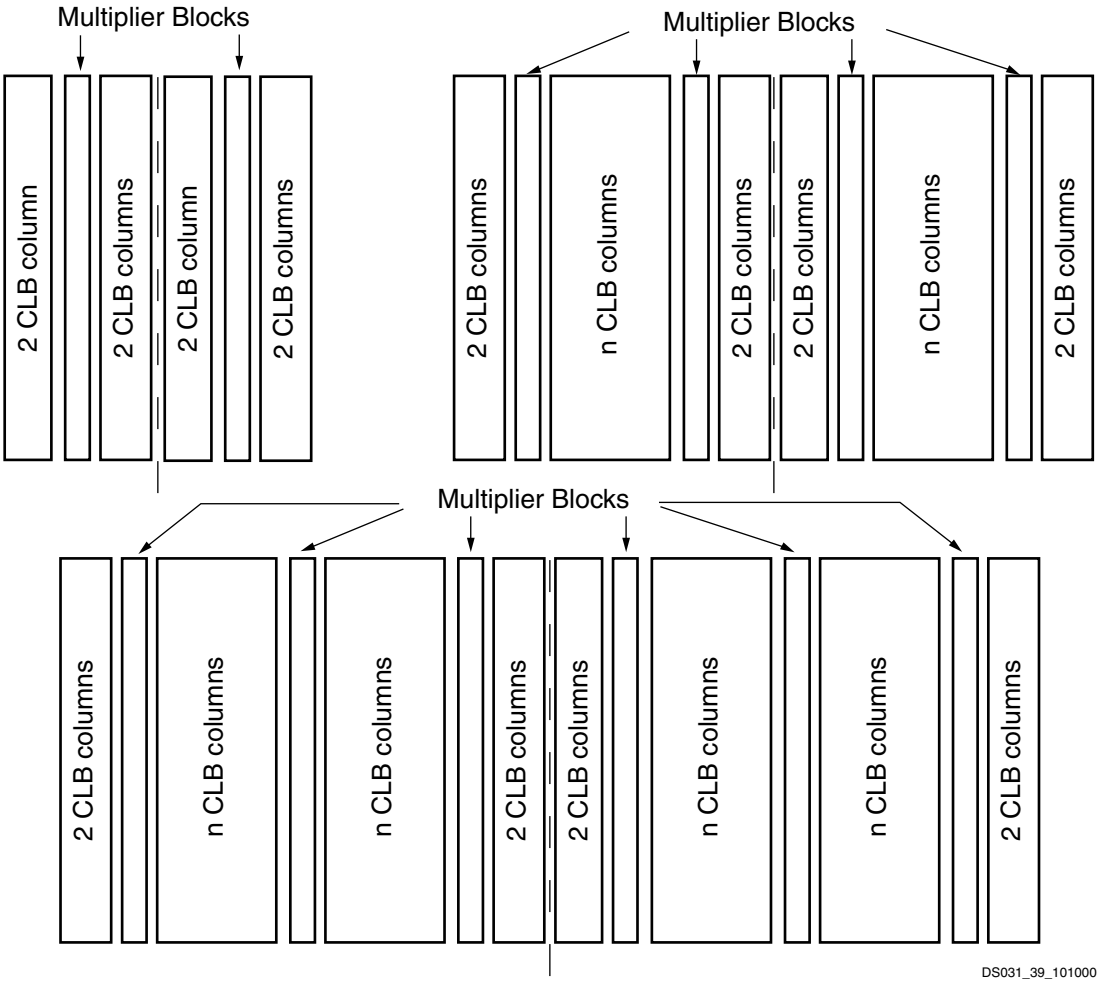


Figure 37: **Multipliers (2-column, 4-column, and 6-column)**

Global Clock Multiplexer Buffers

Virtex-II devices have 16 clock input pins that can also be used as regular user I/Os. Eight clock pads are on the top edge of the device, in the middle of the array, and eight are on the bottom edge, as illustrated in Figure 38.

The global clock multiplexer buffer represents the input to dedicated low-skew clock tree distribution in Virtex-II devices. Like the clock pads, eight global clock multiplexer buffers are on the top edge of the device and eight are on the bottom edge.

Each global clock buffer can either be driven by the clock pad to distribute a clock directly to the device, or driven by the Digital Clock Manager (DCM), discussed in Digital Clock Manager (DCM), page 29. Each global clock buffer can also be driven by local interconnects. The DCM has clock output(s) that can be connected to global clock buffer inputs, as shown in Figure 39.

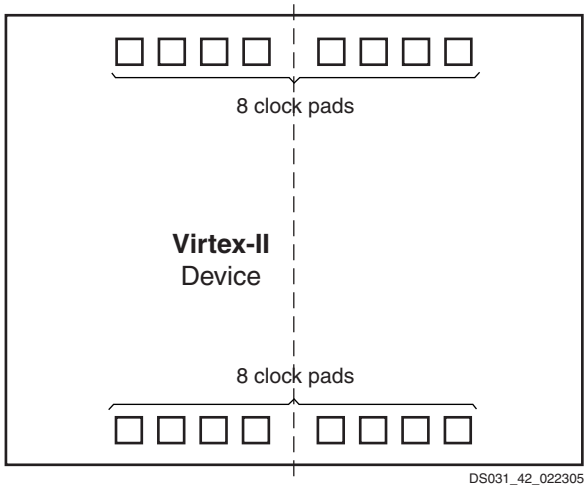


Figure 38: **Virtex-II Clock Pads**

ments to begin changing state in response to the logic and the user clock.

The relative timing of these events can be changed via configuration options in software. In addition, the GTS and GWE events can be made dependent on the DONE pins of multiple devices all going High, forcing the devices to start synchronously. The sequence can also be paused at any stage, until lock has been achieved on any or all DCMs, as well as the DCI.

Readback

In this mode, configuration data from the Virtex-II FPGA device can be read back. Readback is supported only in the SelectMAP (master and slave) and Boundary-Scan mode.

Along with the configuration data, it is possible to read back the contents of all registers, distributed SelectRAM, and block RAM resources. This capability is used for real-time debugging. For more detailed configuration information, see the Virtex-II *Platform FPGA User Guide.*

Bitstream Encryption

Virtex-II devices have an on-chip decryptor using one or two sets of three keys for triple-key Data Encryption Standard (DES) operation. Xilinx software tools offer an optional encryption of the configuration data (bitstream) with a triple-key DES determined by the designer.

The keys are stored in the FPGA by JTAG instruction and retained by a battery connected to the V_{BATT} pin, when the device is not powered. Virtex-II devices can be configured with the corresponding encrypted bitstream, using any of the configuration modes described previously.

A detailed description of how to use bitstream encryption is provided in the *Virtex-II Platform FPGA User Guide*. For devices that support this feature, please contact your sales representative for specific ordering part number.

Partial Reconfiguration

Partial reconfiguration of Virtex-II devices can be accomplished in either Slave SelectMAP mode or Boundary-Scan mode. Instead of resetting the chip and doing a full configuration, new data is loaded into a specified area of the chip, while the rest of the chip remains in operation. Data is loaded on a column basis, with the smallest load unit being a configuration “frame” of the bitstream (device size dependent).

Partial reconfiguration is useful for applications that require different designs to be loaded into the same area of a chip, or that require the ability to change portions of a design without having to reset or reconfigure the entire chip.

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
11/07/00	1.0	Early access draft.
12/06/00	1.1	Initial release.
01/15/01	1.2	Added values to the tables in the Virtex-II Performance Characteristics and Virtex-II Switching Characteristics sections.
01/25/01	1.3	The data sheet was divided into four modules (per the current style standard). A note was added to Table 1.
04/02/01	1.5	• Under Input/Output Individual Options, the range of values for optional pull-up and pull-down resistors was changed to 10 - 60 KΩ from 50 - 100 KΩ. • Skipped v1.4 to sync up modules. Reverted to traditional double-column format.
07/30/01	1.6	• Added Table 6. • Changed definition of multiply and divide integer ranges under Digital Clock Manager (DCM). • Made numerous minor edits throughout this module.
10/02/01	1.7	• Updated descriptions under Digitally Controlled Impedance (DCI), Global Clock Multiplexer Buffers, Digital Clock Manager (DCM), and Creating a Design.
10/12/01	1.8	• Made clarifying edits under Digital Clock Manager (DCM).
11/29/01	1.9	• Changed bitstream lengths for each device in Table 26.

Table 12: **Register-to-Register Performance *(Continued)***

Description	Device Used & Speed Grade	Register-to-Register Performance	Units
8-bit Adder	XC2V1000 -5	292	MHz
16-bit Adder	XC2V1000 -5	239	MHz
64-bit Adder	XC2V1000 -5	114	MHz
64-bit Counter	XC2V1000 -5	114	MHz
64-bit Accumulator	XC2V1000 -5	110	MHz
Multiplier 18x18 (with Block RAM inputs)	XC2V1000 -5	88	MHz
Multiplier 18x18 (with Register inputs)	XC2V1000 -5	105	MHz
Memory			
Block RAM			
Single-Port 4096 x 4 bits		278	MHz
Single-Port 2048 x 9 bits		277	MHz
Single-Port 1024 x 18 bits		270	MHz
Single-Port 512 x 36 bits		253	MHz
Dual-Port A:4096 x 4 bits & B:1024 x 18 bits		257	MHz
Dual-Port A:1024 x 18 bits & B:1024 x 18 bits		259	MHz
Dual-Port A:2048 x 9 bits & B: 512 x 36 bits		250	MHz
Distributed RAM			
Single-Port 32 x 8-bit	XC2V1000 -5	387	MHz
Single-Port 64 x 8-bit	XC2V1000 -5	335	MHz
Single-Port 128 x 8-bit	XC2V1000 -5	266	MHz
Dual-Port 16 x 8	XC2V1000 -5	409	MHz
Dual-Port 32 x 8	XC2V1000 -5	311	MHz
Dual-Port 64 x 8	XC2V1000 -5	294	MHz
Shift Registers			
128-bit SRL		N/A	MHz
256-bit SRL		N/A	MHz
FIFOs (Async. in Block RAM)			
1024 x 18-bit Read		279	MHz
1024 x 18-bit Write		172	MHz
FIFOs (Sync. in SRL)			
128 x 8-bit		N/A	MHz
128 x 16-bit		N/A	MHz

Table 14: **IOB Input Switching Characteristics *(Continued)***

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
Propagation Delays						
Pad to output IQ via transparent latch, no delay	T_{IOPLI}	All	0.83	0.91	1.05	ns, Max
Pad to output IQ via transparent latch, with delay	T_{IOPLID}	XC2V40	3.23	3.55	4.09	ns, Max
		XC2V80	3.23	3.55	4.09	ns, Max
		XC2V250	3.23	3.55	4.09	ns, Max
		XC2V500	3.23	3.55	4.09	ns, Max
		XC2V1000	3.23	3.55	4.09	ns, Max
		XC2V1500	3.23	3.55	4.09	ns, Max
		XC2V2000	3.23	3.55	4.09	ns, Max
		XC2V3000	3.32	3.65	4.20	ns, Max
		XC2V4000	3.32	3.65	4.20	ns, Max
		XC2V6000	3.60	3.95	4.55	ns, Max
		XC2V8000		3.95	4.55	ns, Max
Clock CLK to output IQ	T_{IOCKIQ}	All		0.67	0.77	ns, Max
Setup and Hold Times With Respect to Clock at IOB Input Register						
Pad, no delay	T_{IOPICK}/T_{IOICKP}	All	0.84/–0.36	0.92/–0.39	1.06/–0.45	ns, Min
Pad, with delay	$T_{IOPICKD}/T_{IOICKPD}$	XC2V40	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V80	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V250	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V500	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V1000	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V1500	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V2000	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V3000	3.33/–2.10	3.67/–2.31	4.22/–2.66	ns, Min
		XC2V4000	3.33/–2.10	3.67/–2.31	4.22/–2.66	ns, Min
		XC2V6000	3.61/–2.29	3.97/–2.52	4.56/–2.90	ns, Min
		XC2V8000		3.97/–2.52	4.56/–2.90	ns, Min
ICE input	$T_{IOICECK}/T_{IOCKICE}$	All		0.21/ 0.04	0.24/ 0.04	ns, Min
SR input (IFF, synchronous)	$T_{IOSRCKI}$	All	0.27	0.30	0.34	ns, Min
Set/Reset Delays						
SR input to IQ (asynchronous)	T_{IOSRIQ}	All	1.11	1.22	1.40	ns, Max
GSR to output IQ	T_{GSRQ}	All	5.44	5.98	6.88	ns, Max

Notes:
1. Input timing for LVTTL is measured at 1.4 V. For other I/O standards, see Table 18.

Table 17: **IOB Output Switching Characteristics Standard Adjustments *(Continued)***

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-6	-5	-4	
HSTL, Class II, 1.8V	HSTL_II_18	$T_{OHSTL\_II\_18}$	–0.17	–0.18	–0.20	ns
HSTL, Class III, 1.8V	HSTL_III_18	$T_{OHSTL\_III\_18}$	–0.16	–0.16	–0.18	ns
HSTL, Class IV, 1.8V	HSTL_IV_18	$T_{OHSTL\_IV\_18}$	–0.39	–0.40	–0.44	ns
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	$T_{OSSTL18\_I}$	0.20	0.20	0.22	ns
SSTL, Class II, 1.8V	SSTL18_II	$T_{OSSTL18\_II}$	–0.05	–0.05	–0.06	ns
SSTL, Class I, 2.5V	SSTL2_I	T_{OSSTL2_I}	0.21	0.22	0.24	ns
SSTL, Class II, 2.5V	SSTL2_II	T_{OSSTL2_II}	–0.15	–0.16	–0.18	ns
SSTL, Class I, 3.3V	SSTL3_I	T_{OSSTL3_I}	0.29	0.30	0.33	ns
SSTL, Class II, 3.3V	SSTL3_II	T_{OSSTL3_II}	–0.05	–0.05	–0.05	ns
AGP-2X/AGP (Accelerated Graphics Port)	AGP	T_{OAGP}	–0.27	–0.28	–0.31	ns
LVDCI (Low-Voltage Digitally Controlled Impedance), 3.3V	LVDCI_33	T_{OLVDCI_33}	0.74	0.77	0.84	ns
LVDCI, 2.5V	LVDCI_25	T_{OLVDCI_25}	0.78	0.80	0.88	ns
LVDCI, 1.8V	LVDCI_18	T_{OLVDCI_18}	0.84	0.87	0.95	ns
LVDCI, 1.5V	LVDCI_15	T_{OLVDCI_15}	1.82	1.88	2.06	ns
LVDCI, 3.3V, Half-Impedance	LVDCI_DV2_33	$T_{OLVDCI\_DV2\_33}$	0.12	0.12	0.13	ns
LVDCI, 2.5V, Half-Impedance	LVDCI_DV2_25	$T_{OLVDCI\_DV2\_25}$	0.03	0.03	0.03	ns
LVDCI, 1.8V, Half-Impedance	LVDCI_DV2_18	$T_{OLVDCI\_DV2\_18}$	0.42	0.43	0.48	ns
LVDCI, 1.5V, Half-Impedance	LVDCI_DV2_15	$T_{OLVDCI\_DV2\_15}$	1.20	1.23	1.36	ns
HSLVDCI (High-Speed Low-Voltage DCI), 1.5V	HSLVDCI_15	$T_{OHSLVDCI\_15}$	1.82	1.88	2.06	ns
HSLVDCI, 1.8V	HSLVDCI_18	$T_{OHSLVDCI\_18}$	1.05	1.08	1.24	ns
HSLVDCI, 2.5V	HSLVDCI_25	$T_{OHSLVDCI\_25}$	0.78	0.80	0.88	ns
HSLVDCI, 3.3V	HSLVDCI_33	$T_{OHSLVDCI\_33}$	0.74	0.77	0.84	ns
GTL (Gunning Transceiver Logic) with DCI	GTL_DCI	T_{OGTL_DCI}	–0.31	–0.32	–0.35	ns
GTL Plus with DCI	GTLP_DCI	T_{OGTLP_DCI}	–0.15	–0.16	–0.17	ns
HSTL (High-Speed Transceiver Logic), Class I, with DCI	HSTL_I_DCI	$T_{OHSTL\_I\_DCI}$	0.23	0.23	0.26	ns
HSTL, Class II, with DCI	HSTL_II_DCI	$T_{OHSTL\_II\_DCI}$	0.06	0.06	0.07	ns
HSTL, Class III, with DCI	HSTL_III_DCI	$T_{OHSTL\_III\_DCI}$	–0.17	–0.18	–0.20	ns
HSTL, Class IV, with DCI	HSTL_IV_DCI	$T_{OHSTL\_IV\_DCI}$	–0.46	–0.47	–0.52	ns
HSTL, Class I, 1.8V, with DCI	HSTL_I_DCI_18	$T_{OHSTL\_I\_DCI\_18}$	0.05	0.05	0.06	ns
HSTL, Class II, 1.8V, with DCI	HSTL_II_DCI_18	$T_{OHSTL\_II\_DCI\_18}$	–0.03	–0.03	–0.03	ns
HSTL, Class III, 1.8V, with DCI	HSTL_III_DCI_18	$T_{OHSTL\_III\_DCI\_18}$	–0.14	–0.14	–0.16	ns
HSTL, Class IV, 1.8V, with DCI	HSTL_IV_DCI_18	$T_{OHSTL\_IV\_DCI\_18}$	–0.41	–0.42	–0.47	ns
SSTL (Stub Series Terminated Logic), Class I, 1.8V, with DCI	SSTL18_I_DCI	$T_{OSSTL18\_I\_DCI}$	0.36	0.37	0.40	ns
SSTL, Class II, 1.8V, with DCI	SSTL18_II_DCI	$T_{OSSTL18\_II\_DCI}$	0.06	0.06	0.07	ns
SSTL, Class I, 2.5V, with DCI	SSTL2_I_DCI	$T_{OSSTL2\_I\_DCI}$	0.12	0.13	0.14	ns
SSTL, Class II, 2.5V, with DCI	SSTL2_II_DCI	$T_{OSSTL2\_II\_DCI}$	–0.10	–0.10	–0.11	ns
SSTL, Class I, 3.3V, with DCI	SSTL3_I_DCI	$T_{OSSTL3\_I\_DCI}$	0.15	0.16	0.17	ns
SSTL, Class II, 3.3V, with DCI	SSTL3_II_DCI	$T_{OSSTL3\_II\_DCI}$	0.08	0.08	0.09	ns

Source Synchronous Timing Budgets

This section describes how to use the parameters provided in the Source-Synchronous Switching Characteristics section to develop system-specific timing budgets. The following analysis provides information necessary for determining Virtex-II contributions to an overall system timing analysis; no assumptions are made about the effects of Inter-Symbol Interference or PCB skew.

Virtex-II Transmitter Data-Valid Window (T_X)

T_X is the minimum aggregate valid data period for a source-synchronous data bus at the pins of the device and is calculated as follows:

$$T_X = \text{Data Period} - [\text{Jitter}^{(1)} + \text{Duty Cycle Distortion}^{(2)} + \text{TCKSKEW}^{(3)} + \text{TPKGSKEW}^{(4)}]$$

Notes:

1. Jitter values and accumulation methodology to be provided in a future release of this document. The absolute period jitter values found in the DCM Timing Parameters section of the particular DCM output clock used to clock the IOB FF can be used for a best case analysis.
2. This value depends on the clocking methodology used. See Note1 for Table 45.
3. This value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.
4. These values represent the worst-case skew between any two balls of the package: shortest flight time to longest flight time from Pad to Ball.

Virtex-II Receiver Data-Valid Window (R_X)

R_X is the required minimum aggregate valid data period for a source-synchronous data bus at the pins of the device and is calculated as follows:

$$R_X = [\text{TSAMP}^{(1)} + \text{TCKSKEW}^{(2)} + \text{TPKGSKEW}^{(3)}]$$

Notes:

1. This parameter indicates the total sampling error of Virtex-II DDR input registers across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 and CLK180 DCM jitter in a quiet system
   - Worst-case duty-cycle distortion
   - DCM accuracy (phase offset)
   - DCM phase shift resolution.

   These measurements do not include package or clock tree skew.
2. This value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.
3. These values represent the worst-case skew between any two balls of the package: shortest flight time to longest flight time from Pad to Ball.

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
11/07/00	1.0	Early access draft.
12/06/00	1.1	Initial release.
01/15/01	1.2	Added values to the tables in the Virtex-II Performance Characteristics and Virtex-II Switching Characteristics sections.
01/25/01	1.3	• The data sheet was divided into four modules (per the current style standard). • Updated values in the Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables. • Table 18, "Delay Measurement Methodology"
04/23/01	1.5	• Updated values in the Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables. • Added T_{REG32} symbol to Table 23. • Skipped v1.4 to sync with other modules. Reverted to traditional double-column format.

Table 3: **Virtex-II Device/Package Combinations and Maximum Number of Available I/Os**

Package	Available I/Os										
	XC2V 40	XC2V 80	XC2V 250	XC2V 500	XC2V 1000	XC2V 1500	XC2V 2000	XC2V 3000	XC2V 4000	XC2V 6000	XC2V 8000
CS144	88	92	92	-	-	-	-	-	-	-	-
FG256	88	120	172	172	172	-	-	-	-	-	-
FG456	-	-	200	264	324	-	-	-	-	-	-
FG676	-	-	-	-	-	392	456	484	-	-	-
FF896	-	-	-	-	432	528	624	-	-	-	-
FF1152	-	-	-	-	-	-	-	720	824	824	824
FF1517	-	-	-	-	-	-	-	-	912	1,104	1,108
BG575	-	-	-	-	328	392	408	-	-	-	-
BG728	-	-	-	-	-	-	-	516	-	-	-
BF957	-	-	-	-	-	-	624	684	684	684	-

Virtex-II Pin Definitions

This section describes the pinouts for Virtex-II devices in the following packages:

- CS144: wire-bond chip-scale ball grid array (BGA) of 0.80 mm pitch
- FG256, FG456, and FG676: wire-bond fine-pitch BGA of 1.00 mm pitch
- FF896, FF1152, FF1517: flip-chip fine-pitch BGA of 1.00 mm pitch
- BG575 and BG728: wire-bond BGA of 1.27 mm pitch
- BF957: flip-chip BGA of 1.27 mm pitch

All of the devices supported in a particular package are pinout compatible and are listed in the same table (one table per package). In addition, the FG456 and FG676 packages are compatible, as are the FF896 and FF1152 packages. Pins that are not available for the smallest devices are listed in right-hand columns.

Each device is split into eight I/O banks to allow for flexibility in the choice of I/O standards (see the Virtex-II *Data Sheet*). Global pins, including JTAG, configuration, and power/ground pins, are listed at the end of each table. Table 4 provides definitions for all pin types.

The FG256 pinouts (Table 6) is included as an example. All Virtex-II pinout tables are available on the distribution CD-ROM, or on the web (at **http://www.xilinx.com**).

Table 5: **CS144/CSG144 — XC2V40, XC2V80, and XC2V250**

Bank	Pin Description	Pin Number	No Connect in the XC2V40
6	IO_L01P_6	L3	
6	IO_L01N_6	L2	
6	IO_L02P_6/VRN_6	L1	
6	IO_L02N_6/VRP_6	K3	
6	IO_L03P_6	K2	
6	IO_L03N_6/VREF_6	K1	
6	IO_L94P_6	J2	
6	IO_L94N_6	H4	
6	IO_L96P_6	H3	
6	IO_L96N_6	H1	
7	IO_L96P_7	G4	
7	IO_L96N_7	G3	
7	IO_L94P_7	G1	
7	IO_L94N_7	F1	
7	IO_L93P_7/VREF_7	F2	NC
7	IO_L93N_7	F4	NC
7	IO_L03P_7/VREF_7	E2	
7	IO_L03N_7	E3	
7	IO_L02P_7/VRN_7	E4	
7	IO_L02N_7/VRP_7	D1	
7	IO_L01P_7	D2	
7	IO_L01N_7	D3	
0	VCCO_0	B5	
0	VCCO_0	C3	
1	VCCO_1	A11	
1	VCCO_1	A9	
2	VCCO_2	F10	
2	VCCO_2	C12	
3	VCCO_3	L12	
3	VCCO_3	J12	
4	VCCO_4	M9	
4	VCCO_4	L11	
5	VCCO_5	N3	
5	VCCO_5	N5	
6	VCCO_6	J3	
6	VCCO_6	M1	
7	VCCO_7	D4	
7	VCCO_7	F3	

Table 6: **FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
4	IO_L91N_4/VREF_4	R11	NC	NC
4	IO_L91P_4	T11	NC	NC
4	IO_L92N_4	M11	NC	NC
4	IO_L92P_4	M10	NC	NC
4	IO_L93N_4	N10	NC	NC
4	IO_L93P_4	P10	NC	NC
4	IO_L94N_4/VREF_4	R10		
4	IO_L94P_4	T10		
4	IO_L95N_4/GCLK3S	N9		
4	IO_L95P_4/GCLK2P	P9		
4	IO_L96N_4/GCLK1S	R9		
4	IO_L96P_4/GCLK0P	T9		
5	IO_L96N_5/GCLK7S	T8		
5	IO_L96P_5/GCLK6P	R8		
5	IO_L95N_5/GCLK5S	P8		
5	IO_L95P_5/GCLK4P	N8		
5	IO_L94N_5	T7		
5	IO_L94P_5/VREF_5	R7		
5	IO_L93N_5	P7	NC	NC
5	IO_L93P_5	N7	NC	NC
5	IO_L92N_5	M7	NC	NC
5	IO_L92P_5	M6	NC	NC
5	IO_L91N_5	T6	NC	NC
5	IO_L91P_5/VREF_5	R6	NC	NC
5	IO_L05N_5/VRP_5	P6	NC	NC
5	IO_L05P_5/VRN_5	N6	NC	NC
5	IO_L04N_5	T5	NC	NC
5	IO_L04P_5/VREF_5	R5	NC	NC
5	IO_L03N_5/D4/ALT_VRP_5	P5		
5	IO_L03P_5/D5/ALT_VRN_5	N5		
5	IO_L02N_5/D6	R4		
5	IO_L02P_5/D7	P4		
5	IO_L01N_5/RDWR_B	T4		

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
5	IO_L70N_5	W11		
5	IO_L70P_5	Y10		
5	IO_L69N_5/VREF_5	Y11		
5	IO_L69P_5	AA11		
5	IO_L67N_5	AF9		
5	IO_L67P_5	AF8		
5	IO_L54N_5	AE9		
5	IO_L54P_5	AD9		
5	IO_L52N_5	AB10		
5	IO_L52P_5	AA10		
5	IO_L51N_5/VREF_5	AD10		
5	IO_L51P_5	AC10		
5	IO_L49N_5	AE8		
5	IO_L49P_5	AF7		
5	IO_L28N_5	AD8	NC	NC
5	IO_L28P_5	AC8	NC	NC
5	IO_L27N_5/VREF_5	AB9	NC	NC
5	IO_L27P_5	AC9	NC	NC
5	IO_L25N_5	AA9	NC	NC
5	IO_L25P_5	Y9	NC	NC
5	IO_L24N_5	AF6		
5	IO_L24P_5	AE6		
5	IO_L22N_5	AB8		
5	IO_L22P_5	AA8		
5	IO_L21N_5/VREF_5	AC7		
5	IO_L21P_5	AD7		
5	IO_L19N_5	AF5		
5	IO_L19P_5	AE5		
5	IO_L06N_5	AF4		
5	IO_L06P_5	AE4		
5	IO_L05N_5/VRP_5	AF3		
5	IO_L05P_5/VRN_5	AE3		
5	IO_L04N_5	Y8		
5	IO_L04P_5/VREF_5	Y7		
5	IO_L03N_5/D4/ALT_VRP_5	AB7		
5	IO_L03P_5/D5/ALT_VRN_5	AA7		
5	IO_L02N_5/D6	AD6		

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
1	IO_L70N_1	B15	NC	
1	IO_L70P_1	C15	NC	
1	IO_L69N_1/VREF_1	E15	NC	
1	IO_L69P_1	F15	NC	
1	IO_L67N_1	G15	NC	
1	IO_L67P_1	H15	NC	
1	IO_L54N_1	B16		
1	IO_L54P_1	C16		
1	IO_L52N_1	D16		
1	IO_L52P_1	E16		
1	IO_L51N_1/VREF_1	F16		
1	IO_L51P_1	G16		
1	IO_L49N_1	A17		
1	IO_L49P_1	A19		
1	IO_L24N_1	B17		
1	IO_L24P_1	B18		
1	IO_L22N_1	C17		
1	IO_L22P_1	D17		
1	IO_L21N_1/VREF_1	F17		
1	IO_L21P_1	E17		
1	IO_L19N_1	A20		
1	IO_L19P_1	A21		
1	IO_L06N_1	B19		
1	IO_L06P_1	B20		
1	IO_L05N_1	C18		
1	IO_L05P_1	D18		
1	IO_L04N_1	C20		
1	IO_L04P_1/VREF_1	D20		
1	IO_L03N_1/VRP_1	D19		
1	IO_L03P_1/VRN_1	E19		
1	IO_L02N_1	E18		
1	IO_L02P_1	F18		
1	IO_L01N_1	H16		
1	IO_L01P_1	G17		
2	IO_L01N_2	D22		

BG728/BGG728 Standard BGA Package

As shown in Table 10, XC2V3000 Virtex-II devices are available in the BG728/BGG728 BGA package. Following this table are the BG728/BGG728 Standard BGA Package Specifications (1.27mm pitch).

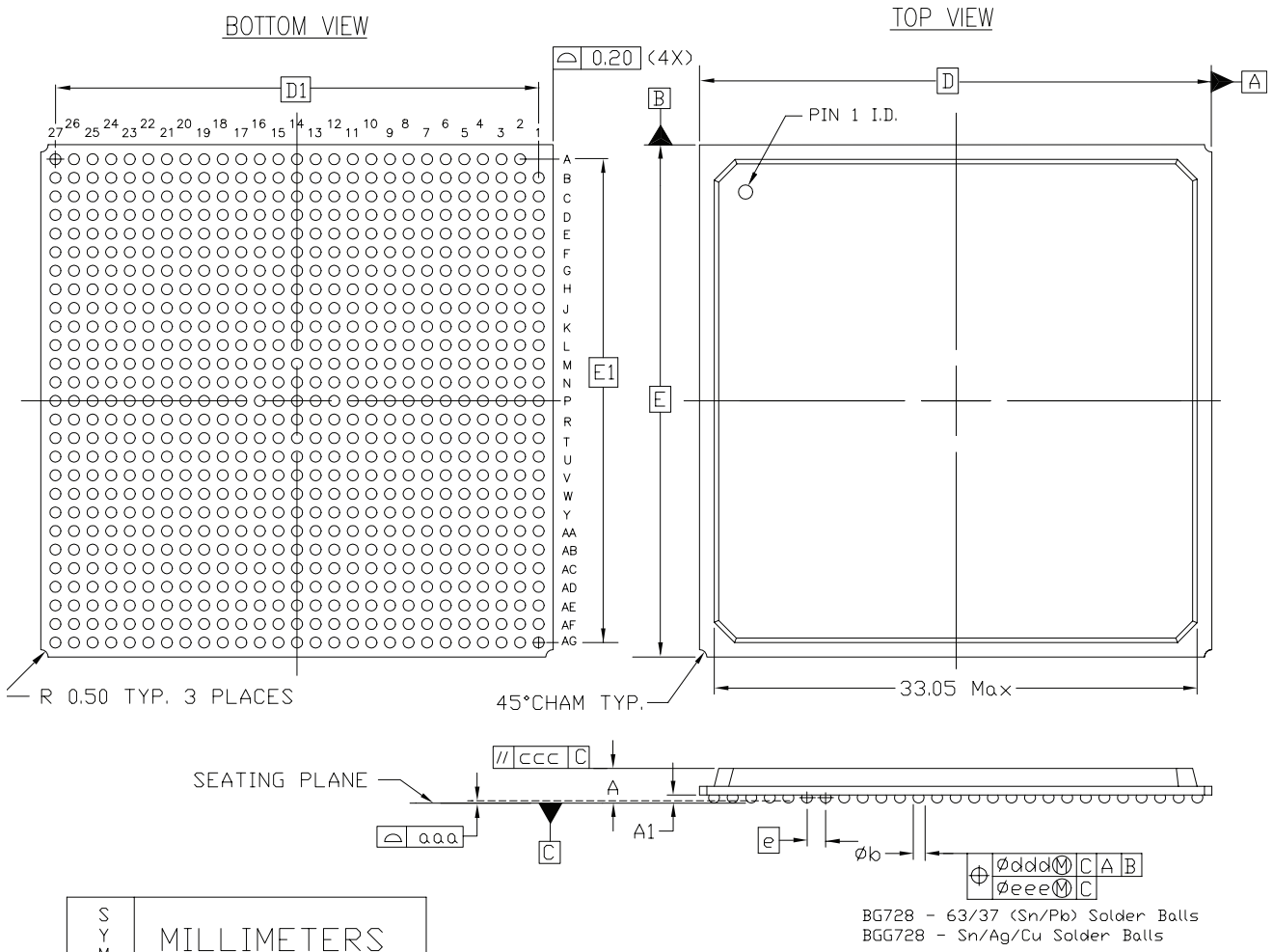
Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
0	IO_L01N_0	B3
0	IO_L01P_0	A3
0	IO_L02N_0	B4
0	IO_L02P_0	A4
0	IO_L03N_0/VRP_0	C5
0	IO_L03P_0/VRN_0	C6
0	IO_L04N_0/VREF_0	B5
0	IO_L04P_0	A5
0	IO_L05N_0	E6
0	IO_L05P_0	D6
0	IO_L06N_0	B6
0	IO_L06P_0	A6
0	IO_L19N_0	E7
0	IO_L19P_0	D8
0	IO_L21N_0	F8
0	IO_L21P_0/VREF_0	E8
0	IO_L22N_0	C7
0	IO_L22P_0	C8
0	IO_L24N_0	B7
0	IO_L24P_0	A7
0	IO_L25N_0	H9
0	IO_L25P_0	J9
0	IO_L27N_0	F9
0	IO_L27P_0/VREF_0	G9
0	IO_L28N_0	E9
0	IO_L28P_0	D9
0	IO_L30N_0	C9
0	IO_L30P_0	B9
0	IO_L49N_0	A8
0	IO_L49P_0	A9
0	IO_L51N_0	G10
0	IO_L51P_0/VREF_0	H10
0	IO_L52N_0	F10

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
7	IO_L78P_7	N6
7	IO_L78N_7	N7
7	IO_L76P_7	N9
7	IO_L76N_7	N8
7	IO_L75P_7/VREF_7	N5
7	IO_L75N_7	M6
7	IO_L73P_7	M1
7	IO_L73N_7	M2
7	IO_L72P_7	M4
7	IO_L72N_7	M5
7	IO_L70P_7	M8
7	IO_L70N_7	M9
7	IO_L69P_7/VREF_7	L1
7	IO_L69N_7	L2
7	IO_L67P_7	L3
7	IO_L67N_7	L4
7	IO_L54P_7	K1
7	IO_L54N_7	K2
7	IO_L52P_7	K4
7	IO_L52N_7	K5
7	IO_L51P_7/VREF_7	L6
7	IO_L51N_7	L7
7	IO_L49P_7	K6
7	IO_L49N_7	K7
7	IO_L48P_7	L8
7	IO_L48N_7	K8
7	IO_L46P_7	J1
7	IO_L46N_7	H1
7	IO_L45P_7/VREF_7	J2
7	IO_L45N_7	J3
7	IO_L43P_7	K3
7	IO_L43N_7	J4
7	IO_L30P_7	H3
7	IO_L30N_7	H4
7	IO_L28P_7	J5
7	IO_L28N_7	J6

BG728/BGG728 Standard BGA Package Specifications (1.27mm pitch)



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	2.33	2.60
A_1	0.50	0.60	0.70
D/E	35.00 BSC		
D_1/E_1	33.02 REF		
e	1.27BSC		
øb	0.60	0.75	0.90
aaa	---	---	0.20
ccc	---	---	0.35
ddd	---	---	0.30
eee	---	---	0.15
M	27		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-BAR-1
4. NO SOLDER BALL AND LAND ON A1.

728-BALL MOLDED BGA (BG728/BGG728)

Figure 6: **BG728/BGG728 Standard BGA Package Specifications**

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
6	IO_L95P_6	W30	
6	IO_L95N_6	V30	
6	IO_L96P_6	V32	
6	IO_L96N_6	W32	
7	IO_L96P_7	U31	
7	IO_L96N_7	V31	
7	IO_L95P_7	T28	
7	IO_L95N_7	U28	
7	IO_L94P_7	U33	
7	IO_L94N_7	U34	
7	IO_L93P_7/VREF_7	U29	
7	IO_L93N_7	T29	
7	IO_L92P_7	U27	
7	IO_L92N_7	U26	
7	IO_L91P_7	T30	
7	IO_L91N_7	U30	
7	IO_L84P_7	R32	NC
7	IO_L84N_7	T32	NC
7	IO_L83P_7	U25	NC
7	IO_L83N_7	T25	NC
7	IO_L82P_7	R34	NC
7	IO_L82N_7	T33	NC
7	IO_L81P_7/VREF_7	N34	NC
7	IO_L81N_7	P34	NC
7	IO_L80P_7	U24	NC
7	IO_L80N_7	T24	NC
7	IO_L79P_7	R31	NC
7	IO_L79N_7	T31	NC
7	IO_L78P_7	N32	
7	IO_L78N_7	P32	
7	IO_L77P_7	T27	
7	IO_L77N_7	R27	
7	IO_L76P_7	N33	
7	IO_L76N_7	P33	
7	IO_L75P_7/VREF_7	R29	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
7	IO_L74P_7	U31		
7	IO_L74N_7	T31		
7	IO_L73P_7	R38		
7	IO_L73N_7	T38		
7	IO_L72P_7	T33		
7	IO_L72N_7	U33		
7	IO_L71P_7	U30		
7	IO_L71N_7	T30		
7	IO_L70P_7	R37		
7	IO_L70N_7	T37		
7	IO_L69P_7/VREF_7	R36		
7	IO_L69N_7	T36		
7	IO_L68P_7	T32		
7	IO_L68N_7	R32		
7	IO_L67P_7	P39		
7	IO_L67N_7	R39		
7	IO_L60P_7	R35		
7	IO_L60N_7	T35		
7	IO_L59P_7	U28		
7	IO_L59N_7	T28		
7	IO_L58P_7	N37		
7	IO_L58N_7	P37		
7	IO_L57P_7/VREF_7	R34		
7	IO_L57N_7	T34		
7	IO_L56P_7	T29		
7	IO_L56N_7	R29		
7	IO_L55P_7	M39		
7	IO_L55N_7	N39		
7	IO_L54P_7	N36		
7	IO_L54N_7	P36		
7	IO_L53P_7	R30		
7	IO_L53N_7	P30		
7	IO_L52P_7	M38		
7	IO_L52N_7	N38		
7	IO_L51P_7/VREF_7	P33		
7	IO_L51N_7	R33		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	DONE	AP7		
NA	M0	AN32		
NA	M1	AP33		
NA	M2	AT35		
NA	HSWAP_EN	E34		
NA	TCK	G8		
NA	TDI	D35		
NA	TDO	E6		
NA	TMS	F7		
NA	PWRDWN_B	AN8		
NA	DXN	G32		
NA	DXP	F33		
NA	VBATT	D5		
NA	RSVD	H9		
NA	VCCAUX	AV20		
NA	VCCAUX	AT37		
NA	VCCAUX	AT3		
NA	VCCAUX	Y38		
NA	VCCAUX	Y2		
NA	VCCAUX	D37		
NA	VCCAUX	D3		
NA	VCCAUX	B20		
NA	VCCINT	AG27		
NA	VCCINT	AG20		
NA	VCCINT	AG13		
NA	VCCINT	AF26		
NA	VCCINT	AF20		
NA	VCCINT	AF14		
NA	VCCINT	AE25		
NA	VCCINT	AE24		
NA	VCCINT	AE23		
NA	VCCINT	AE22		
NA	VCCINT	AE21		
NA	VCCINT	AE20		
NA	VCCINT	AE19		

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
0	IO_L49N_0	C23	
0	IO_L49P_0	C22	
0	IO_L50N_0	E22	
0	IO_L50P_0	E21	
0	IO_L51N_0	F21	
0	IO_L51P_0/VREF_0	F20	
0	IO_L52N_0	A24	
0	IO_L52P_0	A23	
0	IO_L53N_0	E20	
0	IO_L53P_0	E19	
0	IO_L54N_0	B22	
0	IO_L54P_0	B21	
0	IO_L67N_0	D21	
0	IO_L67P_0	D20	
0	IO_L68N_0	J20	
0	IO_L68P_0	J19	
0	IO_L69N_0	F19	
0	IO_L69P_0/VREF_0	F18	
0	IO_L70N_0	A22	
0	IO_L70P_0	A21	
0	IO_L71N_0	H19	
0	IO_L71P_0	H17	
0	IO_L72N_0	C21	
0	IO_L72P_0	C20	
0	IO_L73N_0	B20	
0	IO_L73P_0	B19	
0	IO_L74N_0	G18	
0	IO_L74P_0	G17	
0	IO_L75N_0	E18	
0	IO_L75P_0/VREF_0	D17	
0	IO_L76N_0	A20	
0	IO_L76P_0	A19	
0	IO_L77N_0	D19	
0	IO_L77P_0	D18	
0	IO_L78N_0	C19	
0	IO_L78P_0	C17	
0	IO_L91N_0/VREF_0	K18	
0	IO_L91P_0	J18	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
NA	GND	AG27	
NA	GND	AH4	
NA	GND	AH10	
NA	GND	AH16	
NA	GND	AH22	
NA	GND	AH28	
NA	GND	AJ1	
NA	GND	AJ3	
NA	GND	AJ29	
NA	GND	AJ31	
NA	GND	AK1	
NA	GND	AK2	
NA	GND	AK8	
NA	GND	AK24	
NA	GND	AK30	
NA	GND	AK31	
NA	GND	AL2	
NA	GND	AL3	
NA	GND	AL16	
NA	GND	AL29	
NA	GND	AL30	

Notes:
1. See Table 4 for an explanation of the signals available on this pin.