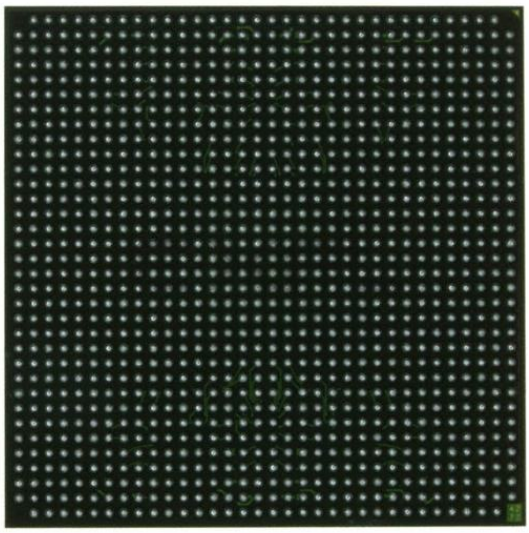

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 8448 |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 2654208 |
| Number of I/O | 824 |
| Number of Gates | 6000000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 1152-BBGA, FCBGA |
| Supplier Device Package | 1152-FCBGA (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc2v6000-6ffg1152c |

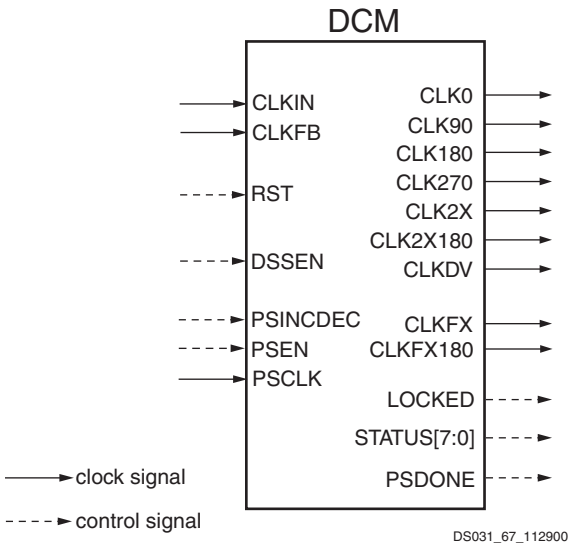


*Figure 45:* **Digital Clock Manager**

The DCM can be configured to delay the completion of the Virtex-II configuration process until after the DCM has achieved lock. This guarantees that the chip does not begin operating until after the system clocks generated by the DCM have stabilized.

The DCM has the following general control signals:

- RST input pin: resets the entire DCM
- LOCKED output pin: asserted High when all enabled DCM circuits have locked.
- STATUS output pins (active High): shown in Table 21.

*Table 21:* **DCM Status Pins**

| Status Pin | Function |
|---|---|
| 0 | Phase Shift Overflow |
| 1 | CLKIN Stopped |
| 2 | CLKFX Stopped |
| 3 | N/A |
| 4 | N/A |
| 5 | N/A |
| 6 | N/A |
| 7 | N/A |

### Clock De-Skew

The DCM de-skews the output clocks relative to the input clock by automatically adjusting a digital delay line. Additional delay is introduced so that clock edges arrive at internal registers and block RAMs simultaneously with the clock edges arriving at the input clock pad. Alternatively, external clocks, which are also de-skewed relative to the input clock, can be generated for board-level routing. All DCM output clocks are phase-aligned to CLK0 and, therefore, are also phase-aligned to the input clock.

To achieve clock de-skew, the CLKFB input must be connected, and its source must be either CLK0 or CLK2X. Note that CLKFB must always be connected, unless only the CLKFX or CLKFX180 outputs are used and de-skew is not required.

### Frequency Synthesis

The DCM provides flexible methods for generating new clock frequencies. Each method has a different operating frequency range and different AC characteristics. The CLK2X and CLK2X180 outputs double the clock frequency. The CLKDV output creates divided output clocks with division options of 1.5, 2, 2.5, 3, 3.5, 4, 4.5, 5, 5.5, 6, 6.5, 7, 7.5, 8, 9, 10, 11, 12, 13, 14, 15, and 16.

The CLKFX and CLKFX180 outputs can be used to produce clocks at the following frequency:

$$FREQ_{CLKFX} = (M/D) * FREQ_{CLKIN}$$

where M and D are two integers. Specifications for M and D are provided under DCM Timing Parameters in Module 3. By default, M=4 and D=1, which results in a clock output frequency four times faster than the clock input frequency (CLKIN).

CLK2X180 is phase shifted 180 degrees relative to CLK2X. CLKFX180 is phase shifted 180 degrees relative to CLKFX. All frequency synthesis outputs automatically have 50/50 duty cycles (with the exception of the CLKDV output when performing a non-integer divide in high-frequency mode).

Note that CLK2X and CLK2X180 are not available in high-frequency mode.

### Phase Shifting

The DCM provides additional control over clock skew through either coarse or fine-grained phase shifting. The CLK0, CLK90, CLK180, and CLK270 outputs are each phase shifted by ¼ of the input clock period relative to each other, providing coarse phase control. Note that CLK90 and CLK270 are not available in high-frequency mode.

Fine-phase adjustment affects all nine DCM output clocks. When activated, the phase shift between the rising edges of CLKIN and CLKFB is a specified fraction of the input clock period.

In variable mode, the PHASE_SHIFT value can also be dynamically incremented or decremented as determined by PSINCDEC synchronously to PSCLK, when the PSEN input is active. Figure 46 illustrates the effects of fine-phase shifting. For more information on DCM features, see the Virtex-II *User Guide*.

*Table 47:* **Sample Window**

| Description | Symbol | Device | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -6 | -5 | -4 | |
| Sampling Error at Receiver Pins(1) | $T_{SAMP}$ | XC2V40 | 500 | 500 | 550 | ps |
| | | XC2V80 | 500 | 500 | 550 | ps |
| | | XC2V250 | 500 | 500 | 550 | ps |
| | | XC2V500 | 500 | 500 | 550 | ps |
| | | XC2V1000 | 500 | 500 | 550 | ps |
| | | XC2V1500 | 500 | 500 | 550 | ps |
| | | XC2V2000 | 500 | 500 | 550 | ps |
| | | XC2V3000 | 500 | 500 | 550 | ps |
| | | XC2V4000 | 500 | 500 | 550 | ps |
| | | XC2V6000 | 500 | 500 | 550 | ps |
| | | XC2V8000 | | 500 | 550 | ps |

**Notes:**
1. This parameter indicates the total sampling error of Virtex-II DDR input registers across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 and CLK180 DCM jitter
   - Worst-case Duty-Cycle Distortion - $T_{DCD\_CLK180}$
   - DCM accuracy (phase offset)
   - DCM phase shift resolution.

   These measurements do not include package or clock tree skew.

*Table 48:* **Pin-to-Pin Setup/Hold: Source-Synchronous Configuration**

| Description | Symbol | Device | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -6 | -5 | -4 | |
| Data Input Set-Up and Hold Times Relative to a Forwarded Clock Input Pin, Using DCM and Global Clock Buffer.<br>For situations where clock and data inputs conform to different standards, adjust the setup and hold values accordingly using the values shown in IOB Input Switching Characteristics Standard Adjustments, page 11. | | | | | | |
| No Delay<br>Global Clock and IFF with DCM | $T_{PSDCM}$/ $T_{PHDCM}$ | XC2V40 | 0.2/0.5 | 0.2/0.5 | 0.2/0.5 | ns |
| | | XC2V80 | 0.2/0.5 | 0.2/0.5 | 0.2/0.5 | ns |
| | | XC2V250 | 0.2/0.5 | 0.2/0.5 | 0.2/0.5 | ns |
| | | XC2V500 | 0.2/0.5 | 0.2/0.5 | 0.2/0.5 | ns |
| | | XC2V1000 | 0.2/0.5 | 0.2/0.5 | 0.2/0.5 | ns |
| | | XC2V1500 | 0.2/0.5 | 0.2/0.5 | 0.2/0.5 | ns |
| | | XC2V2000 | 0.2/0.5 | 0.2/0.5 | 0.2/0.5 | ns |
| | | XC2V3000 | 0.2/0.5 | 0.2/0.5 | 0.2/0.6 | ns |
| | | XC2V4000 | 0.2/0.5 | 0.2/0.6 | 0.2/0.6 | ns |
| | | XC2V6000 | 0.2/0.5 | 0.2/0.6 | 0.2/0.6 | ns |
| | | XC2V8000 | | 0.2/0.6 | 0.2/0.7 | ns |

**Notes:**
1. IFF = Input Flip-Flop
2. The timing values were measured using the fine-phase adjustment feature of the DCM.
3. The worst-case duty-cycle distortion and DCM jitter on CLK0 and CLK180 is included in these measurements.

*Table 5:* **CS144/CSG144 — XC2V40, XC2V80, and XC2V250**

| Bank | Pin Description | Pin Number | No Connect in the XC2V40 |
|---|---|---|---|
| | | | |
| NA | CCLK | M13 | |
| NA | PROG_B | B1 | |
| NA | DONE | N12 | |
| NA | M0 | N2 | |
| NA | M1 | M2 | |
| NA | M2 | M3 | |
| NA | TCK | B12 | |
| NA | TDI | C1 | |
| NA | TDO | C11 | |
| NA | TMS | A13 | |
| NA | PWRDWN_B | M12 | |
| NA | HSWAP_EN | A1 | |
| NA | RSVD | A2 | |
| NA | RSVD | B2 | |
| NA | VBATT | A12 | |
| NA | RSVD | B11 | |
| | | | |
| NA | VCCAUX | C2 | |
| NA | VCCAUX | N1 | |
| NA | VCCAUX | N13 | |
| NA | VCCAUX | B13 | |
| NA | VCCINT | H2 | |
| NA | VCCINT | L7 | |
| NA | VCCINT | H13 | |
| NA | VCCINT | C7 | |
| NA | GND | E1 | |
| NA | GND | G2 | |
| NA | GND | J1 | |
| NA | GND | J4 | |
| NA | GND | M5 | |
| NA | GND | L9 | |
| NA | GND | J11 | |
| NA | GND | H10 | |
| NA | GND | F13 | |
| NA | GND | E12 | |
| NA | GND | B9 | |
| NA | GND | C5 | |

**Notes:**
1. See Table 4 for an explanation of the signals available on this pin.

## FG256/FGG256 Fine-Pitch BGA Package

As shown in Table 6, XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000 Virtex-II devices are available in the FG256/FGG256 fine-pitch BGA package. The pins in the XC2V250, XC2V500, and XC2V1000 devices are same. The No Connect columns show pin differences for the XC2V40 and XC2V80 devices. Following this table are the FG256/FGG256 Fine-Pitch BGA Package Specifications (1.00mm pitch).

*Table 6:* **FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

| Bank | Pin Description | Pin Number | No Connect in XC2V40 | No Connect in XC2V80 |
|---|---|---|---|---|
| 0 | IO_L01N_0 | C4 | | |
| 0 | IO_L01P_0 | B4 | | |
| 0 | IO_L02N_0 | D5 | | |
| 0 | IO_L02P_0 | C5 | | |
| 0 | IO_L03N_0/VRP_0 | B5 | | |
| 0 | IO_L03P_0/VRN_0 | A5 | | |
| 0 | IO_L04N_0/VREF_0 | D6 | NC | NC |
| 0 | IO_L04P_0 | C6 | NC | NC |
| 0 | IO_L05N_0 | B6 | NC | NC |
| 0 | IO_L05P_0 | A6 | NC | NC |
| 0 | IO_L92N_0 | E6 | NC | NC |
| 0 | IO_L92P_0 | E7 | NC | NC |
| 0 | IO_L93N_0 | D7 | NC | NC |
| 0 | IO_L93P_0 | C7 | NC | NC |
| 0 | IO_L94N_0/VREF_0 | B7 | | |
| 0 | IO_L94P_0 | A7 | | |
| 0 | IO_L95N_0/GCLK7P | D8 | | |
| 0 | IO_L95P_0/GCLK6S | C8 | | |
| 0 | IO_L96N_0/GCLK5P | B8 | | |
| 0 | IO_L96P_0/GCLK4S | A8 | | |
| | | | | |
| 1 | IO_L96N_1/GCLK3P | A9 | | |
| 1 | IO_L96P_1/GCLK2S | B9 | | |
| 1 | IO_L95N_1/GCLK1P | C9 | | |
| 1 | IO_L95P_1/GCLK0S | D9 | | |
| 1 | IO_L94N_1 | A10 | | |
| 1 | IO_L94P_1/VREF_1 | B10 | | |
| 1 | IO_L93N_1 | C10 | NC | NC |
| 1 | IO_L93P_1 | D10 | NC | NC |
| 1 | IO_L92N_1 | E10 | NC | NC |

*Table 7:* **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

| Bank | Pin Description | Pin Number | No Connect in XC2V250 | No Connect in XC2V500 |
|---|---|---|---|---|
| 2 | IO_L45N_2 | H19 | | |
| 2 | IO_L45P_2/VREF_2 | H20 | | |
| 2 | IO_L46N_2 | H21 | | |
| 2 | IO_L46P_2 | H22 | | |
| 2 | IO_L48N_2 | J17 | | |
| 2 | IO_L48P_2 | J18 | | |
| 2 | IO_L49N_2 | J19 | NC | |
| 2 | IO_L49P_2 | J20 | NC | |
| 2 | IO_L51N_2 | J21 | NC | |
| 2 | IO_L51P_2/VREF_2 | J22 | NC | |
| 2 | IO_L52N_2 | K17 | NC | |
| 2 | IO_L52P_2 | K18 | NC | |
| 2 | IO_L54N_2 | K19 | NC | |
| 2 | IO_L54P_2 | K20 | NC | |
| 2 | IO_L91N_2 | K21 | | |
| 2 | IO_L91P_2 | K22 | | |
| 2 | IO_L93N_2 | L17 | | |
| 2 | IO_L93P_2/VREF_2 | L18 | | |
| 2 | IO_L94N_2 | L19 | | |
| 2 | IO_L94P_2 | L20 | | |
| 2 | IO_L96N_2 | L21 | | |
| 2 | IO_L96P_2 | L22 | | |
| | | | | |
| 3 | IO_L96N_3 | M21 | | |
| 3 | IO_L96P_3 | M20 | | |
| 3 | IO_L94N_3 | M19 | | |
| 3 | IO_L94P_3 | M18 | | |
| 3 | IO_L93N_3/VREF_3 | M17 | | |
| 3 | IO_L93P_3 | N17 | | |
| 3 | IO_L91N_3 | N22 | | |
| 3 | IO_L91P_3 | N21 | | |
| 3 | IO_L54N_3 | N20 | NC | |
| 3 | IO_L54P_3 | N19 | NC | |
| 3 | IO_L52N_3 | N18 | NC | |

*Table 7:* **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

| Bank | Pin Description | Pin Number | No Connect in XC2V250 | No Connect in XC2V500 |
|---|---|---|---|---|
| NA | GND | M10 | | |
| NA | GND | M9 | | |
| NA | GND | L14 | | |
| NA | GND | L13 | | |
| NA | GND | L12 | | |
| NA | GND | L11 | | |
| NA | GND | L10 | | |
| NA | GND | L9 | | |
| NA | GND | K14 | | |
| NA | GND | K13 | | |
| NA | GND | K12 | | |
| NA | GND | K11 | | |
| NA | GND | K10 | | |
| NA | GND | K9 | | |
| NA | GND | J14 | | |
| NA | GND | J13 | | |
| NA | GND | J12 | | |
| NA | GND | J11 | | |
| NA | GND | J10 | | |
| NA | GND | J9 | | |
| NA | GND | D19 | | |
| NA | GND | D4 | | |
| NA | GND | C20 | | |
| NA | GND | C3 | | |
| NA | GND | B21 | | |
| NA | GND | B2 | | |
| NA | GND | A22 | | |
| NA | GND | A1 | | |

**Notes:**
1. See Table 4 for an explanation of the signals available on this pin.

*Table 8:* **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

| Bank | Pin Description | Pin Number | No Connect in XC2V1500 | No Connect in XC2V2000 |
|---|---|---|---|---|
| 3 | IO_L46P_3 | Y26 | | |
| 3 | IO_L45N_3/VREF_3 | U20 | | |
| 3 | IO_L45P_3 | V20 | | |
| 3 | IO_L43N_3 | W25 | | |
| 3 | IO_L43P_3 | W24 | | |
| 3 | IO_L25N_3 | V21 | NC | NC |
| 3 | IO_L25P_3 | W21 | NC | NC |
| 3 | IO_L24N_3 | AA26 | | |
| 3 | IO_L24P_3 | AA25 | | |
| 3 | IO_L22N_3 | Y24 | | |
| 3 | IO_L22P_3 | Y23 | | |
| 3 | IO_L21N_3/VREF_3 | W22 | | |
| 3 | IO_L21P_3 | W23 | | |
| 3 | IO_L19N_3 | AB26 | | |
| 3 | IO_L19P_3 | AB25 | | |
| 3 | IO_L06N_3 | AC26 | | |
| 3 | IO_L06P_3 | AC25 | | |
| 3 | IO_L04N_3 | AD26 | | |
| 3 | IO_L04P_3 | AD25 | | |
| 3 | IO_L03N_3/VREF_3 | AA24 | | |
| 3 | IO_L03P_3 | AA23 | | |
| 3 | IO_L02N_3/VRP_3 | AB24 | | |
| 3 | IO_L02P_3/VRN_3 | AB23 | | |
| 3 | IO_L01N_3 | Y22 | | |
| 3 | IO_L01P_3 | AA22 | | |
| | | | | |
| 4 | IO_L01N_4/BUSY/DOUT(1) | AD21 | | |
| 4 | IO_L01P_4/INIT_B | AC21 | | |
| 4 | IO_L02N_4/D0/DIN(1) | Y20 | | |
| 4 | IO_L02P_4/D1 | Y19 | | |
| 4 | IO_L03N_4/D2/ALT_VRP_4 | AA20 | | |
| 4 | IO_L03P_4/D3/ALT_VRN_4 | AB20 | | |
| 4 | IO_L04N_4/VREF_4 | AC22 | | |
| 4 | IO_L04P_4 | AE21 | | |
| 4 | IO_L05N_4/VRP_4 | AE26 | | |
| 4 | IO_L05P_4/VRN_4 | AF25 | | |
| 4 | IO_L06N_4 | W20 | | |

*Table 8:* **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

| Bank | Pin Description | Pin Number | No Connect in XC2V1500 | No Connect in XC2V2000 |
|---|---|---|---|---|
| NA | VCCINT | H19 | | |
| NA | VCCINT | H8 | | |
| NA | GND | AF26 | | |
| NA | GND | AF1 | | |
| NA | GND | AE25 | | |
| NA | GND | AE14 | | |
| NA | GND | AE13 | | |
| NA | GND | AE2 | | |
| NA | GND | AD24 | | |
| NA | GND | AD3 | | |
| NA | GND | AC23 | | |
| NA | GND | AC4 | | |
| NA | GND | AB22 | | |
| NA | GND | AB5 | | |
| NA | GND | AA21 | | |
| NA | GND | AA6 | | |
| NA | GND | U17 | | |
| NA | GND | U16 | | |
| NA | GND | U15 | | |
| NA | GND | U14 | | |
| NA | GND | U13 | | |
| NA | GND | U12 | | |
| NA | GND | U11 | | |
| NA | GND | U10 | | |
| NA | GND | T17 | | |
| NA | GND | T16 | | |
| NA | GND | T15 | | |
| NA | GND | T14 | | |
| NA | GND | T13 | | |
| NA | GND | T12 | | |
| NA | GND | T11 | | |
| NA | GND | T10 | | |
| NA | GND | R17 | | |
| NA | GND | R16 | | |
| NA | GND | R15 | | |
| NA | GND | R14 | | |
| NA | GND | R13 | | |

*Table 9:* **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

| Bank | Pin Description | Pin Number | No Connect in XC2V1000 | No Connect in XC2V1500 |
|---|---|---|---|---|
| NA | GND | D15 | | |
| NA | GND | D10 | | |
| NA | GND | D4 | | |
| NA | GND | C22 | | |
| NA | GND | C3 | | |
| NA | GND | B24 | | |
| NA | GND | B23 | | |
| NA | GND | B2 | | |
| NA | GND | B1 | | |
| NA | GND | A24 | | |
| NA | GND | A23 | | |
| NA | GND | A18 | | |
| NA | GND | A7 | | |
| NA | GND | A2 | | |

**Notes:**
1. See Table 4 for an explanation of the signals available on this pin.

*Table 10:* **BG728 BGA — XC2V3000**

| Bank | Pin Description | Pin Number |
|---|---|---|
| 3 | IO_L72N_3 | T20 |
| 3 | IO_L72P_3 | T19 |
| 3 | IO_L70N_3 | U27 |
| 3 | IO_L70P_3 | U26 |
| 3 | IO_L69N_3/VREF_3 | U25 |
| 3 | IO_L69P_3 | V25 |
| 3 | IO_L67N_3 | U21 |
| 3 | IO_L67P_3 | U20 |
| 3 | IO_L54N_3 | V27 |
| 3 | IO_L54P_3 | V26 |
| 3 | IO_L52N_3 | V24 |
| 3 | IO_L52P_3 | V23 |
| 3 | IO_L51N_3/VREF_3 | V22 |
| 3 | IO_L51P_3 | W22 |
| 3 | IO_L49N_3 | V21 |
| 3 | IO_L49P_3 | V20 |
| 3 | IO_L48N_3 | W27 |
| 3 | IO_L48P_3 | Y27 |
| 3 | IO_L46N_3 | W26 |
| 3 | IO_L46P_3 | W25 |
| 3 | IO_L45N_3/VREF_3 | W24 |
| 3 | IO_L45P_3 | W23 |
| 3 | IO_L43N_3 | W21 |
| 3 | IO_L43P_3 | W20 |
| 3 | IO_L28N_3 | W19 |
| 3 | IO_L28P_3 | Y19 |
| 3 | IO_L27N_3/VREF_3 | Y25 |
| 3 | IO_L27P_3 | Y24 |
| 3 | IO_L25N_3 | Y23 |
| 3 | IO_L25P_3 | AA23 |
| 3 | IO_L24N_3 | Y22 |
| 3 | IO_L24P_3 | Y21 |
| 3 | IO_L22N_3 | AA27 |
| 3 | IO_L22P_3 | AB27 |
| 3 | IO_L21N_3/VREF_3 | AA26 |
| 3 | IO_L21P_3 | AA25 |

*Table 12:* **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

| Bank | Pin Description | Pin Number | No Connect in the XC2V3000 |
|---|---|---|---|
| 3 | IO_L23P_3 | AJ3 | |
| 3 | IO_L22N_3 | AF7 | |
| 3 | IO_L22P_3 | AG7 | |
| 3 | IO_L21N_3/VREF_3 | AL1 | |
| 3 | IO_L21P_3 | AK1 | |
| 3 | IO_L20N_3 | AH2 | |
| 3 | IO_L20P_3 | AJ2 | |
| 3 | IO_L19N_3 | AJ4 | |
| 3 | IO_L19P_3 | AK4 | |
| 3 | IO_L06N_3 | AE10 | |
| 3 | IO_L06P_3 | AD10 | |
| 3 | IO_L05N_3 | AK2 | |
| 3 | IO_L05P_3 | AL2 | |
| 3 | IO_L04N_3 | AH6 | |
| 3 | IO_L04P_3 | AJ5 | |
| 3 | IO_L03N_3/VREF_3 | AE11 | |
| 3 | IO_L03P_3 | AF11 | |
| 3 | IO_L02N_3/VRP_3 | AK3 | |
| 3 | IO_L02P_3/VRN_3 | AL3 | |
| 3 | IO_L01N_3 | AF10 | |
| 3 | IO_L01P_3 | AG9 | |
| | | | |
| 4 | IO_L01N_4/BUSY/DOUT(1) | AM4 | |
| 4 | IO_L01P_4/INIT_B | AL5 | |
| 4 | IO_L02N_4/D0/DIN(1) | AG10 | |
| 4 | IO_L02P_4/D1 | AH11 | |
| 4 | IO_L03N_4/D2/ALT_VRP_4 | AK7 | |
| 4 | IO_L03P_4/D3/ALT_VRN_4 | AK8 | |
| 4 | IO_L04N_4/VREF_4 | AL6 | |
| 4 | IO_L04P_4 | AM6 | |
| 4 | IO_L05N_4/VRP_4 | AK9 | |
| 4 | IO_L05P_4/VRN_4 | AJ8 | |
| 4 | IO_L06N_4 | AM8 | |
| 4 | IO_L06P_4 | AM7 | |
| 4 | IO_L19N_4 | AN3 | |
| 4 | IO_L19P_4 | AM2 | |

*Table 12:* **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

| Bank | Pin Description | Pin Number | No Connect in the XC2V3000 |
|---|---|---|---|
| NA | GND | V19 | |
| NA | GND | V18 | |
| NA | GND | V17 | |
| NA | GND | V16 | |
| NA | GND | V15 | |
| NA | GND | V14 | |
| NA | GND | U21 | |
| NA | GND | U20 | |
| NA | GND | U19 | |
| NA | GND | U18 | |
| NA | GND | U17 | |
| NA | GND | U16 | |
| NA | GND | U15 | |
| NA | GND | U14 | |
| NA | GND | T26 | |
| NA | GND | T21 | |
| NA | GND | T20 | |
| NA | GND | T19 | |
| NA | GND | T18 | |
| NA | GND | T17 | |
| NA | GND | T16 | |
| NA | GND | T15 | |
| NA | GND | T14 | |
| NA | GND | T9 | |
| NA | GND | R33 | |
| NA | GND | R21 | |
| NA | GND | R20 | |
| NA | GND | R19 | |
| NA | GND | R18 | |
| NA | GND | R17 | |
| NA | GND | R16 | |
| NA | GND | R15 | |
| NA | GND | R14 | |
| NA | GND | R2 | |
| NA | GND | P28 | |
| NA | GND | P21 | |

*Table 13:* **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

| Bank | Pin Description | Pin Number | No Connect in the XC2V4000 | No Connect in the XC2V6000 |
|---|---|---|---|---|
| 1 | IO_L33N_1/VREF_1 | D11 | NC | |
| 1 | IO_L33P_1 | D12 | NC | |
| 1 | IO_L32N_1 | H14 | NC | |
| 1 | IO_L32P_1 | H13 | NC | |
| 1 | IO_L31N_1 | A8 | NC | |
| 1 | IO_L31P_1 | A9 | NC | |
| 1 | IO_L30N_1 | F11 | | |
| 1 | IO_L30P_1 | F12 | | |
| 1 | IO_L29N_1 | K14 | | |
| 1 | IO_L29P_1 | L14 | | |
| 1 | IO_L28N_1 | C9 | | |
| 1 | IO_L28P_1 | C10 | | |
| 1 | IO_L27N_1/VREF_1 | G11 | | |
| 1 | IO_L27P_1 | G12 | | |
| 1 | IO_L26N_1 | M15 | | |
| 1 | IO_L26P_1 | M14 | | |
| 1 | IO_L25N_1 | B7 | | |
| 1 | IO_L25P_1 | B8 | | |
| 1 | IO_L24N_1 | D9 | | |
| 1 | IO_L24P_1 | D10 | | |
| 1 | IO_L23N_1 | J13 | | |
| 1 | IO_L23P_1 | J12 | | |
| 1 | IO_L22N_1 | A6 | | |
| 1 | IO_L22P_1 | A7 | | |
| 1 | IO_L21N_1/VREF_1 | E9 | | |
| 1 | IO_L21P_1 | E10 | | |
| 1 | IO_L20N_1 | D8 | | |
| 1 | IO_L20P_1 | E7 | | |
| 1 | IO_L19N_1 | C7 | | |
| 1 | IO_L19P_1 | C8 | | |
| 1 | IO_L12N_1 | F9 | NC | |
| 1 | IO_L12P_1 | F10 | NC | |
| 1 | IO_L11N_1 | H12 | NC | |
| 1 | IO_L11P_1 | H11 | NC | |
| 1 | IO_L10N_1 | B5 | NC | |
| 1 | IO_L10P_1 | B6 | NC | |

*Table 13:* **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

| Bank | Pin Description | Pin Number | No Connect in the XC2V4000 | No Connect in the XC2V6000 |
|---|---|---|---|---|
| 2 | IO_L57P_2/VREF_2 | P7 | | |
| 2 | IO_L58N_2 | R3 | | |
| 2 | IO_L58P_2 | P3 | | |
| 2 | IO_L59N_2 | T10 | | |
| 2 | IO_L59P_2 | U10 | | |
| 2 | IO_L60N_2 | P4 | | |
| 2 | IO_L60P_2 | N4 | | |
| 2 | IO_L67N_2 | T6 | | |
| 2 | IO_L67P_2 | R6 | | |
| 2 | IO_L68N_2 | T9 | | |
| 2 | IO_L68P_2 | U9 | | |
| 2 | IO_L69N_2 | T5 | | |
| 2 | IO_L69P_2/VREF_2 | R5 | | |
| 2 | IO_L70N_2 | R1 | | |
| 2 | IO_L70P_2 | P1 | | |
| 2 | IO_L71N_2 | V12 | | |
| 2 | IO_L71P_2 | W12 | | |
| 2 | IO_L72N_2 | T4 | | |
| 2 | IO_L72P_2 | R4 | | |
| 2 | IO_L73N_2 | T2 | | |
| 2 | IO_L73P_2 | R2 | | |
| 2 | IO_L74N_2 | V11 | | |
| 2 | IO_L74P_2 | W11 | | |
| 2 | IO_L75N_2 | U7 | | |
| 2 | IO_L75P_2/VREF_2 | T7 | | |
| 2 | IO_L76N_2 | U3 | | |
| 2 | IO_L76P_2 | T3 | | |
| 2 | IO_L77N_2 | V10 | | |
| 2 | IO_L77P_2 | W10 | | |
| 2 | IO_L78N_2 | V6 | | |
| 2 | IO_L78P_2 | U6 | | |
| 2 | IO_L79N_2 | U1 | | |
| 2 | IO_L79P_2 | T1 | | |
| 2 | IO_L80N_2 | V9 | | |
| 2 | IO_L80P_2 | W9 | | |
| 2 | IO_L81N_2 | V5 | | |

*Table 13:* **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

| Bank | Pin Description | Pin Number | No Connect in the XC2V4000 | No Connect in the XC2V6000 |
|---|---|---|---|---|
| 6 | IO_L23N_6 | AM38 | | |
| 6 | IO_L24P_6 | AM36 | | |
| 6 | IO_L24N_6 | AN36 | | |
| 6 | IO_L25P_6 | AH30 | | |
| 6 | IO_L25N_6 | AG30 | | |
| 6 | IO_L26P_6 | AM37 | | |
| 6 | IO_L26N_6 | AL37 | | |
| 6 | IO_L27P_6 | AK34 | | |
| 6 | IO_L27N_6/VREF_6 | AL34 | | |
| 6 | IO_L28P_6 | AG29 | | |
| 6 | IO_L28N_6 | AF29 | | |
| 6 | IO_L29P_6 | AL35 | | |
| 6 | IO_L29N_6 | AK35 | | |
| 6 | IO_L30P_6 | AH33 | | |
| 6 | IO_L30N_6 | AJ33 | | |
| 6 | IO_L31P_6 | AJ32 | NC | |
| 6 | IO_L31N_6 | AH32 | NC | |
| 6 | IO_L32P_6 | AM39 | NC | |
| 6 | IO_L32N_6 | AL39 | NC | |
| 6 | IO_L33P_6 | AK36 | NC | |
| 6 | IO_L33N_6/VREF_6 | AL36 | NC | |
| 6 | IO_L34P_6 | AF28 | NC | |
| 6 | IO_L34N_6 | AE28 | NC | |
| 6 | IO_L35P_6 | AL38 | NC | |
| 6 | IO_L35N_6 | AK38 | NC | |
| 6 | IO_L36P_6 | AH34 | NC | |
| 6 | IO_L36N_6 | AJ34 | NC | |
| 6 | IO_L43P_6 | AG31 | | |
| 6 | IO_L43N_6 | AF31 | | |
| 6 | IO_L44P_6 | AK37 | | |
| 6 | IO_L44N_6 | AJ37 | | |
| 6 | IO_L45P_6 | AH36 | | |
| 6 | IO_L45N_6/VREF_6 | AJ36 | | |
| 6 | IO_L46P_6 | AF30 | | |
| 6 | IO_L46N_6 | AE30 | | |
| 6 | IO_L47P_6 | AK39 | | |

*Table 13:* **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

| Bank | Pin Description | Pin Number | No Connect in the XC2V4000 | No Connect in the XC2V6000 |
|---|---|---|---|---|
| 6 | IO_L71N_6 | AE39 | | |
| 6 | IO_L72P_6 | AD36 | | |
| 6 | IO_L72N_6 | AE36 | | |
| 6 | IO_L73P_6 | AB29 | | |
| 6 | IO_L73N_6 | AA29 | | |
| 6 | IO_L74P_6 | AE38 | | |
| 6 | IO_L74N_6 | AD38 | | |
| 6 | IO_L75P_6 | AC33 | | |
| 6 | IO_L75N_6/VREF_6 | AD33 | | |
| 6 | IO_L76P_6 | AB30 | | |
| 6 | IO_L76N_6 | AA30 | | |
| 6 | IO_L77P_6 | AD37 | | |
| 6 | IO_L77N_6 | AC37 | | |
| 6 | IO_L78P_6 | AB34 | | |
| 6 | IO_L78N_6 | AC34 | | |
| 6 | IO_L79P_6 | AB31 | | |
| 6 | IO_L79N_6 | AA31 | | |
| 6 | IO_L80P_6 | AD39 | | |
| 6 | IO_L80N_6 | AC39 | | |
| 6 | IO_L81P_6 | AB35 | | |
| 6 | IO_L81N_6/VREF_6 | AC35 | | |
| 6 | IO_L82P_6 | AB32 | | |
| 6 | IO_L82N_6 | AA32 | | |
| 6 | IO_L83P_6 | AC38 | | |
| 6 | IO_L83N_6 | AB38 | | |
| 6 | IO_L84P_6 | AA33 | | |
| 6 | IO_L84N_6 | AB33 | | |
| 6 | IO_L91P_6 | Y28 | | |
| 6 | IO_L91N_6 | Y29 | | |
| 6 | IO_L92P_6 | AB39 | | |
| 6 | IO_L92N_6 | AA39 | | |
| 6 | IO_L93P_6 | AA36 | | |
| 6 | IO_L93N_6/VREF_6 | AB36 | | |
| 6 | IO_L94P_6 | Y31 | | |
| 6 | IO_L94N_6 | Y32 | | |
| 6 | IO_L95P_6 | AA37 | | |

*Table 13:* **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

| Bank | Pin Description | Pin Number | No Connect in the XC2V4000 | No Connect in the XC2V6000 |
|---|---|---|---|---|
| 7 | IO_L26P_7 | M31 | | |
| 7 | IO_L26N_7 | L31 | | |
| 7 | IO_L25P_7 | G38 | | |
| 7 | IO_L25N_7 | H38 | | |
| 7 | IO_L24P_7 | J34 | | |
| 7 | IO_L24N_7 | K34 | | |
| 7 | IO_L23P_7 | K32 | | |
| 7 | IO_L23N_7 | K31 | | |
| 7 | IO_L22P_7 | F39 | | |
| 7 | IO_L22N_7 | G39 | | |
| 7 | IO_L21P_7/VREF_7 | G36 | | |
| 7 | IO_L21N_7 | H36 | | |
| 7 | IO_L20P_7 | N28 | | |
| 7 | IO_L20N_7 | M28 | | |
| 7 | IO_L19P_7 | G37 | | |
| 7 | IO_L19N_7 | H37 | | |
| 7 | IO_L12P_7 | J33 | NC | |
| 7 | IO_L12N_7 | K33 | NC | |
| 7 | IO_L11P_7 | M29 | NC | |
| 7 | IO_L11N_7 | L28 | NC | |
| 7 | IO_L10P_7 | E38 | NC | |
| 7 | IO_L10N_7 | F38 | NC | |
| 7 | IO_L09P_7/VREF_7 | G35 | NC | |
| 7 | IO_L09N_7 | H35 | NC | |
| 7 | IO_L08P_7 | L30 | NC | |
| 7 | IO_L08N_7 | K29 | NC | |
| 7 | IO_L07P_7 | D39 | NC | |
| 7 | IO_L07N_7 | E39 | NC | |
| 7 | IO_L06P_7 | G34 | | |
| 7 | IO_L06N_7 | H34 | | |
| 7 | IO_L05P_7 | J32 | | |
| 7 | IO_L05N_7 | H33 | | |
| 7 | IO_L04P_7 | F36 | | |
| 7 | IO_L04N_7 | F37 | | |
| 7 | IO_L03P_7/VREF_7 | E36 | | |
| 7 | IO_L03N_7 | F35 | | |

*Table 13:* **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

| Bank | Pin Description | Pin Number | No Connect in the XC2V4000 | No Connect in the XC2V6000 |
|---|---|---|---|---|
| NA | GND | D4 | | |
| NA | GND | C39 | | |
| NA | GND | C38 | | |
| NA | GND | C37 | | |
| NA | GND | C3 | | |
| NA | GND | C2 | | |
| NA | GND | C1 | | |
| NA | GND | B39 | | |
| NA | GND | B38 | | |
| NA | GND | B37 | | |
| NA | GND | B29 | | |
| NA | GND | B11 | | |
| NA | GND | B3 | | |
| NA | GND | B2 | | |
| NA | GND | B1 | | |
| NA | GND | A38 | | |
| NA | GND | A37 | | |
| NA | GND | A20 | | |
| NA | GND | A3 | | |
| NA | GND | A2 | | |

**Notes:**
1. See Table 4 for an explanation of the signals available on this pin.

*Table 14:* **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

| Bank | Pin Description | Pin Number | No Connect in XC2V2000 |
|---|---|---|---|
| 7 | IO_L06N_7 | E28 | |
| 7 | IO_L05P_7 | K22 | |
| 7 | IO_L05N_7 | K21 | |
| 7 | IO_L04P_7 | F29 | |
| 7 | IO_L04N_7 | E29 | |
| 7 | IO_L03P_7/VREF_7 | H26 | |
| 7 | IO_L03N_7 | H25 | |
| 7 | IO_L02P_7/VRN_7 | G26 | |
| 7 | IO_L02N_7/VRP_7 | F27 | |
| 7 | IO_L01P_7 | D30 | |
| 7 | IO_L01N_7 | D29 | |
| | | | |
| 0 | VCCO_0 | C18 | |
| 0 | VCCO_0 | C25 | |
| 0 | VCCO_0 | F22 | |
| 0 | VCCO_0 | H18 | |
| 0 | VCCO_0 | L17 | |
| 0 | VCCO_0 | L18 | |
| 0 | VCCO_0 | L19 | |
| 0 | VCCO_0 | L20 | |
| 0 | VCCO_0 | M17 | |
| 0 | VCCO_0 | M18 | |
| 0 | VCCO_0 | M19 | |
| 1 | VCCO_1 | C7 | |
| 1 | VCCO_1 | C14 | |
| 1 | VCCO_1 | F10 | |
| 1 | VCCO_1 | H14 | |
| 1 | VCCO_1 | L12 | |
| 1 | VCCO_1 | L13 | |
| 1 | VCCO_1 | L14 | |
| 1 | VCCO_1 | L15 | |
| 1 | VCCO_1 | M13 | |
| 1 | VCCO_1 | M14 | |
| 1 | VCCO_1 | M15 | |
| 2 | VCCO_2 | G3 | |
| 2 | VCCO_2 | K6 | |
| 2 | VCCO_2 | M11 | |
| 2 | VCCO_2 | N11 | |

## Notice of Disclaimer



## Virtex-II Data Sheet

The Virtex-II Data Sheet contains the following modules: