Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	128
Number of Logic Elements/Cells	-
Total RAM Bits	147456
Number of I/O	92
Number of Gates	80000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-TFBGA, CSPBGA
Supplier Device Package	144-LCSBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v80-4csg144c

Architecture

Virtex-II Array Overview

Virtex-II devices are user-programmable gate arrays with various configurable elements. The Virtex-II architecture is optimized for high-density and high-performance logic designs. As shown in Figure 1, the programmable device is comprised of input/output blocks (IOBs) and internal configurable logic blocks (CLBs).

Programmable I/O blocks provide the interface between package pins and the internal configurable logic. Most popular and leading-edge I/O standards are supported by the programmable IOBs.

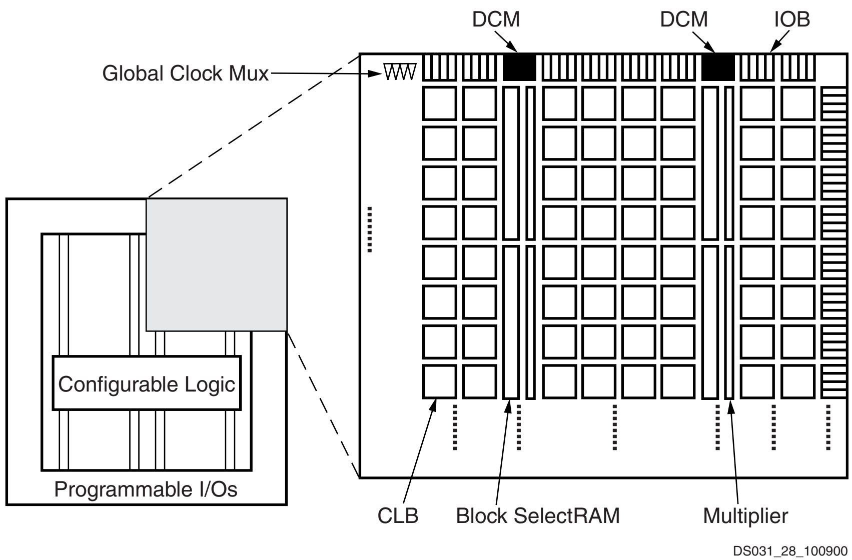


Figure 1: **Virtex-II Architecture Overview**

The internal configurable logic includes four major elements organized in a regular array.

- Configurable Logic Blocks (CLBs) provide functional elements for combinatorial and synchronous logic, including basic storage elements. BUFTs (3-state buffers) associated with each CLB element drive dedicated segmentable horizontal routing resources.
- Block SelectRAM memory modules provide large 18 Kbit storage elements of dual-port RAM.
- Multiplier blocks are 18-bit x 18-bit dedicated multipliers.
- DCM (Digital Clock Manager) blocks provide self-calibrating, fully digital solutions for clock distribution delay compensation, clock multiplication and division, coarse- and fine-grained clock phase shifting.

A new generation of programmable routing resources called Active Interconnect Technology interconnects all of these elements. The general routing matrix (GRM) is an array of routing switches. Each programmable element is tied to a switch matrix, allowing multiple connections to the general routing matrix. The overall programmable interconnection is hierarchical and designed to support high-speed designs.

All programmable elements, including the routing resources, are controlled by values stored in static memory cells. These values are loaded in the memory cells during configuration and can be reloaded to change the functions of the programmable elements.

Virtex-II Features

This section briefly describes Virtex-II features.

Input/Output Blocks (IOBs)

IOBs are programmable and can be categorized as follows:

- Input block with an optional single-data-rate or double-data-rate (DDR) register
- Output block with an optional single-data-rate or DDR register, and an optional 3-state buffer, to be driven directly or through a single or DDR register
- Bidirectional block (any combination of input and output configurations)

These registers are either edge-triggered D-type flip-flops or level-sensitive latches.

IOBs support the following single-ended I/O standards:

- LVTTL, LVCMOS (3.3V, 2.5V, 1.8V, and 1.5V)
- PCI-X compatible (133 MHz and 66 MHz) at 3.3V
- PCI compliant (66 MHz and 33 MHz) at 3.3V
- CardBus compliant (33 MHz) at 3.3V
- GTL and GTLP

- HSTL (Class I, II, III, and IV)
- SSTL (3.3V and 2.5V, Class I and II)
- AGP-2X

The digitally controlled impedance (DCI) I/O feature automatically provides on-chip termination for each I/O element.

The IOB elements also support the following differential signaling I/O standards:

- LVDS
- BLVDS (Bus LVDS)
- ULVDS
- LDT
- LVPECL

Two adjacent pads are used for each differential pair. Two or four IOB blocks connect to one switch matrix to access the routing resources.

Configurable Logic Blocks (CLBs)

CLB resources include four slices and two 3-state buffers. Each slice is equivalent and contains:

- Two function generators (F & G)
- Two storage elements
- Arithmetic logic gates
- Large multiplexers
- Wide function capability
- Fast carry look-ahead chain
- Horizontal cascade chain (OR gate)

The function generators F & G are configurable as 4-input look-up tables (LUTs), as 16-bit shift registers, or as 16-bit distributed SelectRAM memory.

In addition, the two storage elements are either edge-triggered D-type flip-flops or level-sensitive latches.

Each CLB has internal fast interconnect and connects to a switch matrix to access general routing resources.

Block SelectRAM Memory

The block SelectRAM memory resources are 18 Kb of dual-port RAM, programmable from 16K x 1 bit to 512 x 36 bits, in various depth and width configurations. Each port is totally synchronous and independent, offering three "read-during-write" modes. Block SelectRAM memory is cascadable to implement large embedded storage blocks. Supported memory configurations for dual-port and single-port modes are shown in Table 3.

Table 3: **Dual-Port And Single-Port Configurations**

16K x 1 bit	2K x 9 bits
8K x 2 bits	1K x 18 bits
4K x 4 bits	512 x 36 bits

A multiplier block is associated with each SelectRAM memory block. The multiplier block is a dedicated 18 x 18-bit multiplier and is optimized for operations based on the block SelectRAM content on one port. The 18 x 18 multiplier can be used independently of the block SelectRAM resource. Read/multiply/accumulate operations and DSP filter structures are extremely efficient.

Both the SelectRAM memory and the multiplier resource are connected to four switch matrices to access the general routing resources.

Global Clocking

The DCM and global clock multiplexer buffers provide a complete solution for designing high-speed clocking schemes.

Up to 12 DCM blocks are available. To generate de-skewed internal or external clocks, each DCM can be used to eliminate clock distribution delay. The DCM also provides 90-, 180-, and 270-degree phase-shifted versions of its output clocks. Fine-grained phase shifting offers high-resolution phase adjustments in increments of 1/256 of the clock period. Very flexible frequency synthesis provides a clock output frequency equal to any M/D ratio of the input clock frequency, where M and D are two integers. For the exact timing parameters, see Virtex-II Electrical Characteristics.

Virtex-II devices have 16 global clock MUX buffers, with up to eight clock nets per quadrant. Each global clock MUX buffer can select one of the two clock inputs and switch glitch-free from one clock to the other. Each DCM block is able to drive up to four of the 16 global clock MUX buffers.

Routing Resources

The IOB, CLB, block SelectRAM, multiplier, and DCM elements all use the same interconnect scheme and the same access to the global routing matrix. Timing models are shared, greatly improving the predictability of the performance of high-speed designs.

There are a total of 16 global clock lines, with eight available per quadrant. In addition, 24 vertical and horizontal long lines per row or column as well as massive secondary and local routing resources provide fast interconnect. Virtex-II buffered interconnects are relatively unaffected by net fanout and the interconnect layout is designed to minimize crosstalk.

Horizontal and vertical routing resources for each row or column include:

- 24 long lines
- 120 hex lines
- 40 double lines
- 16 direct connect lines (total in all four directions)

Table 14: **IOB Input Switching Characteristics** ***(Continued)***

			Speed Grade			
Description	**Symbol**	**Device**	**-6**	**-5**	**-4**	**Units**
Propagation Delays						
Pad to output IQ via transparent latch, no delay	T_{IOPLI}	All	0.83	0.91	1.05	ns, Max
Pad to output IQ via transparent latch, with delay	T_{IOPLID}	XC2V40	3.23	3.55	4.09	ns, Max
		XC2V80	3.23	3.55	4.09	ns, Max
		XC2V250	3.23	3.55	4.09	ns, Max
		XC2V500	3.23	3.55	4.09	ns, Max
		XC2V1000	3.23	3.55	4.09	ns, Max
		XC2V1500	3.23	3.55	4.09	ns, Max
		XC2V2000	3.23	3.55	4.09	ns, Max
		XC2V3000	3.32	3.65	4.20	ns, Max
		XC2V4000	3.32	3.65	4.20	ns, Max
		XC2V6000	3.60	3.95	4.55	ns, Max
		XC2V8000		3.95	4.55	ns, Max
Clock CLK to output IQ	T_{IOCKIQ}	All		0.67	0.77	ns, Max
Setup and Hold Times With Respect to Clock at IOB Input Register						
Pad, no delay	T_{IOPICK}/T_{IOICKP}	All	0.84/–0.36	0.92/–0.39	1.06/–0.45	ns, Min
Pad, with delay	$T_{IOPICKD}/T_{IOICKPD}$	XC2V40	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V80	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V250	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V500	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V1000	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V1500	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V2000	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V3000	3.33/–2.10	3.67/–2.31	4.22/–2.66	ns, Min
		XC2V4000	3.33/–2.10	3.67/–2.31	4.22/–2.66	ns, Min
		XC2V6000	3.61/–2.29	3.97/–2.52	4.56/–2.90	ns, Min
		XC2V8000		3.97/–2.52	4.56/–2.90	ns, Min
ICE input	$T_{IOICECK}/T_{IOCKICE}$	All		0.21/ 0.04	0.24/ 0.04	ns, Min
SR input (IFF, synchronous)	$T_{IOSRCKI}$	All	0.27	0.30	0.34	ns, Min
Set/Reset Delays						
SR input to IQ (asynchronous)	T_{IOSRIQ}	All	1.11	1.22	1.40	ns, Max
GSR to output IQ	T_{GSRQ}	All	5.44	5.98	6.88	ns, Max

Notes:
1. Input timing for LVTTL is measured at 1.4 V. For other I/O standards, see Table 18.

Multiplier Switching Characteristics

Table 24: **Multiplier Switching Characteristics**

Description	Symbol	Speed Grade -6	Speed Grade -5	Speed Grade -4	Units
Propagation Delay to Output Pin					
Input to Pin 35	T_{MULT_P35}	4.66	8.50	10.36	ns, Max
Input to Pin 34	T_{MULT_P34}	4.57	8.33	10.15	ns, Max
Input to Pin 33	T_{MULT_P33}	4.47	8.16	9.95	ns, Max
Input to Pin 32	T_{MULT_P32}	4.37	7.99	9.74	ns, Max
Input to Pin 31	T_{MULT_P31}	4.28	7.82	9.53	ns, Max
Input to Pin 30	T_{MULT_P30}	4.18	7.65	9.33	ns, Max
Input to Pin 29	T_{MULT_P29}	4.08	7.48	9.12	ns, Max
Input to Pin 28	T_{MULT_P28}	3.99	7.31	8.91	ns, Max
Input to Pin 27	T_{MULT_P27}	3.89	7.14	8.70	ns, Max
Input to Pin 26	T_{MULT_P26}	3.79	6.97	8.50	ns, Max
Input to Pin 25	T_{MULT_P25}	3.69	6.80	8.29	ns, Max
Input to Pin 24	T_{MULT_P24}	3.60	6.63	8.08	ns, Max
Input to Pin 23	T_{MULT_P23}	3.50	6.46	7.88	ns, Max
Input to Pin 22	T_{MULT_P22}	3.40	6.29	7.67	ns, Max
Input to Pin 21	T_{MULT_P21}	3.31	6.12	7.46	ns, Max
Input to Pin 20	T_{MULT_P20}	3.21	5.95	7.26	ns, Max
Input to Pin 19	T_{MULT_P19}	3.11	5.78	7.05	ns, Max
Input to Pin 18	T_{MULT_P18}	3.02	5.61	6.84	ns, Max
Input to Pin 17	T_{MULT_P17}	2.92	5.44	6.63	ns, Max
Input to Pin 16	T_{MULT_P16}	2.82	5.27	6.43	ns, Max
Input to Pin 15	T_{MULT_P15}	2.72	5.10	6.22	ns, Max
Input to Pin 14	T_{MULT_P14}	2.63	4.93	6.01	ns, Max
Input to Pin 13	T_{MULT_P13}	2.53	4.76	5.81	ns, Max
Input to Pin 12	T_{MULT_P12}	2.43	4.59	5.60	ns, Max
Input to Pin 11	T_{MULT_P11}	2.34	4.42	5.39	ns, Max
Input to Pin 10	T_{MULT_P10}	2.24	4.25	5.19	ns, Max
Input to Pin 9	T_{MULT_P9}	2.14	4.08	4.98	ns, Max
Input to Pin 8	T_{MULT_P8}	2.05	3.91	4.77	ns, Max
Input to Pin 7	T_{MULT_P7}	1.95	3.74	4.56	ns, Max
Input to Pin 6	T_{MULT_P6}	1.85	3.57	4.36	ns, Max
Input to Pin 5	T_{MULT_P5}	1.75	3.40	4.15	ns, Max
Input to Pin 4	T_{MULT_P4}	1.66	3.23	3.94	ns, Max
Input to Pin 3	T_{MULT_P3}	1.56	3.06	3.74	ns, Max
Input to Pin 2	T_{MULT_P2}	1.46	2.89	3.53	ns, Max
Input to Pin 1	T_{MULT_P1}	1.37	2.72	3.32	ns, Max
Input to Pin 0	T_{MULT_P0}	1.27	2.55	3.12	ns, Max

Enhanced Multiplier Switching Characteristics

Table 26 and Table 27 provide timing information for enhanced Virtex-II multiplier blocks, available in stepping revisions of Virtex-II devices. For more information on stepping revisions, availability, and ordering instructions, see your local sales representative.

Table 26: **Enhanced Multiplier Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Propagation Delay to Output Pin					
Input to Pin 35	T_{MULT1_P35}	4.66	5.14	5.91	ns, Max
Input to Pin 34	T_{MULT1_P34}	4.57	5.03	5.79	ns, Max
Input to Pin 33	T_{MULT1_P33}	4.47	4.93	5.66	ns, Max
Input to Pin 32	T_{MULT1_P32}	4.37	4.82	5.54	ns, Max
Input to Pin 31	T_{MULT1_P31}	4.28	4.71	5.42	ns, Max
Input to Pin 30	T_{MULT1_P30}	4.18	4.61	5.29	ns, Max
Input to Pin 29	T_{MULT1_P29}	4.08	4.50	5.17	ns, Max
Input to Pin 28	T_{MULT1_P28}	3.99	4.39	5.05	ns, Max
Input to Pin 27	T_{MULT1_P27}	3.89	4.28	4.92	ns, Max
Input to Pin 26	T_{MULT1_P26}	3.79	4.18	4.80	ns, Max
Input to Pin 25	T_{MULT1_P25}	3.69	4.07	4.68	ns, Max
Input to Pin 24	T_{MULT1_P24}	3.60	3.96	4.56	ns, Max
Input to Pin 23	T_{MULT1_P23}	3.50	3.86	4.43	ns, Max
Input to Pin 22	T_{MULT1_P22}	3.40	3.75	4.31	ns, Max
Input to Pin 21	T_{MULT1_P21}	3.31	3.64	4.19	ns, Max
Input to Pin 20	T_{MULT1_P20}	3.21	3.54	4.06	ns, Max
Input to Pin 19	T_{MULT1_P19}	3.11	3.43	3.94	ns, Max
Input to Pin 18	T_{MULT1_P18}	3.02	3.32	3.82	ns, Max
Input to Pin 17	T_{MULT1_P17}	2.92	3.21	3.69	ns, Max
Input to Pin 16	T_{MULT1_P16}	2.82	3.11	3.57	ns, Max
Input to Pin 15	T_{MULT1_P15}	2.72	3.00	3.45	ns, Max
Input to Pin 14	T_{MULT1_P14}	2.63	2.89	3.33	ns, Max
Input to Pin 13	T_{MULT1_P13}	2.53	2.79	3.20	ns, Max
Input to Pin 12	T_{MULT1_P12}	2.43	2.68	3.08	ns, Max
Input to Pin 11	T_{MULT1_P11}	2.34	2.57	2.96	ns, Max
Input to Pin 10	T_{MULT1_P10}	2.24	2.47	2.83	ns, Max
Input to Pin 9	T_{MULT1_P9}	2.14	2.36	2.71	ns, Max
Input to Pin 8	T_{MULT1_P8}	2.05	2.25	2.59	ns, Max
Input to Pin 7	T_{MULT1_P7}	1.95	2.14	2.46	ns, Max
Input to Pin 6	T_{MULT1_P6}	1.85	2.04	2.34	ns, Max
Input to Pin 5	T_{MULT1_P5}	1.75	1.93	2.22	ns, Max
Input to Pin 4	T_{MULT1_P4}	1.66	1.82	2.10	ns, Max
Input to Pin 3	T_{MULT1_P3}	1.56	1.72	1.97	ns, Max
Input to Pin 2	T_{MULT1_P2}	1.46	1.61	1.85	ns, Max
Input to Pin 1	T_{MULT1_P1}	1.37	1.50	1.73	ns, Max
Input to Pin 0	T_{MULT1_P0}	1.27	1.40	1.60	ns, Max

Table 47: **Sample Window**

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
Sampling Error at Receiver Pins(1)	T_{SAMP}	XC2V40	500	500	550	ps
		XC2V80	500	500	550	ps
		XC2V250	500	500	550	ps
		XC2V500	500	500	550	ps
		XC2V1000	500	500	550	ps
		XC2V1500	500	500	550	ps
		XC2V2000	500	500	550	ps
		XC2V3000	500	500	550	ps
		XC2V4000	500	500	550	ps
		XC2V6000	500	500	550	ps
		XC2V8000		500	550	ps

Notes:
1. This parameter indicates the total sampling error of Virtex-II DDR input registers across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 and CLK180 DCM jitter
   - Worst-case Duty-Cycle Distortion - T_{DCD_CLK180}
   - DCM accuracy (phase offset)
   - DCM phase shift resolution.

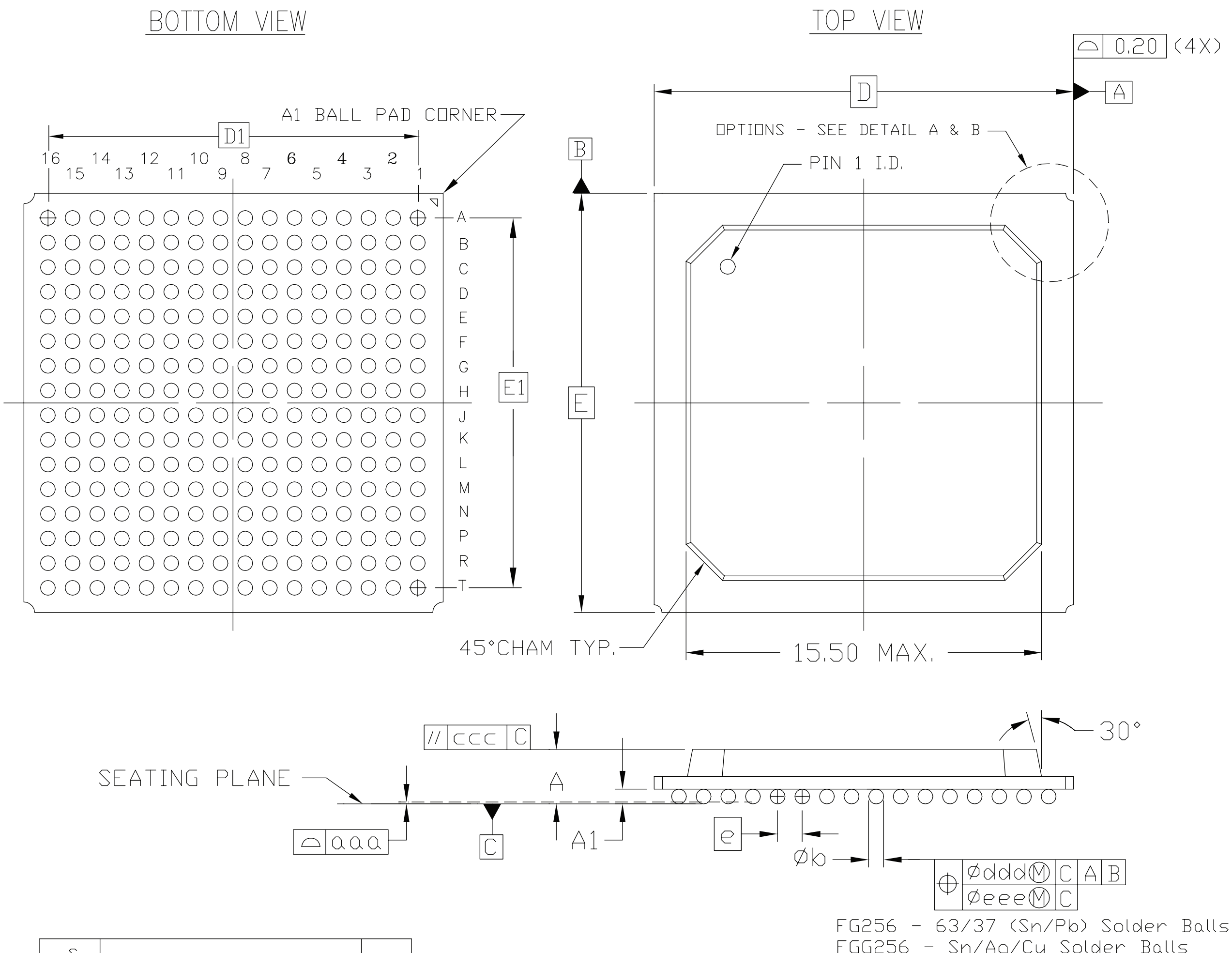
   These measurements do not include package or clock tree skew.

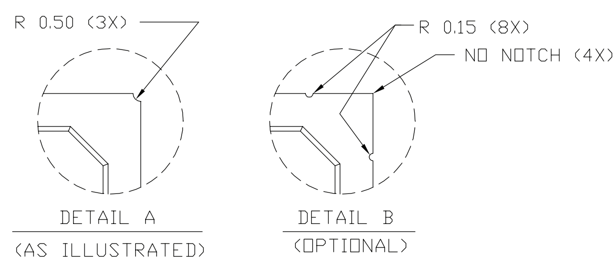
Table 48: **Pin-to-Pin Setup/Hold: Source-Synchronous Configuration**

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
Data Input Set-Up and Hold Times Relative to a Forwarded Clock Input Pin, Using DCM and Global Clock Buffer. For situations where clock and data inputs conform to different standards, adjust the setup and hold values accordingly using the values shown in IOB Input Switching Characteristics Standard Adjustments, page 11.						
No Delay Global Clock and IFF with DCM	T_{PSDCM}/ T_{PHDCM}	XC2V40	0.2/0.5	0.2/0.5	0.2/0.5	ns
		XC2V80	0.2/0.5	0.2/0.5	0.2/0.5	ns
		XC2V250	0.2/0.5	0.2/0.5	0.2/0.5	ns
		XC2V500	0.2/0.5	0.2/0.5	0.2/0.5	ns
		XC2V1000	0.2/0.5	0.2/0.5	0.2/0.5	ns
		XC2V1500	0.2/0.5	0.2/0.5	0.2/0.5	ns
		XC2V2000	0.2/0.5	0.2/0.5	0.2/0.5	ns
		XC2V3000	0.2/0.5	0.2/0.5	0.2/0.6	ns
		XC2V4000	0.2/0.5	0.2/0.6	0.2/0.6	ns
		XC2V6000	0.2/0.5	0.2/0.6	0.2/0.6	ns
		XC2V8000		0.2/0.6	0.2/0.7	ns

Notes:
1. IFF = Input Flip-Flop
2. The timing values were measured using the fine-phase adjustment feature of the DCM.
3. The worst-case duty-cycle distortion and DCM jitter on CLK0 and CLK180 is included in these measurements.

FG256/FGG256 Fine-Pitch BGA Package Specifications (1.00mm pitch)





SYMBOL	MILLIMETERS MIN.	MILLIMETERS NOM.	MILLIMETERS MAX.	NOTE
A	—	—	2.00	3
A_1	0.35	0.50	0.60	
D/E	17.00 BSC			
D_1/E_1	15.00 REF			
e	1.00 BSC			
Øb	0.50	0.60	0.70	
aaa	—	—	0.20	
ccc	—	—	0.35	
ddd	—	—	0.30	
eee	—	—	0.10	
M	16			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994.
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. NOMINAL DIMENSION IS TYPICALLY 1.60-1.73mm
4. CONFORMS TO JEDEC MS-034-AAF-1

256-BALL FINE PITCH BGA (FG256/FGG256)

Figure 2: **FG256/FGG256 Fine-Pitch BGA Package Specifications**

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

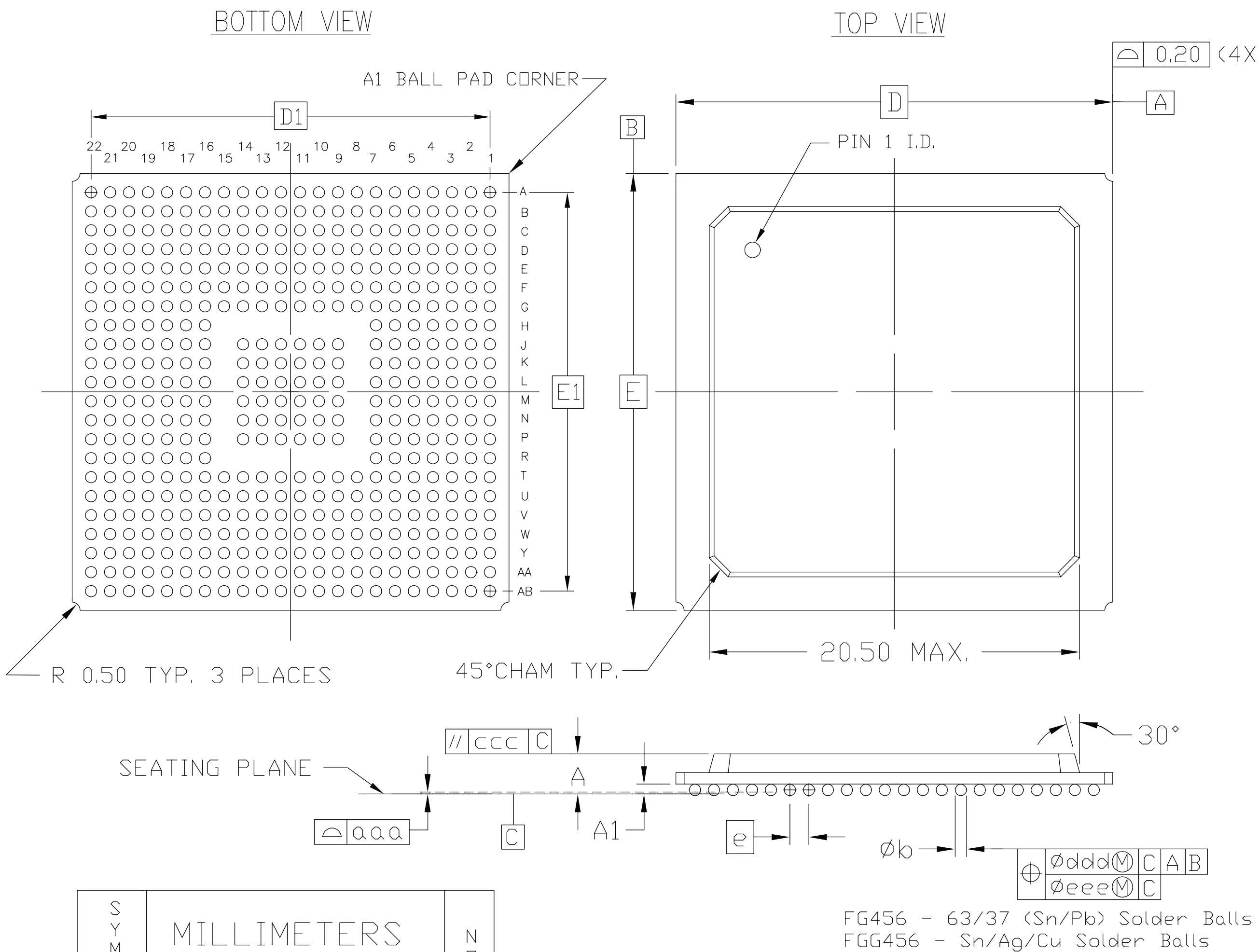
Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
7	VCCO_7	H6		
7	VCCO_7	G6		
NA	CCLK	Y19		
NA	PROG_B	A2		
NA	DONE	AB20		
NA	M0	AB2		
NA	M1	W3		
NA	M2	AB3		
NA	HSWAP_EN	B3		
NA	TCK	C19		
NA	TDI	D3		
NA	TDO	D20		
NA	TMS	B20		
NA	PWRDWN_B	AB21		
NA	DXN	D5		
NA	DXP	A3		
NA	VBATT	A21		
NA	RSVD	A20		
NA	VCCAUX	AB11		
NA	VCCAUX	AA22		
NA	VCCAUX	AA1		
NA	VCCAUX	M22		
NA	VCCAUX	L1		
NA	VCCAUX	B22		
NA	VCCAUX	B1		
NA	VCCAUX	A12		
NA	VCCINT	U17		
NA	VCCINT	U6		
NA	VCCINT	T16		
NA	VCCINT	T15		
NA	VCCINT	T8		
NA	VCCINT	T7		

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
NA	GND	M10		
NA	GND	M9		
NA	GND	L14		
NA	GND	L13		
NA	GND	L12		
NA	GND	L11		
NA	GND	L10		
NA	GND	L9		
NA	GND	K14		
NA	GND	K13		
NA	GND	K12		
NA	GND	K11		
NA	GND	K10		
NA	GND	K9		
NA	GND	J14		
NA	GND	J13		
NA	GND	J12		
NA	GND	J11		
NA	GND	J10		
NA	GND	J9		
NA	GND	D19		
NA	GND	D4		
NA	GND	C20		
NA	GND	C3		
NA	GND	B21		
NA	GND	B2		
NA	GND	A22		
NA	GND	A1		

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

FG456/FGG456 Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	—	—	2.60	3
A_1	0.35	0.50	0.60	
D/E	23.00 BSC			
D_1/E_1	21.00 REF			
e	1.00 BSC			
Øb	0.50	0.60	0.70	
aaa	—	—	0.20	
ccc	—	—	0.35	
ddd	—	—	0.30	
eee	—	—	0.10	
M	22			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. NOMINAL 'A' DIMENSION FOR 2-LAYER IS 2.03mm AND FOR 4-LAYER IS 2.20mm.
4. CONFORMS TO JEDEC MS-034-AAJ-1 (DEPOPULATED)

456-BALL FINE PITCH BGA (FG456/FGG456)

Figure 3: **FG456/FGG456 Fine-Pitch BGA Package Specifications**

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
NA	GND	L11		
NA	GND	L10		
NA	GND	K17		
NA	GND	K16		
NA	GND	K15		
NA	GND	K14		
NA	GND	K13		
NA	GND	K12		
NA	GND	K11		
NA	GND	K10		
NA	GND	F21		
NA	GND	F6		
NA	GND	E22		
NA	GND	E5		
NA	GND	D23		
NA	GND	D4		
NA	GND	C24		
NA	GND	C3		
NA	GND	B25		
NA	GND	B14		
NA	GND	B13		
NA	GND	B2		
NA	GND	A26		
NA	GND	A1		

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
NA	VCCAUX	P26
NA	VCCAUX	P2
NA	VCCAUX	C26
NA	VCCAUX	C2
NA	VCCAUX	B14
NA	VCCINT	V18
NA	VCCINT	V14
NA	VCCINT	V10
NA	VCCINT	U17
NA	VCCINT	U16
NA	VCCINT	U15
NA	VCCINT	U14
NA	VCCINT	U13
NA	VCCINT	U12
NA	VCCINT	U11
NA	VCCINT	T17
NA	VCCINT	T11
NA	VCCINT	R17
NA	VCCINT	R11
NA	VCCINT	P18
NA	VCCINT	P17
NA	VCCINT	P11
NA	VCCINT	P10
NA	VCCINT	N17
NA	VCCINT	N11
NA	VCCINT	M17
NA	VCCINT	M11
NA	VCCINT	L17
NA	VCCINT	L16
NA	VCCINT	L15
NA	VCCINT	L14
NA	VCCINT	L13
NA	VCCINT	L12
NA	VCCINT	L11
NA	VCCINT	K18
NA	VCCINT	K14

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
2	IO_L48N_2	J5		
2	IO_L48P_2	H5		
2	IO_L49N_2	J3		
2	IO_L49P_2	H3		
2	IO_L50N_2	K7		
2	IO_L50P_2	L7		
2	IO_L51N_2	J4		
2	IO_L51P_2/VREF_2	K4		
2	IO_L52N_2	K1		
2	IO_L52P_2	J1		
2	IO_L53N_2	L6		
2	IO_L53P_2	M6		
2	IO_L54N_2	L5		
2	IO_L54P_2	K5		
2	IO_L67N_2	L2	NC	
2	IO_L67P_2	K2	NC	
2	IO_L68N_2	M8	NC	
2	IO_L68P_2	N8	NC	
2	IO_L69N_2	L4	NC	
2	IO_L69P_2/VREF_2	M4	NC	
2	IO_L70N_2	M1	NC	
2	IO_L70P_2	L1	NC	
2	IO_L71N_2	M7	NC	
2	IO_L71P_2	N7	NC	
2	IO_L72N_2	M3	NC	
2	IO_L72P_2	L3	NC	
2	IO_L73N_2	N2	NC	NC
2	IO_L73P_2	M2	NC	NC
2	IO_L74N_2	N6	NC	NC
2	IO_L74P_2	P6	NC	NC
2	IO_L75N_2	N5	NC	NC
2	IO_L75P_2/VREF_2	N4	NC	NC
2	IO_L76N_2	P1	NC	NC
2	IO_L76P_2	N1	NC	NC
2	IO_L77N_2	P9	NC	NC
2	IO_L77P_2	R9	NC	NC
2	IO_L78N_2	R5	NC	NC

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
5	IO_L23N_5	AD20		
5	IO_L23P_5	AD21		
5	IO_L22N_5	AK25		
5	IO_L22P_5	AK24		
5	IO_L21N_5/VREF_5	AH24		
5	IO_L21P_5	AH25		
5	IO_L20N_5	AE21		
5	IO_L20P_5	AD22		
5	IO_L19N_5	AJ25		
5	IO_L19P_5	AJ24		
5	IO_L06N_5	AG25		
5	IO_L06P_5	AG24		
5	IO_L05N_5/VRP_5	AC20		
5	IO_L05P_5/VRN_5	AC21		
5	IO_L04N_5	AK26		
5	IO_L04P_5/VREF_5	AK27		
5	IO_L03N_5/D4/ALT_VRP_5	AH26		
5	IO_L03P_5/D5/ALT_VRN_5	AJ27		
5	IO_L02N_5/D6	AE22		
5	IO_L02P_5/D7	AE23		
5	IO_L01N_5/RDWR_B	AJ28		
5	IO_L01P_5/CS_B	AK29		
6	IO_L01P_6	AC22		
6	IO_L01N_6	AB23		
6	IO_L02P_6/VRN_6	AG28		
6	IO_L02N_6/VRP_6	AF28		
6	IO_L03P_6	AJ30		
6	IO_L03N_6/VREF_6	AH30		
6	IO_L04P_6	AD23		
6	IO_L04N_6	AC23		
6	IO_L05P_6	AF27		
6	IO_L05N_6	AE27		
6	IO_L06P_6	AG29		
6	IO_L06N_6	AH29		
6	IO_L19P_6	AE24		
6	IO_L19N_6	AD24		

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
3	IO_L83P_3	Y4	NC
3	IO_L82N_3	W11	NC
3	IO_L82P_3	V11	NC
3	IO_L81N_3/VREF_3	W8	NC
3	IO_L81P_3	Y8	NC
3	IO_L80N_3	W2	NC
3	IO_L80P_3	Y1	NC
3	IO_L79N_3	AA3	NC
3	IO_L79P_3	AB3	NC
3	IO_L78N_3	Y6	
3	IO_L78P_3	AA6	
3	IO_L77N_3	AA4	
3	IO_L77P_3	AB4	
3	IO_L76N_3	Y7	
3	IO_L76P_3	AA8	
3	IO_L75N_3/VREF_3	Y10	
3	IO_L75P_3	AA10	
3	IO_L74N_3	AA1	
3	IO_L74P_3	AB1	
3	IO_L73N_3	AA5	
3	IO_L73P_3	AB5	
3	IO_L72N_3	AA9	
3	IO_L72P_3	Y9	
3	IO_L71N_3	AA2	
3	IO_L71P_3	AB2	
3	IO_L70N_3	AB6	
3	IO_L70P_3	AC6	
3	IO_L69N_3/VREF_3	AD1	
3	IO_L69P_3	AC1	
3	IO_L68N_3	AC3	
3	IO_L68P_3	AD3	
3	IO_L67N_3	AC4	
3	IO_L67P_3	AD4	
3	IO_L54N_3	AB7	
3	IO_L54P_3	AC7	
3	IO_L53N_3	AC2	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
7	IO_L75N_7	R28	
7	IO_L74P_7	R26	
7	IO_L74N_7	P26	
7	IO_L73P_7	N31	
7	IO_L73N_7	P31	
7	IO_L72P_7	N30	
7	IO_L72N_7	P30	
7	IO_L71P_7	R25	
7	IO_L71N_7	P25	
7	IO_L70P_7	L34	
7	IO_L70N_7	M34	
7	IO_L69P_7/VREF_7	P29	
7	IO_L69N_7	N29	
7	IO_L68P_7	P27	
7	IO_L68N_7	N27	
7	IO_L67P_7	L32	
7	IO_L67N_7	M32	
7	IO_L54P_7	L31	
7	IO_L54N_7	M31	
7	IO_L53P_7	K29	
7	IO_L53N_7	L30	
7	IO_L52P_7	L33	
7	IO_L52N_7	M33	
7	IO_L51P_7/VREF_7	M29	
7	IO_L51N_7	L29	
7	IO_L50P_7	M28	
7	IO_L50N_7	N28	
7	IO_L49P_7	K30	
7	IO_L49N_7	K31	
7	IO_L48P_7	H32	
7	IO_L48N_7	J32	
7	IO_L47P_7	N26	
7	IO_L47N_7	M26	
7	IO_L46P_7	J33	
7	IO_L46N_7	K33	
7	IO_L45P_7/VREF_7	H33	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
NA	GND	P20	
NA	GND	P19	
NA	GND	P18	
NA	GND	P17	
NA	GND	P16	
NA	GND	P15	
NA	GND	P14	
NA	GND	P7	
NA	GND	M30	
NA	GND	M5	
NA	GND	K32	
NA	GND	K3	
NA	GND	J19	
NA	GND	J16	
NA	GND	H34	
NA	GND	H27	
NA	GND	H8	
NA	GND	H1	
NA	GND	G28	
NA	GND	G21	
NA	GND	G14	
NA	GND	G7	
NA	GND	F29	
NA	GND	F6	
NA	GND	E30	
NA	GND	E23	
NA	GND	E12	
NA	GND	E5	
NA	GND	D31	
NA	GND	D4	
NA	GND	C34	
NA	GND	C32	
NA	GND	C25	
NA	GND	C10	
NA	GND	C3	
NA	GND	C1	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
6	IO_L71N_6	AE39		
6	IO_L72P_6	AD36		
6	IO_L72N_6	AE36		
6	IO_L73P_6	AB29		
6	IO_L73N_6	AA29		
6	IO_L74P_6	AE38		
6	IO_L74N_6	AD38		
6	IO_L75P_6	AC33		
6	IO_L75N_6/VREF_6	AD33		
6	IO_L76P_6	AB30		
6	IO_L76N_6	AA30		
6	IO_L77P_6	AD37		
6	IO_L77N_6	AC37		
6	IO_L78P_6	AB34		
6	IO_L78N_6	AC34		
6	IO_L79P_6	AB31		
6	IO_L79N_6	AA31		
6	IO_L80P_6	AD39		
6	IO_L80N_6	AC39		
6	IO_L81P_6	AB35		
6	IO_L81N_6/VREF_6	AC35		
6	IO_L82P_6	AB32		
6	IO_L82N_6	AA32		
6	IO_L83P_6	AC38		
6	IO_L83N_6	AB38		
6	IO_L84P_6	AA33		
6	IO_L84N_6	AB33		
6	IO_L91P_6	Y28		
6	IO_L91N_6	Y29		
6	IO_L92P_6	AB39		
6	IO_L92N_6	AA39		
6	IO_L93P_6	AA36		
6	IO_L93N_6/VREF_6	AB36		
6	IO_L94P_6	Y31		
6	IO_L94N_6	Y32		
6	IO_L95P_6	AA37		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	GND	D4		
NA	GND	C39		
NA	GND	C38		
NA	GND	C37		
NA	GND	C3		
NA	GND	C2		
NA	GND	C1		
NA	GND	B39		
NA	GND	B38		
NA	GND	B37		
NA	GND	B29		
NA	GND	B11		
NA	GND	B3		
NA	GND	B2		
NA	GND	B1		
NA	GND	A38		
NA	GND	A37		
NA	GND	A20		
NA	GND	A3		
NA	GND	A2		

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
1	IO_L71P_1	B12	
1	IO_L70N_1	C13	
1	IO_L70P_1	C12	
1	IO_L69N_1/VREF_1	H13	
1	IO_L69P_1	H12	
1	IO_L68N_1	D12	
1	IO_L68P_1	D11	
1	IO_L67N_1	B11	
1	IO_L67P_1	B10	
1	IO_L54N_1	E12	
1	IO_L54P_1	E11	
1	IO_L53N_1	A11	
1	IO_L53P_1	A10	
1	IO_L52N_1	G12	
1	IO_L52P_1	G11	
1	IO_L51N_1/VREF_1	K13	
1	IO_L51P_1	K12	
1	IO_L50N_1	C11	
1	IO_L50P_1	C10	
1	IO_L49N_1	B9	
1	IO_L49P_1	B7	
1	IO_L30N_1	F11	NC
1	IO_L30P_1	F9	NC
1	IO_L29N_1	A9	NC
1	IO_L29P_1	A8	NC
1	IO_L27N_1/VREF_1	D9	NC
1	IO_L27P_1	D8	NC
1	IO_L26N_1	J12	NC
1	IO_L26P_1	J11	NC
1	IO_L25N_1	C9	NC
1	IO_L25P_1	C8	NC
1	IO_L24N_1	E10	
1	IO_L24P_1	E9	
1	IO_L23N_1	H11	
1	IO_L23P_1	H10	
1	IO_L22N_1	A7	
1	IO_L22P_1	A6	
1	IO_L21N_1/VREF_1	A5	