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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	128
Number of Logic Elements/Cells	-
Total RAM Bits	147456
Number of I/O	92
Number of Gates	80000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	144-TFBGA, CSPBGA
Supplier Device Package	144-LCSBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v80-5csg144i

Detailed Description

Input/Output Blocks (IOBs)

Virtex-II™ I/O blocks (IOBs) are provided in groups of two or four on the perimeter of each device. Each IOB can be used as input and/or output for single-ended I/Os. Two IOBs can be used as a differential pair. A differential pair is always connected to the same switch matrix, as shown in Figure 1.

IOB blocks are designed for high performances I/Os, supporting 19 single-ended standards, as well as differential signaling with LVDS, LDT, Bus LVDS, and LVPECL.

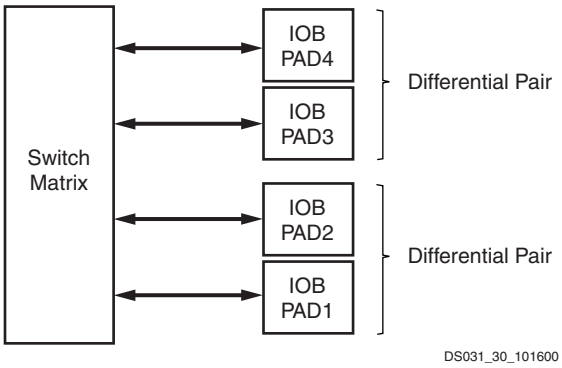


Figure 1: **Virtex-II Input/Output Tile**

Note: Differential I/Os must use the same clock.

Supported I/O Standards

Virtex-II IOB blocks feature SelectI/O-Ultra inputs and outputs that support a wide variety of I/O signaling standards. In addition to the internal supply voltage (V_{CCINT} = 1.5V), output driver supply voltage (V_{CCO}) is dependent on the I/O standard (see Table 1 and Table 2). An auxiliary supply voltage (V_{CCAUX} = 3.3 V) is required, regardless of the I/O standard used. For exact supply voltage absolute maximum ratings, see DC Input and Output Levels in Module 3.

All of the user IOBs have fixed-clamp diodes to V_{CCO} and to ground. As outputs, these IOBs are not compatible or compliant with 5V I/O standards. As inputs, these IOBs are not normally 5V tolerant, but can be used with 5V I/O standards when external current-limiting resistors are used. For more details, see the “5V Tolerant I/Os“ Tech Topic at www.xilinx.com.

Table 3 lists supported I/O standards with Digitally Controlled Impedance. See Digitally Controlled Impedance (DCI), page 8.

Table 1: **Supported Single-Ended I/O Standards**

IOSTANDARD Attribute	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Board Termination Voltage (V_{TT})
LVTTL	3.3	3.3	N/R(3)	N/R
LVCMOS33	3.3	3.3	N/R	N/R
LVCMOS25	2.5	2.5	N/R	N/R
LVCMOS18	1.8	1.8	N/R	N/R
LVCMOS15	1.5	1.5	N/R	N/R
PCI33_3	3.3	3.3	N/R	N/R
PCI66_3	3.3	3.3	N/R	N/R
PCI-X	3.3	3.3	N/R	N/R
GTL	Note (1)	Note (1)	0.8	1.2
GTLP	Note (1)	Note (1)	1.0	1.5
HSTL_I	1.5	N/R	0.75	0.75
HSTL_II	1.5	N/R	0.75	0.75
HSTL_III	1.5	N/R	0.9	1.5
HSTL_IV	1.5	N/R	0.9	1.5
HSTL_I_18	1.8	N/R	0.9	0.9
HSTL_II_18	1.8	N/R	0.9	0.9
HSTL_III _18	1.8	N/R	1.1	1.8
HSTL_IV_18	1.8	N/R	1.1	1.8
SSTL18_I(2)	1.8	N/R	0.9	0.9
SSTL18_II	1.8	N/R	0.9	0.9
SSTL2_I	2.5	N/R	1.25	1.25
SSTL2_II	2.5	N/R	1.25	1.25
SSTL3_I	3.3	N/R	1.5	1.5
SSTL3_II	3.3	N/R	1.5	1.5
AGP-2X/AGP	3.3	N/R	1.32	N/R

Notes:
1. V_{CCO} of GTL or GTLP should not be lower than the termination voltage or the voltage seen at the I/O pad. Example: If the pin High level is 1.5V, connect V_{CCO} to 1.5V.
2. SSTL18_I is not a JEDEC-supported standard.
3. N/R = no requirement.

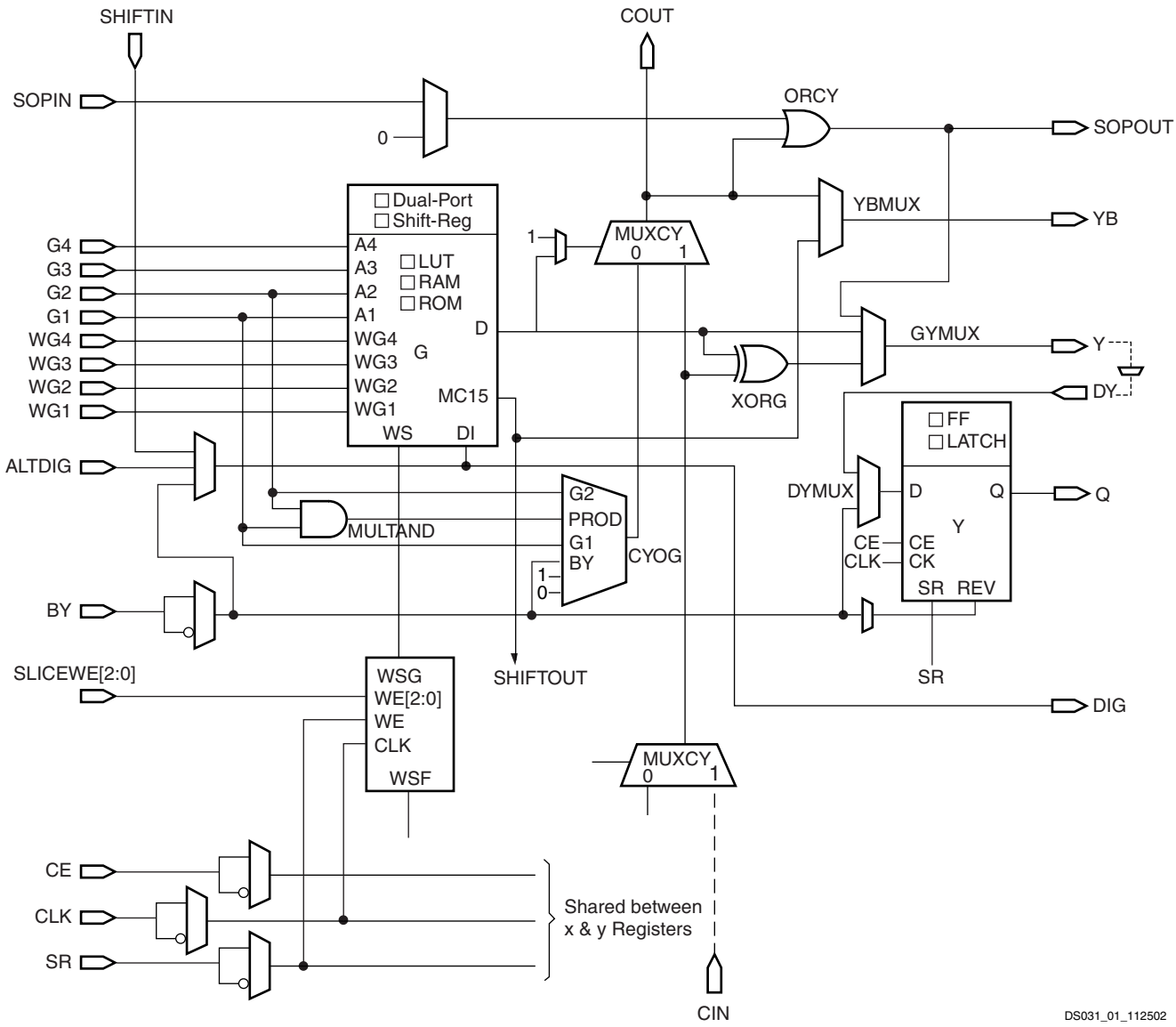


Figure 16: **Virtex-II Slice (Top Half)**

Extended LVDS DC Specifications (LVDSEXT_33 & LVDSEXT_25)

Table 9: **Extended LVDS DC Specifications**

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}			3.3 or 2.5		V
Output High voltage for Q and $\overline{Q}$	V_{OH}	R_T = 100 Ω across Q and $\overline{Q}$ signals			1.785	V
Output Low voltage for Q and $\overline{Q}$	V_{OL}	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.705			V
Differential output voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{ODIFF}	R_T = 100 Ω across Q and $\overline{Q}$ signals	440		820	mV
Output common-mode voltage	V_{OCM}	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.200	1.375	V
Differential input voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{IDIFF}	Common-mode input voltage = 1.25 V	100	350	N/A	mV
Input common-mode voltage	V_{ICM}	Differential input voltage = ±350 mV	0.2	1.25	V_{CCO} – 0.5	V

LVPECL DC Specifications

These values are valid when driving a 100 Ω differential load only, i.e., a 100 Ω resistor between the two receiver pins. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. Table 10 summarizes the DC output specifications of LVPECL. For more information on using LVPECL, see the *Virtex-II User Guide*.

Table 10: **LVPECL DC Specifications**

DC Parameter	Min	Max	Min	Max	Min	Max	Units
V_{CCO}	3.0		3.3		3.6		V
V_{OH}	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{OL}	0.96	1.27	1.06	1.43	1.30	1.57	V
V_{IH}	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	0.86	2.125	0.86	2.125	0.86	2.125	V
Differential Input Voltage	0.3	–	0.3	–	0.3	–	V

Table 14: **IOB Input Switching Characteristics *(Continued)***

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
Propagation Delays						
Pad to output IQ via transparent latch, no delay	T_{IOPLI}	All	0.83	0.91	1.05	ns, Max
Pad to output IQ via transparent latch, with delay	T_{IOPLID}	XC2V40	3.23	3.55	4.09	ns, Max
		XC2V80	3.23	3.55	4.09	ns, Max
		XC2V250	3.23	3.55	4.09	ns, Max
		XC2V500	3.23	3.55	4.09	ns, Max
		XC2V1000	3.23	3.55	4.09	ns, Max
		XC2V1500	3.23	3.55	4.09	ns, Max
		XC2V2000	3.23	3.55	4.09	ns, Max
		XC2V3000	3.32	3.65	4.20	ns, Max
		XC2V4000	3.32	3.65	4.20	ns, Max
		XC2V6000	3.60	3.95	4.55	ns, Max
		XC2V8000		3.95	4.55	ns, Max
Clock CLK to output IQ	T_{IOCKIQ}	All		0.67	0.77	ns, Max
Setup and Hold Times With Respect to Clock at IOB Input Register						
Pad, no delay	T_{IOPICK}/T_{IOICKP}	All	0.84/–0.36	0.92/–0.39	1.06/–0.45	ns, Min
Pad, with delay	$T_{IOPICKD}/T_{IOICKPD}$	XC2V40	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V80	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V250	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V500	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V1000	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V1500	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V2000	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V3000	3.33/–2.10	3.67/–2.31	4.22/–2.66	ns, Min
		XC2V4000	3.33/–2.10	3.67/–2.31	4.22/–2.66	ns, Min
		XC2V6000	3.61/–2.29	3.97/–2.52	4.56/–2.90	ns, Min
		XC2V8000		3.97/–2.52	4.56/–2.90	ns, Min
ICE input	$T_{IOICECK}/T_{IOCKICE}$	All		0.21/ 0.04	0.24/ 0.04	ns, Min
SR input (IFF, synchronous)	$T_{IOSRCKI}$	All	0.27	0.30	0.34	ns, Min
Set/Reset Delays						
SR input to IQ (asynchronous)	T_{IOSRIQ}	All	1.11	1.22	1.40	ns, Max
GSR to output IQ	T_{GSRQ}	All	5.44	5.98	6.88	ns, Max

Notes:
1. Input timing for LVTTL is measured at 1.4 V. For other I/O standards, see Table 18.

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
2	IO_L45N_2	H19		
2	IO_L45P_2/VREF_2	H20		
2	IO_L46N_2	H21		
2	IO_L46P_2	H22		
2	IO_L48N_2	J17		
2	IO_L48P_2	J18		
2	IO_L49N_2	J19	NC	
2	IO_L49P_2	J20	NC	
2	IO_L51N_2	J21	NC	
2	IO_L51P_2/VREF_2	J22	NC	
2	IO_L52N_2	K17	NC	
2	IO_L52P_2	K18	NC	
2	IO_L54N_2	K19	NC	
2	IO_L54P_2	K20	NC	
2	IO_L91N_2	K21		
2	IO_L91P_2	K22		
2	IO_L93N_2	L17		
2	IO_L93P_2/VREF_2	L18		
2	IO_L94N_2	L19		
2	IO_L94P_2	L20		
2	IO_L96N_2	L21		
2	IO_L96P_2	L22		
3	IO_L96N_3	M21		
3	IO_L96P_3	M20		
3	IO_L94N_3	M19		
3	IO_L94P_3	M18		
3	IO_L93N_3/VREF_3	M17		
3	IO_L93P_3	N17		
3	IO_L91N_3	N22		
3	IO_L91P_3	N21		
3	IO_L54N_3	N20	NC	
3	IO_L54P_3	N19	NC	
3	IO_L52N_3	N18	NC	

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
5	IO_L06P_5	W6		
5	IO_L05N_5/VRP_5	V7		
5	IO_L05P_5/VRN_5	V6		
5	IO_L04N_5	AB5		
5	IO_L04P_5/VREF_5	AA5		
5	IO_L03N_5/D4/ALT_VRP_5	Y5		
5	IO_L03P_5/D5/ALT_VRN_5	W5		
5	IO_L02N_5/D6	AB4		
5	IO_L02P_5/D7	AA4		
5	IO_L01N_5/RDWR_B	Y4		
5	IO_L01P_5/CS_B	AA3		
6	IO_L01P_6	V5		
6	IO_L01N_6	U5		
6	IO_L02P_6/VRN_6	Y2		
6	IO_L02N_6/VRP_6	Y1		
6	IO_L03P_6	V4		
6	IO_L03N_6/VREF_6	V3		
6	IO_L04P_6	W2		
6	IO_L04N_6	W1		
6	IO_L06P_6	U4		
6	IO_L06N_6	U3		
6	IO_L19P_6	V2	NC	NC
6	IO_L19N_6	V1	NC	NC
6	IO_L21P_6	U2	NC	NC
6	IO_L21N_6/VREF_6	U1	NC	NC
6	IO_L22P_6	T5	NC	NC
6	IO_L22N_6	R5	NC	NC
6	IO_L24P_6	T4	NC	NC
6	IO_L24N_6	T3	NC	NC
6	IO_L43P_6	T2		
6	IO_L43N_6	T1		
6	IO_L45P_6	R4		
6	IO_L45N_6/VREF_6	R3		

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
1	IO_L19N_1	E20		
1	IO_L19P_1	F20		
1	IO_L06N_1	B21		
1	IO_L06P_1	B22		
1	IO_L05N_1	A22		
1	IO_L05P_1	A23		
1	IO_L04N_1	C21		
1	IO_L04P_1/VREF_1	D21		
1	IO_L03N_1/VRP_1	C20		
1	IO_L03P_1/VRN_1	D20		
1	IO_L02N_1	A24		
1	IO_L02P_1	A25		
1	IO_L01N_1	B23		
1	IO_L01P_1	B24		
2	IO_L01N_2	B26		
2	IO_L01P_2	C26		
2	IO_L02N_2/VRP_2	G20		
2	IO_L02P_2/VRN_2	H20		
2	IO_L03N_2	C25		
2	IO_L03P_2/VREF_2	D25		
2	IO_L04N_2	E23		
2	IO_L04P_2	E24		
2	IO_L06N_2	G21		
2	IO_L06P_2	G22		
2	IO_L19N_2	D26		
2	IO_L19P_2	E26		
2	IO_L21N_2	F23		
2	IO_L21P_2/VREF_2	F24		
2	IO_L22N_2	E25		
2	IO_L22P_2	F25		
2	IO_L24N_2	H22		
2	IO_L24P_2	H21		
2	IO_L25N_2	G23	NC	NC
2	IO_L25P_2	G24	NC	NC
2	IO_L43N_2	F26		
2	IO_L43P_2	G26		

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
NA	GND	R12		
NA	GND	R11		
NA	GND	R10		
NA	GND	P25		
NA	GND	P17		
NA	GND	P16		
NA	GND	P15		
NA	GND	P14		
NA	GND	P13		
NA	GND	P12		
NA	GND	P11		
NA	GND	P10		
NA	GND	P2		
NA	GND	N25		
NA	GND	N17		
NA	GND	N16		
NA	GND	N15		
NA	GND	N14		
NA	GND	N13		
NA	GND	N12		
NA	GND	N11		
NA	GND	N10		
NA	GND	N2		
NA	GND	M17		
NA	GND	M16		
NA	GND	M15		
NA	GND	M14		
NA	GND	M13		
NA	GND	M12		
NA	GND	M11		
NA	GND	M10		
NA	GND	L17		
NA	GND	L16		
NA	GND	L15		
NA	GND	L14		
NA	GND	L13		
NA	GND	L12		

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
6	IO_L91N_6	P4		
6	IO_L93P_6	N4		
6	IO_L93N_6/VREF_6	N3		
6	IO_L94P_6	N6		
6	IO_L94N_6	N5		
6	IO_L96P_6	N8		
6	IO_L96N_6	N7		
7	IO_L96P_7	N2		
7	IO_L96N_7	M1		
7	IO_L94P_7	M2		
7	IO_L94N_7	M3		
7	IO_L93P_7/VREF_7	M4		
7	IO_L93N_7	M5		
7	IO_L91P_7	M6		
7	IO_L91N_7	M7		
7	IO_L73P_7	M8	NC	NC
7	IO_L73N_7	L8	NC	NC
7	IO_L72P_7	L1	NC	
7	IO_L72N_7	K1	NC	
7	IO_L70P_7	K2	NC	
7	IO_L70N_7	K3	NC	
7	IO_L69P_7/VREF_7	L3	NC	
7	IO_L69N_7	L4	NC	
7	IO_L67P_7	L5	NC	
7	IO_L67N_7	L7	NC	
7	IO_L54P_7	J1		
7	IO_L54N_7	H1		
7	IO_L52P_7	J2		
7	IO_L52N_7	J3		
7	IO_L51P_7/VREF_7	J4		
7	IO_L51N_7	J5		
7	IO_L49P_7	K5		
7	IO_L49N_7	K6		
7	IO_L48P_7	F1		
7	IO_L48N_7	F2		

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
5	IO_L52N_5	AC10
5	IO_L52P_5	AB10
5	IO_L51N_5/VREF_5	Y9
5	IO_L51P_5	Y10
5	IO_L49N_5	AG9
5	IO_L49P_5	AG8
5	IO_L30N_5	AF9
5	IO_L30P_5	AE9
5	IO_L28N_5	AD9
5	IO_L28P_5	AC9
5	IO_L27N_5/VREF_5	AB9
5	IO_L27P_5	AA9
5	IO_L25N_5	AE8
5	IO_L25P_5	AE7
5	IO_L24N_5	AD8
5	IO_L24P_5	AC8
5	IO_L22N_5	AB8
5	IO_L22P_5	AA8
5	IO_L21N_5/VREF_5	AG7
5	IO_L21P_5	AF7
5	IO_L19N_5	AC7
5	IO_L19P_5	AB7
5	IO_L06N_5	AG6
5	IO_L06P_5	AF6
5	IO_L05N_5/VRP_5	AE6
5	IO_L05P_5/VRN_5	AD6
5	IO_L04N_5	AG5
5	IO_L04P_5/VREF_5	AF5
5	IO_L03N_5/D4/ALT_VRP_5	AE5
5	IO_L03P_5/D5/ALT_VRN_5	AD5
5	IO_L02N_5/D6	AG4
5	IO_L02P_5/D7	AF4
5	IO_L01N_5/RDWR_B	AG3
5	IO_L01P_5/CS_B	AF3
6	IO_L01P_6	AE1

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
1	IO_L68P_1	G12	NC	
1	IO_L67N_1	A9	NC	
1	IO_L67P_1	A10	NC	
1	IO_L54N_1	E10		
1	IO_L54P_1	E11		
1	IO_L53N_1	H12		
1	IO_L53P_1	H11		
1	IO_L52N_1	D9		
1	IO_L52P_1	D10		
1	IO_L51N_1/VREF_1	C9		
1	IO_L51P_1	C8		
1	IO_L50N_1	F11		
1	IO_L50P_1	F10		
1	IO_L49N_1	B8		
1	IO_L49P_1	B9		
1	IO_L24N_1	E8		
1	IO_L24P_1	E9		
1	IO_L23N_1	G11		
1	IO_L23P_1	H10		
1	IO_L22N_1	B7		
1	IO_L22P_1	A7		
1	IO_L21N_1/VREF_1	D8		
1	IO_L21P_1	E7		
1	IO_L20N_1	G10		
1	IO_L20P_1	G9		
1	IO_L19N_1	A5		
1	IO_L19P_1	A6		
1	IO_L06N_1	C6		
1	IO_L06P_1	C7		
1	IO_L05N_1	F9		
1	IO_L05P_1	G8		
1	IO_L04N_1	B6		
1	IO_L04P_1/VREF_1	C5		
1	IO_L03N_1/VRP_1	D7		
1	IO_L03P_1/VRN_1	D6		
1	IO_L02N_1	F8		
1	IO_L02P_1	F7		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
3	IO_L24N_3	AC8		
3	IO_L24P_3	AB8		
3	IO_L23N_3	AE2		
3	IO_L23P_3	AF3		
3	IO_L22N_3	AD3		
3	IO_L22P_3	AE3		
3	IO_L21N_3/VREF_3	AD6		
3	IO_L21P_3	AD7		
3	IO_L20N_3	AF1		
3	IO_L20P_3	AG1		
3	IO_L19N_3	AD4		
3	IO_L19P_3	AE4		
3	IO_L06N_3	AD8		
3	IO_L06P_3	AE7		
3	IO_L05N_3	AG2		
3	IO_L05P_3	AH2		
3	IO_L04N_3	AD5		
3	IO_L04P_3	AE5		
3	IO_L03N_3/VREF_3	AC9		
3	IO_L03P_3	AD9		
3	IO_L02N_3/VRP_3	AH1		
3	IO_L02P_3/VRN_3	AJ1		
3	IO_L01N_3	AF4		
3	IO_L01P_3	AG3		
4	IO_L01N_4/BUSY/DOUT(1)	AK2		
4	IO_L01P_4/INIT_B	AJ3		
4	IO_L02N_4/D0/DIN(1)	AE8		
4	IO_L02P_4/D1	AF9		
4	IO_L03N_4/D2/ALT_VRP_4	AH5		
4	IO_L03P_4/D3/ALT_VRN_4	AH6		
4	IO_L04N_4/VREF_4	AJ4		
4	IO_L04P_4	AK4		
4	IO_L05N_4/VRP_4	AC10		
4	IO_L05P_4/VRN_4	AC11		
4	IO_L06N_4	AH7		
4	IO_L06P_4	AG6		

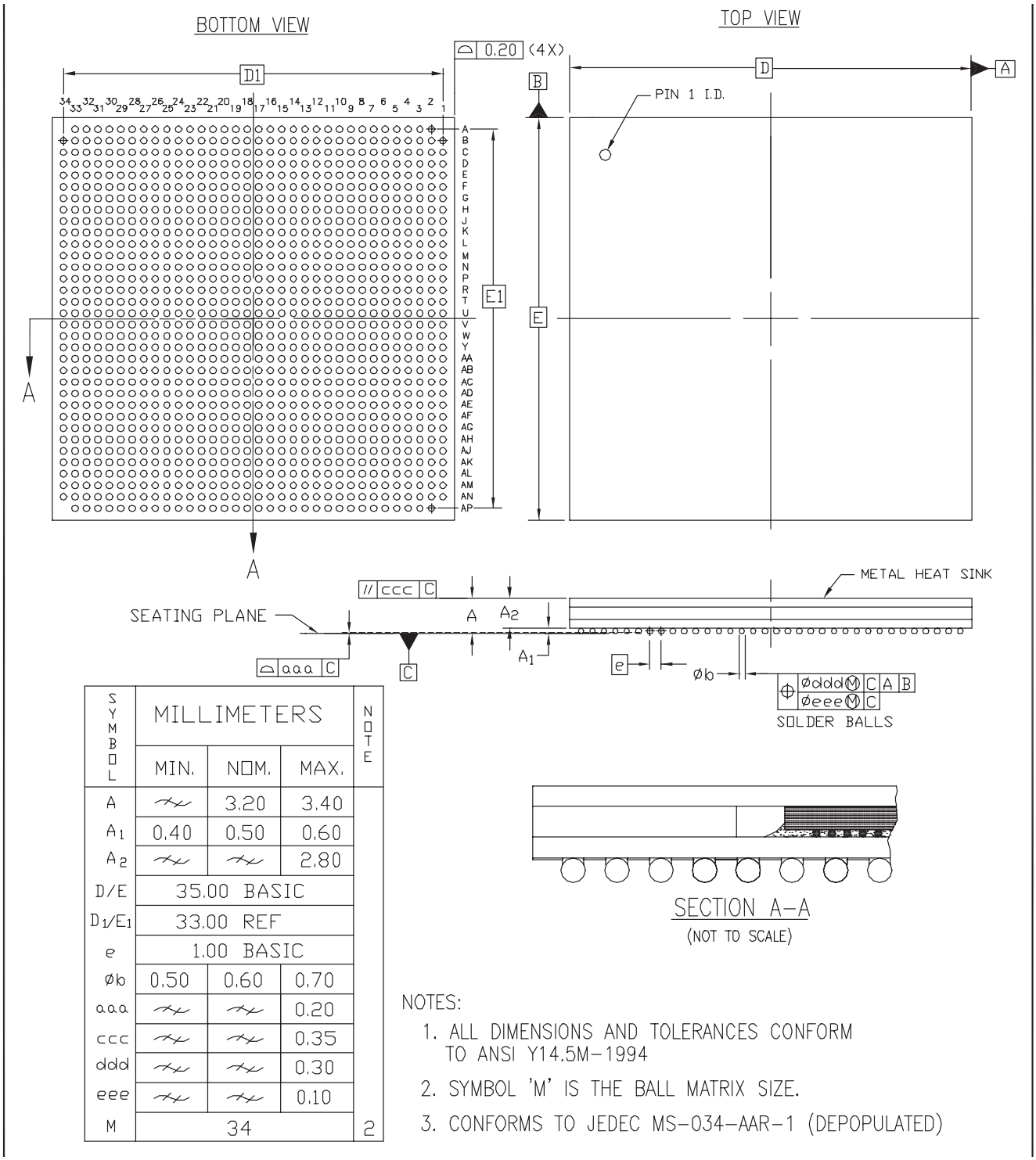
Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
3	IO_L83P_3	Y4	NC
3	IO_L82N_3	W11	NC
3	IO_L82P_3	V11	NC
3	IO_L81N_3/VREF_3	W8	NC
3	IO_L81P_3	Y8	NC
3	IO_L80N_3	W2	NC
3	IO_L80P_3	Y1	NC
3	IO_L79N_3	AA3	NC
3	IO_L79P_3	AB3	NC
3	IO_L78N_3	Y6	
3	IO_L78P_3	AA6	
3	IO_L77N_3	AA4	
3	IO_L77P_3	AB4	
3	IO_L76N_3	Y7	
3	IO_L76P_3	AA8	
3	IO_L75N_3/VREF_3	Y10	
3	IO_L75P_3	AA10	
3	IO_L74N_3	AA1	
3	IO_L74P_3	AB1	
3	IO_L73N_3	AA5	
3	IO_L73P_3	AB5	
3	IO_L72N_3	AA9	
3	IO_L72P_3	Y9	
3	IO_L71N_3	AA2	
3	IO_L71P_3	AB2	
3	IO_L70N_3	AB6	
3	IO_L70P_3	AC6	
3	IO_L69N_3/VREF_3	AD1	
3	IO_L69P_3	AC1	
3	IO_L68N_3	AC3	
3	IO_L68P_3	AD3	
3	IO_L67N_3	AC4	
3	IO_L67P_3	AD4	
3	IO_L54N_3	AB7	
3	IO_L54P_3	AC7	
3	IO_L53N_3	AC2	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
4	IO_L91N_4/VREF_4	AL16	
4	IO_L91P_4	AL17	
4	IO_L92N_4	AJ17	
4	IO_L92P_4	AJ16	
4	IO_L93N_4	AM15	
4	IO_L93P_4	AM14	
4	IO_L94N_4/VREF_4	AM16	
4	IO_L94P_4	AM17	
4	IO_L95N_4/GCLK3S	AF17	
4	IO_L95P_4/GCLK2P	AG17	
4	IO_L96N_4/GCLK1S	AK16	
4	IO_L96P_4/GCLK0P	AK17	
5	IO_L96N_5/GCLK7S	AK18	
5	IO_L96P_5/GCLK6P	AK19	
5	IO_L95N_5/GCLK5S	AG18	
5	IO_L95P_5/GCLK4P	AF18	
5	IO_L94N_5	AL18	
5	IO_L94P_5/VREF_5	AL19	
5	IO_L93N_5	AJ19	
5	IO_L93P_5	AJ18	
5	IO_L92N_5	AH19	
5	IO_L92P_5	AH18	
5	IO_L91N_5	AM19	
5	IO_L91P_5/VREF_5	AM20	
5	IO_L84N_5	AL21	NC
5	IO_L84P_5	AL20	NC
5	IO_L83N_5	AM22	NC
5	IO_L83P_5	AM21	NC
5	IO_L82N_5	AN18	NC
5	IO_L82P_5	AP18	NC
5	IO_L81N_5/VREF_5	AP20	NC
5	IO_L81P_5	AN19	NC
5	IO_L80N_5	AE18	NC
5	IO_L80P_5	AE19	NC
5	IO_L79N_5	AP22	NC

FF1152 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A		3.20	3.40	
A_1	0.40	0.50	0.60	
A_2			2.80	
D/E	35.00 BASIC			
D_1/E_1	33.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.35	
ddd			0.30	
eee			0.10	
M	34			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAR–1 (DEPOPULATED)

Figure 8: **FF1152 Flip-Chip Fine-Pitch BGA Package Specifications**

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
0	IO_L76P_0	C24		
0	IO_L77N_0	K22		
0	IO_L77P_0	K21		
0	IO_L78N_0	E22		
0	IO_L78P_0	E23		
0	IO_L79N_0	B23		
0	IO_L79P_0	B24		
0	IO_L80N_0	J22		
0	IO_L80P_0	J21		
0	IO_L81N_0	G21		
0	IO_L81P_0/VREF_0	G22		
0	IO_L82N_0	A23		
0	IO_L82P_0	A24		
0	IO_L83N_0	H22		
0	IO_L83P_0	H21		
0	IO_L84N_0	F21		
0	IO_L84P_0	F22		
0	IO_L91N_0/VREF_0	B21		
0	IO_L91P_0	B22		
0	IO_L92N_0	L20		
0	IO_L92P_0	M20		
0	IO_L93N_0	E21		
0	IO_L93P_0	D22		
0	IO_L94N_0/VREF_0	A21		
0	IO_L94P_0	A22		
0	IO_L95N_0/GCLK7P	H20		
0	IO_L95P_0/GCLK6S	J20		
0	IO_L96N_0/GCLK5P	C21		
0	IO_L96P_0/GCLK4S	D21		
1	IO_L96N_1/GCLK3P	F19		
1	IO_L96P_1/GCLK2S	F20		
1	IO_L95N_1/GCLK1P	H19		
1	IO_L95P_1/GCLK0S	H18		
1	IO_L94N_1	C19		
1	IO_L94P_1/VREF_1	C20		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
1	IO_L33N_1/VREF_1	D11	NC	
1	IO_L33P_1	D12	NC	
1	IO_L32N_1	H14	NC	
1	IO_L32P_1	H13	NC	
1	IO_L31N_1	A8	NC	
1	IO_L31P_1	A9	NC	
1	IO_L30N_1	F11		
1	IO_L30P_1	F12		
1	IO_L29N_1	K14		
1	IO_L29P_1	L14		
1	IO_L28N_1	C9		
1	IO_L28P_1	C10		
1	IO_L27N_1/VREF_1	G11		
1	IO_L27P_1	G12		
1	IO_L26N_1	M15		
1	IO_L26P_1	M14		
1	IO_L25N_1	B7		
1	IO_L25P_1	B8		
1	IO_L24N_1	D9		
1	IO_L24P_1	D10		
1	IO_L23N_1	J13		
1	IO_L23P_1	J12		
1	IO_L22N_1	A6		
1	IO_L22P_1	A7		
1	IO_L21N_1/VREF_1	E9		
1	IO_L21P_1	E10		
1	IO_L20N_1	D8		
1	IO_L20P_1	E7		
1	IO_L19N_1	C7		
1	IO_L19P_1	C8		
1	IO_L12N_1	F9	NC	
1	IO_L12P_1	F10	NC	
1	IO_L11N_1	H12	NC	
1	IO_L11P_1	H11	NC	
1	IO_L10N_1	B5	NC	
1	IO_L10P_1	B6	NC	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	VCCINT	AE18		
NA	VCCINT	AE17		
NA	VCCINT	AE16		
NA	VCCINT	AE15		
NA	VCCINT	AD25		
NA	VCCINT	AD24		
NA	VCCINT	AD16		
NA	VCCINT	AD15		
NA	VCCINT	AC25		
NA	VCCINT	AC15		
NA	VCCINT	AB25		
NA	VCCINT	AB15		
NA	VCCINT	AA25		
NA	VCCINT	AA15		
NA	VCCINT	Y27		
NA	VCCINT	Y26		
NA	VCCINT	Y25		
NA	VCCINT	Y15		
NA	VCCINT	Y14		
NA	VCCINT	Y13		
NA	VCCINT	W25		
NA	VCCINT	W15		
NA	VCCINT	V25		
NA	VCCINT	V15		
NA	VCCINT	U25		
NA	VCCINT	U15		
NA	VCCINT	T25		
NA	VCCINT	T24		
NA	VCCINT	T16		
NA	VCCINT	T15		
NA	VCCINT	R25		
NA	VCCINT	R24		
NA	VCCINT	R23		
NA	VCCINT	R22		
NA	VCCINT	R21		
NA	VCCINT	R20		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	GND	D4		
NA	GND	C39		
NA	GND	C38		
NA	GND	C37		
NA	GND	C3		
NA	GND	C2		
NA	GND	C1		
NA	GND	B39		
NA	GND	B38		
NA	GND	B37		
NA	GND	B29		
NA	GND	B11		
NA	GND	B3		
NA	GND	B2		
NA	GND	B1		
NA	GND	A38		
NA	GND	A37		
NA	GND	A20		
NA	GND	A3		
NA	GND	A2		

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
3	IO_L50P_3	AB3	
3	IO_L49N_3	AB5	
3	IO_L49P_3	AC5	
3	IO_L48N_3	W9	
3	IO_L48P_3	Y9	
3	IO_L47N_3	AC1	
3	IO_L47P_3	AD1	
3	IO_L46N_3	AC3	
3	IO_L46P_3	AD3	
3	IO_L45N_3/VREF_3	Y8	
3	IO_L45P_3	AA8	
3	IO_L44N_3	AC2	
3	IO_L44P_3	AE2	
3	IO_L43N_3	AB7	
3	IO_L43P_3	AC7	
3	IO_L27N_3/VREF_3	Y10	NC
3	IO_L27P_3	AA10	NC
3	IO_L25N_3	AE1	NC
3	IO_L25P_3	AF1	NC
3	IO_L24N_3	AF2	
3	IO_L24P_3	AG2	
3	IO_L23N_3	AA9	
3	IO_L23P_3	AB9	
3	IO_L22N_3	AD4	
3	IO_L22P_3	AE4	
3	IO_L21N_3/VREF_3	AD5	
3	IO_L21P_3	AE5	
3	IO_L20N_3	AB8	
3	IO_L20P_3	AC8	
3	IO_L19N_3	AG1	
3	IO_L19P_3	AH1	
3	IO_L06N_3	AF4	
3	IO_L06P_3	AG4	
3	IO_L05N_3	AB10	
3	IO_L05P_3	AB11	
3	IO_L04N_3	AF3	
3	IO_L04P_3	AG3	
3	IO_L03N_3/VREF_3	AD6	