AMD Xilinx - XC2V80-5FGG256C Datasheet

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	128
Number of Logic Elements/Cells	-
Total RAM Bits	147456
Number of I/O	120
Number of Gates	80000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v80-5fgg256c

Digitally Controlled Impedance (DCI)

Today's chip output signals with fast edge rates require termination to prevent reflections and maintain signal integrity. High pin count packages (especially ball grid arrays) can not accommodate external termination resistors.

Virtex-II XCITE DCI provides controlled impedance drivers and on-chip termination for single-ended and differential I/Os. This eliminates the need for external resistors, and improves signal integrity. The DCI feature can be used on any IOB by selecting one of the DCI I/O standards.

When applied to inputs, DCI provides input parallel termination. When applied to outputs, DCI provides controlled impedance drivers (series termination) or output parallel termination.

DCI operates independently on each I/O bank. When a DCI I/O standard is used in a particular I/O bank, external reference resistors must be connected to two dual-function pins on the bank. These resistors, voltage reference of N transistor (VRN) and the voltage reference of P transistor (VRP) are shown in Figure 9.

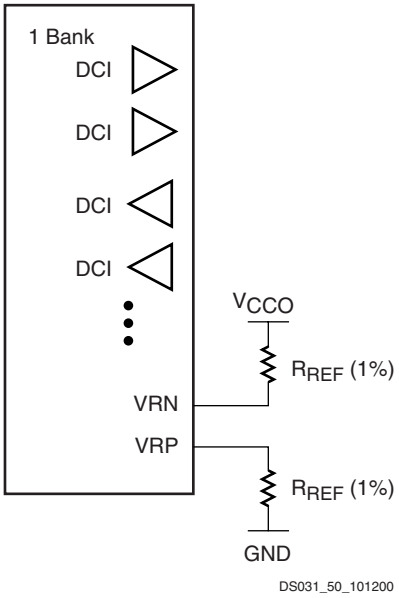


Figure 9: **DCI in a Virtex-II Bank**

When used with a terminated I/O standard, the value of resistors are specified by the standard (typically 50Ω). When used with a controlled impedance driver, the resistors set the output impedance of the driver within the specified range (25Ω to 100Ω). For all series and parallel terminations listed in Table 6 and Table 7, the reference resistors must have the same value for any given bank. One percent resistors are recommended.

The DCI system adjusts the I/O impedance to match the two external reference resistors, or half of the reference resistors, and compensates for impedance changes due to voltage and/or temperature fluctuations. The adjustment is done by turning parallel transistors in the IOB on or off.

Controlled Impedance Drivers (Series Term.)

DCI can be used to provide a buffer with a controlled output impedance. It is desirable for this output impedance to match the transmission line impedance (Z_0). Virtex-II input buffers also support LVDCI and LVDCI_DV2 I/O standards.

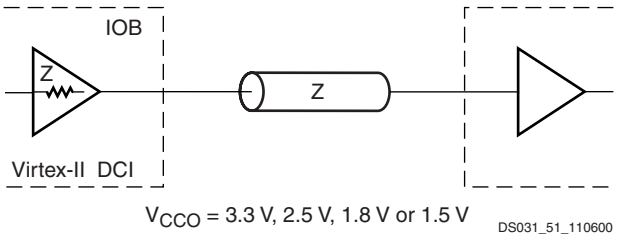


Figure 10: **Internal Series Termination**

Table 6: **SelectI/O-Ultra Controlled Impedance Buffers**

V_{CCO}	DCI	DCI Half Impedance
3.3 V	LVDCI_33	LVDCI_DV2_33
2.5 V	LVDCI_25	LVDCI_DV2_25
1.8 V	LVDCI_18	LVDCI_DV2_18
1.5 V	LVDCI_15	LVDCI_DV2_15

Controlled Impedance Drivers (Parallel)

DCI also provides on-chip termination for SSTL3, SSTL2, HSTL (Class I, II, III, or IV), and GTL/GTLP receivers or transmitters on bidirectional lines.

Table 7 and Table 8 list the on-chip parallel terminations available in Virtex-II devices. V_{CCO} must be set according to Table 3. Note that there is a V_{CCO} requirement for GTL_DCI and GTLP_DCI, due to the on-chip termination resistor.

Table 7: **SelectI/O-Ultra Buffers With On-Chip Parallel Termination**

I/O Standard Description	IOSTANDARD Attribute	
	External Termination	On-Chip Termination
SSTL3 Class I	SSTL3_I	SSTL3_I_DCI(1)
SSTL3 Class II	SSTL3_II	SSTL3_II_DCI(1)
SSTL2 Class I	SSTL2_I	SSTL2_I_DCI(1)
SSTL2 Class II	SSTL2_II	SSTL2_II_DCI(1)
HSTL Class I	HSTL_I	HSTL_I_DCI
HSTL Class II	HSTL_II	HSTL_II_DCI
HSTL Class III	HSTL_III	HSTL_III_DCI
HSTL Class IV	HSTL_IV	HSTL_IV_DCI
GTL	GTL	GTL_DCI
GTLP	GTLP	GTLP_DCI

Notes:
1. SSTL-compatible

Figure 18, Figure 19, and Figure 20 illustrate various example configurations.

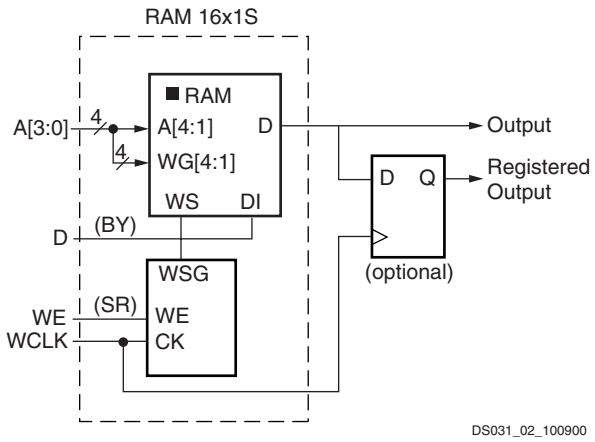


Figure 18: **Distributed SelectRAM (RAM16x1S)**

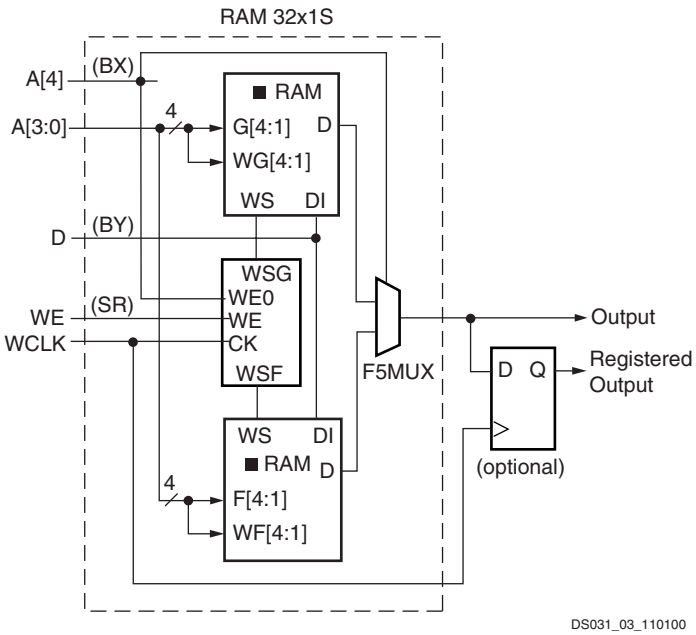


Figure 19: **Single-Port Distributed SelectRAM (RAM32x1S)**

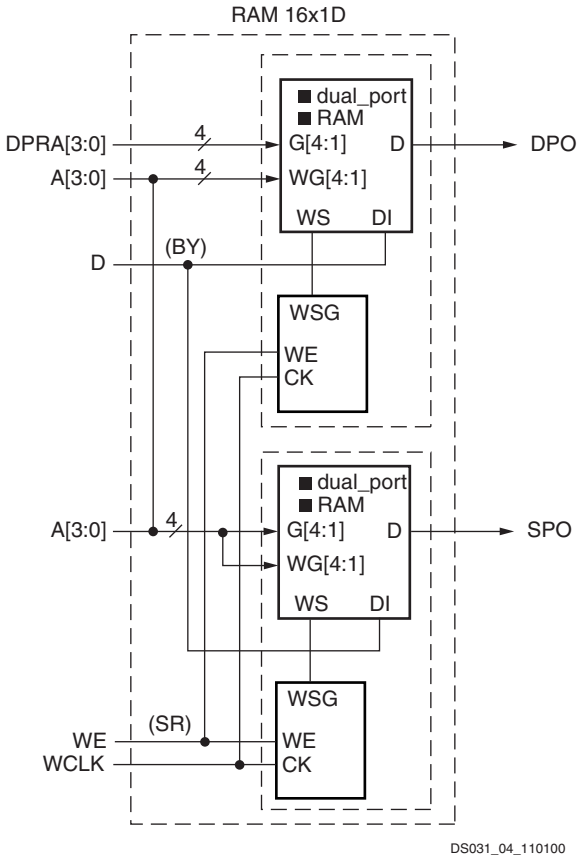


Figure 20: **Dual-Port Distributed SelectRAM (RAM16x1D)**

Similar to the RAM configuration, each function generator (LUT) can implement a 16 x 1-bit ROM. Five configurations are available: ROM16x1, ROM32x1, ROM64x1, ROM128x1, and ROM256x1. The ROM elements are cascadable to implement wider or/and deeper ROM. ROM contents are loaded at configuration. Table 10 shows the number of LUTs occupied by each configuration.

Table 10: **ROM Configuration**

ROM	Number of LUTs
16 x 1	1
32 x 1	2
64 x 1	4
128 x 1	8 (1 CLB)
256 x 1	16 (2 CLBs)

Table 17: **IOB Output Switching Characteristics Standard Adjustments *(Continued)***

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-6	-5	-4	
HSTL, Class II, 1.8V	HSTL_II_18	$T_{OHSTL\_II\_18}$	–0.17	–0.18	–0.20	ns
HSTL, Class III, 1.8V	HSTL_III_18	$T_{OHSTL\_III\_18}$	–0.16	–0.16	–0.18	ns
HSTL, Class IV, 1.8V	HSTL_IV_18	$T_{OHSTL\_IV\_18}$	–0.39	–0.40	–0.44	ns
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	$T_{OSSTL18\_I}$	0.20	0.20	0.22	ns
SSTL, Class II, 1.8V	SSTL18_II	$T_{OSSTL18\_II}$	–0.05	–0.05	–0.06	ns
SSTL, Class I, 2.5V	SSTL2_I	T_{OSSTL2_I}	0.21	0.22	0.24	ns
SSTL, Class II, 2.5V	SSTL2_II	T_{OSSTL2_II}	–0.15	–0.16	–0.18	ns
SSTL, Class I, 3.3V	SSTL3_I	T_{OSSTL3_I}	0.29	0.30	0.33	ns
SSTL, Class II, 3.3V	SSTL3_II	T_{OSSTL3_II}	–0.05	–0.05	–0.05	ns
AGP-2X/AGP (Accelerated Graphics Port)	AGP	T_{OAGP}	–0.27	–0.28	–0.31	ns
LVDCI (Low-Voltage Digitally Controlled Impedance), 3.3V	LVDCI_33	T_{OLVDCI_33}	0.74	0.77	0.84	ns
LVDCI, 2.5V	LVDCI_25	T_{OLVDCI_25}	0.78	0.80	0.88	ns
LVDCI, 1.8V	LVDCI_18	T_{OLVDCI_18}	0.84	0.87	0.95	ns
LVDCI, 1.5V	LVDCI_15	T_{OLVDCI_15}	1.82	1.88	2.06	ns
LVDCI, 3.3V, Half-Impedance	LVDCI_DV2_33	$T_{OLVDCI\_DV2\_33}$	0.12	0.12	0.13	ns
LVDCI, 2.5V, Half-Impedance	LVDCI_DV2_25	$T_{OLVDCI\_DV2\_25}$	0.03	0.03	0.03	ns
LVDCI, 1.8V, Half-Impedance	LVDCI_DV2_18	$T_{OLVDCI\_DV2\_18}$	0.42	0.43	0.48	ns
LVDCI, 1.5V, Half-Impedance	LVDCI_DV2_15	$T_{OLVDCI\_DV2\_15}$	1.20	1.23	1.36	ns
HSLVDCI (High-Speed Low-Voltage DCI), 1.5V	HSLVDCI_15	$T_{OHSLVDCI\_15}$	1.82	1.88	2.06	ns
HSLVDCI, 1.8V	HSLVDCI_18	$T_{OHSLVDCI\_18}$	1.05	1.08	1.24	ns
HSLVDCI, 2.5V	HSLVDCI_25	$T_{OHSLVDCI\_25}$	0.78	0.80	0.88	ns
HSLVDCI, 3.3V	HSLVDCI_33	$T_{OHSLVDCI\_33}$	0.74	0.77	0.84	ns
GTL (Gunning Transceiver Logic) with DCI	GTL_DCI	T_{OGTL_DCI}	–0.31	–0.32	–0.35	ns
GTL Plus with DCI	GTLP_DCI	T_{OGTLP_DCI}	–0.15	–0.16	–0.17	ns
HSTL (High-Speed Transceiver Logic), Class I, with DCI	HSTL_I_DCI	$T_{OHSTL\_I\_DCI}$	0.23	0.23	0.26	ns
HSTL, Class II, with DCI	HSTL_II_DCI	$T_{OHSTL\_II\_DCI}$	0.06	0.06	0.07	ns
HSTL, Class III, with DCI	HSTL_III_DCI	$T_{OHSTL\_III\_DCI}$	–0.17	–0.18	–0.20	ns
HSTL, Class IV, with DCI	HSTL_IV_DCI	$T_{OHSTL\_IV\_DCI}$	–0.46	–0.47	–0.52	ns
HSTL, Class I, 1.8V, with DCI	HSTL_I_DCI_18	$T_{OHSTL\_I\_DCI\_18}$	0.05	0.05	0.06	ns
HSTL, Class II, 1.8V, with DCI	HSTL_II_DCI_18	$T_{OHSTL\_II\_DCI\_18}$	–0.03	–0.03	–0.03	ns
HSTL, Class III, 1.8V, with DCI	HSTL_III_DCI_18	$T_{OHSTL\_III\_DCI\_18}$	–0.14	–0.14	–0.16	ns
HSTL, Class IV, 1.8V, with DCI	HSTL_IV_DCI_18	$T_{OHSTL\_IV\_DCI\_18}$	–0.41	–0.42	–0.47	ns
SSTL (Stub Series Terminated Logic), Class I, 1.8V, with DCI	SSTL18_I_DCI	$T_{OSSTL18\_I\_DCI}$	0.36	0.37	0.40	ns
SSTL, Class II, 1.8V, with DCI	SSTL18_II_DCI	$T_{OSSTL18\_II\_DCI}$	0.06	0.06	0.07	ns
SSTL, Class I, 2.5V, with DCI	SSTL2_I_DCI	$T_{OSSTL2\_I\_DCI}$	0.12	0.13	0.14	ns
SSTL, Class II, 2.5V, with DCI	SSTL2_II_DCI	$T_{OSSTL2\_II\_DCI}$	–0.10	–0.10	–0.11	ns
SSTL, Class I, 3.3V, with DCI	SSTL3_I_DCI	$T_{OSSTL3\_I\_DCI}$	0.15	0.16	0.17	ns
SSTL, Class II, 3.3V, with DCI	SSTL3_II_DCI	$T_{OSSTL3\_II\_DCI}$	0.08	0.08	0.09	ns

Table 19: **Output Delay Measurement Methodology**

Description	IOSTANDARD Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	50	0	V_{REF}	0.9
SSTL, Class II, 1.8V	SSTL18_II	25	0	V_{REF}	0.9
SSTL, Class I, 2.5V	SSTL2_I	50	0	V_{REF}	1.25
SSTL, Class II, 2.5V	SSTL2_II	25	0	V_{REF}	1.25
SSTL, Class I, 3.3V	SSTL3_I	50	0	V_{REF}	1.5
SSTL, Class II, 3.3V	SSTL3_II	25	0	V_{REF}	1.5
AGP-2X/AGP (Accelerated Graphics Port)	AGP-2X/AGP (rising edge)	50	0	0.94	0
	AGP-2X/AGP (falling edge)	50	0	2.03	3.3
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	50	0	V_{REF}	1.2
LVDS, 3.3V	LVDSEXT_25	50	0	V_{REF}	1.2
LVDSEXT (LVDS Extended Mode), 2.5V	LVDS_33	50	0	V_{REF}	1.2
LVDSEXT, 3.3V	LVDSEXT_33	50	0	V_{REF}	1.2
BLVDS (Bus LVDS), 2.5V	BLVDS_25	1M	0	1.2	0
LDT (HyperTransport), 2.5V	LDT_25	50	0	V_{REF}	0.6
LVPECL (Low-Voltage Positive Electron-Coupled Logic), 3.3V	LVPECL_33	1M	0	1.23	0
LVDCI/HSLVDCI (Low-Voltage Digitally Controlled Impedance), 3.3V	LVDCI_33, HSLVDCI_33	1M	0	1.65	0
LVDCI/HSLVDCI, 2.5V	LVDCI_25, HSLVDCI_25	1M	0	1.25	0
LVDCI/HSLVDCI, 1.8V	LVDCI_18, HSLVDCI_18	1M	0	0.9	0
LVDCI/HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I & II, with DCI	HSTL_I_DCI, HSTL_II_DCI	50	0	V_{REF}	0.75
HSTL, Class III & IV, with DCI	HSTL_III_DCI, HSTL_IV_DCI	50	0	0.9	1.5
HSTL, Class I & II, 1.8V, with DCI	HSTL_I_DCI_18, HSTL_II_DCI_18	50	0	V_{REF}	0.9
HSTL, Class III & IV, 1.8V, with DCI	HSTL_III_DCI_18, HSTL_IV_DCI_18	50	0	1.1	1.8
SSTL (Stub Series Termi.Logic), Class I & II, 1.8V, with DCI	SSTL18_I_DCI, SSTL18_II_DCI	50	0	V_{REF}	0.9
SSTL, Class I & II, 2.5V, with DCI	SSTL2_I_DCI, SSTL2_II_DCI	50	0	V_{REF}	1.25
SSTL, Class I & II, 3.3V, with DCI	SSTL3_I_DCI, SSTL3_II_DCI	50	0	V_{REF}	1.5
GTL (Gunning Transceiver Logic) with DCI	GTL_DCI	50	0	0.8	1.2
GTL Plus with DCI	GTLP_DCI	50	0	1.0	1.5

Notes:
1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. Per PCI specifications.
3. Per PCI-X specifications.

Output Clock Jitter

Table 40: **Output Clock Jitter**

Description	Symbol	Constraints	Speed Grade			Units
			-6	-5	-4	
Clock Synthesis Period Jitter						
CLK0	CLKOUT_PER_JITT_0		±100	±100	±100	ps
CLK90	CLKOUT_PER_JITT_90		±150	±150	±150	ps
CLK180	CLKOUT_PER_JITT_180		±150	±150	±150	ps
CLK270	CLKOUT_PER_JITT_270		±150	±150	±150	ps
CLK2X, CLK2X180	CLKOUT_PER_JITT_2X		±200	±200	±200	ps
CLKDV (integer division)	CLKOUT_PER_JITT_DV1		±150	±150	±150	ps
CLKDV (non-integer division)	CLKOUT_PER_JITT_DV2		±300	±300	±300	ps
CLKFX, CLKFX180	CLKOUT_PER_JITT_FX		Note 1	Note 1	Note 1	ps

Notes:
1. Values for this parameter are available at www.xilinx.com.

Output Clock Phase Alignment

Table 41: **Output Clock Phase Alignment**

Description	Symbol	Constraints	Speed Grade			Units
			-6	-5	-4	
Phase Offset Between CLKIN and CLKFB						
CLKIN/CLKFB	CLKIN_CLKFB_PHASE		±50	±50	±50	ps
Phase Offset Between Any DCM Outputs						
All CLK outputs	CLKOUT_PHASE		±140	±140	±140	ps
Duty Cycle Precision						
DLL outputs(1)	CLKOUT_DUTY_CYCLE_DLL(2)		±150	±150	±150	ps
CLKFX outputs	CLKOUT_DUTY_CYCLE_FX		±100	±100	±100	ps

Notes:
1. "DLL outputs" is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. CLKOUT_DUTY_CYCLE_DLL applies to the 1X clock outputs (CLK0, CLK90, CLK180, and CLK270) only if DUTY_CYCLE_CORRECTION = TRUE.
3. Specification also applies to PSCLK.

Table 4: **Virtex-II Pin Definitions *(Continued)***

Pin Name	Direction	Description
PROG_B	Input	Active Low asynchronous reset to configuration logic. This pin has a permanent weak pull-up resistor.
DONE	Input/Output	DONE is a bidirectional signal with an optional internal pull-up resistor. As an output, this pin indicates completion of the configuration process. As an input, a Low level on DONE can be configured to delay the start-up sequence.
M2, M1, M0	Input	Configuration mode selection.
HSWAP_EN	Input	Enable I/O pull-ups during configuration.
TCK	Input	Boundary Scan Clock.
TDI	Input	Boundary Scan Data Input.
TDO	Output	Boundary Scan Data Output.
TMS	Input	Boundary Scan Mode Select.
PWRDWN_B	Input *(unsupported)*	Active Low power-down pin (unsupported). *Driving this pin Low can adversely affect device operation and configuration.* PWRDWN_B is internally pulled High, which is its default state. It does not require an external pull-up.
Other Pins		
DXN, DXP	N/A	Temperature-sensing diode pins (Anode: DXP, Cathode: DXN).
V_{BATT}	Input	Decryptor key memory backup supply. Connect V_{BATT} to V_{CCAUX} or GND if battery is not used.
RSVD	N/A	Reserved pin - do not connect.
V_{CCO}	Input	Power-supply pins for the output drivers (per bank).
V_{CCAUX}	Input	Power-supply pins for auxiliary circuits.
V_{CCINT}	Input	Power-supply pins for the internal core logic.
GND	Input	Ground.

Notes:
1. All dedicated pins (JTAG and configuration) are powered by V_{CCAUX} (independent of the bank V_{CCO} voltage).

Table 6: **FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
1	IO_L92P_1	E11	NC	NC
1	IO_L05N_1	A11	NC	NC
1	IO_L05P_1	B11	NC	NC
1	IO_L04N_1	C11	NC	NC
1	IO_L04P_1/VREF_1	D11	NC	NC
1	IO_L03N_1/VRP_1	A12		
1	IO_L03P_1/VRN_1	B12		
1	IO_L02N_1	C12		
1	IO_L02P_1	D12		
1	IO_L01N_1	B13		
1	IO_L01P_1	C13		
2	IO_L01N_2	C16		
2	IO_L01P_2	D16		
2	IO_L02N_2/VRP_2	D14		
2	IO_L02P_2/VRN_2	D15		
2	IO_L03N_2	E13		
2	IO_L03P_2/VREF_2	E14		
2	IO_L04N_2	E15	NC	
2	IO_L04P_2	E16	NC	
2	IO_L06N_2	F13	NC	
2	IO_L06P_2	F14	NC	
2	IO_L43N_2	F15	NC	NC
2	IO_L43P_2	F16	NC	NC
2	IO_L45N_2	F12	NC	NC
2	IO_L45P_2/VREF_2	G12	NC	NC
2	IO_L91N_2	G13	NC	
2	IO_L91P_2	G14	NC	
2	IO_L93N_2	G15	NC	
2	IO_L93P_2/VREF_2	G16	NC	
2	IO_L94N_2	H13		
2	IO_L94P_2	H14		
2	IO_L96N_2	H15		
2	IO_L96P_2	H16		

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
NA	VCCINT	H19		
NA	VCCINT	H8		
NA	GND	AF26		
NA	GND	AF1		
NA	GND	AE25		
NA	GND	AE14		
NA	GND	AE13		
NA	GND	AE2		
NA	GND	AD24		
NA	GND	AD3		
NA	GND	AC23		
NA	GND	AC4		
NA	GND	AB22		
NA	GND	AB5		
NA	GND	AA21		
NA	GND	AA6		
NA	GND	U17		
NA	GND	U16		
NA	GND	U15		
NA	GND	U14		
NA	GND	U13		
NA	GND	U12		
NA	GND	U11		
NA	GND	U10		
NA	GND	T17		
NA	GND	T16		
NA	GND	T15		
NA	GND	T14		
NA	GND	T13		
NA	GND	T12		
NA	GND	T11		
NA	GND	T10		
NA	GND	R17		
NA	GND	R16		
NA	GND	R15		
NA	GND	R14		
NA	GND	R13		

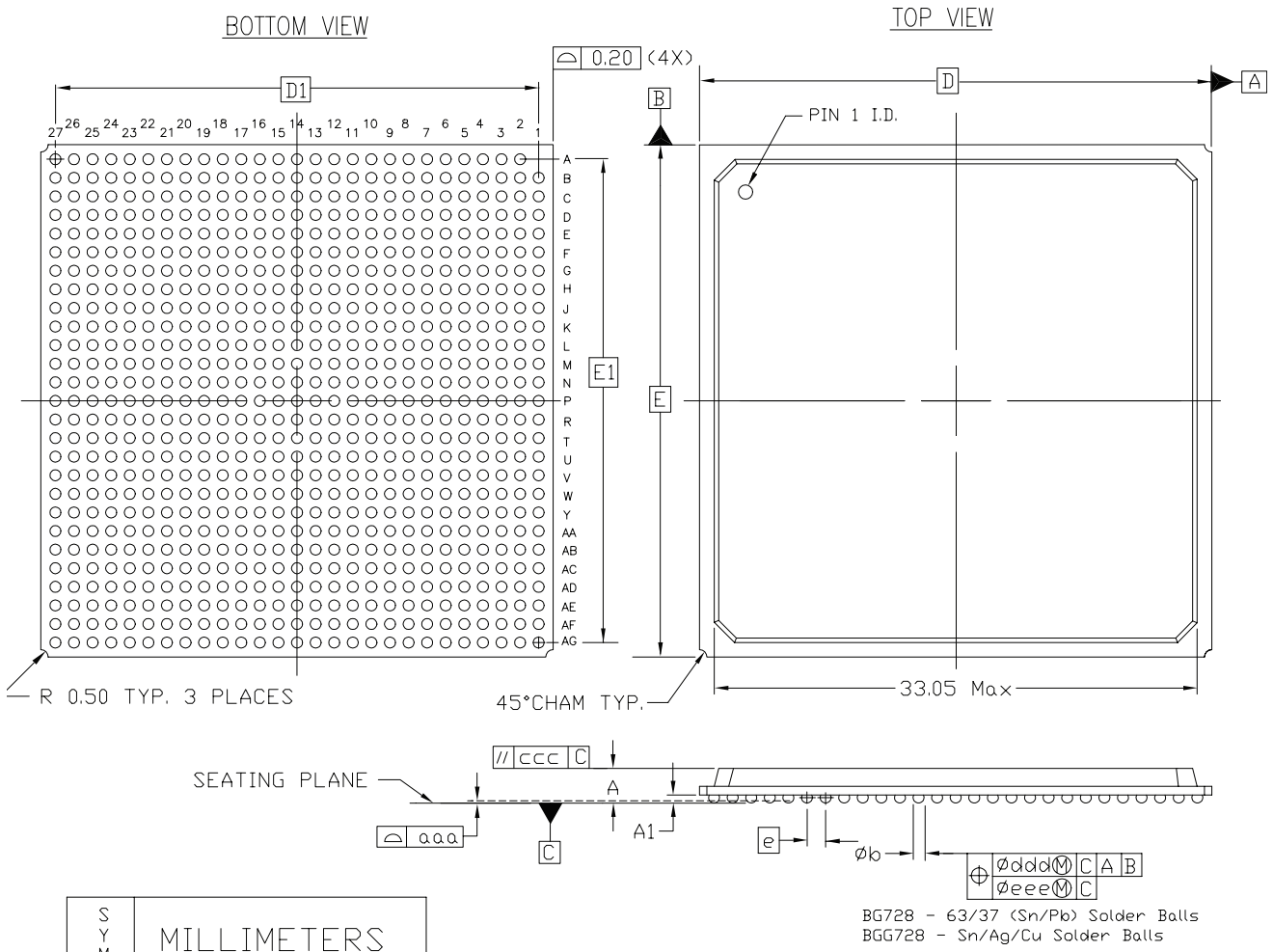
Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
4	IO_L91P_4	AB14		
4	IO_L92N_4	V14		
4	IO_L92P_4	Y14		
4	IO_L93N_4	AB13		
4	IO_L93P_4	AC13		
4	IO_L94N_4/VREF_4	Y13		
4	IO_L94P_4	AA13		
4	IO_L95N_4/GCLK3S	V13		
4	IO_L95P_4/GCLK2P	W13		
4	IO_L96N_4/GCLK1S	U14		
4	IO_L96P_4/GCLK0P	U13		
5	IO_L96N_5/GCLK7S	AD12		
5	IO_L96P_5/GCLK6P	AD11		
5	IO_L95N_5/GCLK5S	AC12		
5	IO_L95P_5/GCLK4P	AB12		
5	IO_L94N_5	AA12		
5	IO_L94P_5/VREF_5	Y12		
5	IO_L93N_5	W12		
5	IO_L93P_5	V12		
5	IO_L92N_5	U12		
5	IO_L92P_5	U11		
5	IO_L91N_5	AB11		
5	IO_L91P_5/VREF_5	AA11		
5	IO_L73N_5	Y11	NC	NC
5	IO_L73P_5	V11	NC	NC
5	IO_L72N_5	AD10	NC	
5	IO_L72P_5	AD9	NC	
5	IO_L70N_5	AC10	NC	
5	IO_L70P_5	AB10	NC	
5	IO_L69N_5/VREF_5	Y10	NC	
5	IO_L69P_5	W10	NC	
5	IO_L67N_5	V10	NC	
5	IO_L67P_5	U10	NC	
5	IO_L54N_5	AC9		
5	IO_L54P_5	AB9		

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
7	VCCO_7	F3		
NA	CCLK	AB23		
NA	PROG_B	C1		
NA	DONE	AB21		
NA	M0	AC4		
NA	M1	AB4		
NA	M2	AD3		
NA	HSWAP_EN	C2		
NA	TCK	C23		
NA	TDI	D1		
NA	TDO	C24		
NA	TMS	C21		
NA	PWRDWN_B	AC21		
NA	DXN	B4		
NA	DXP	C4		
NA	VBATT	B21		
NA	RSVD	A22		
NA	VCCAUX	AD13		
NA	VCCAUX	AC22		
NA	VCCAUX	AC3		
NA	VCCAUX	N1		
NA	VCCAUX	M24		
NA	VCCAUX	B22		
NA	VCCAUX	B3		
NA	VCCAUX	A12		
NA	VCCINT	U17		
NA	VCCINT	U8		
NA	VCCINT	T16		
NA	VCCINT	T9		
NA	VCCINT	R15		
NA	VCCINT	R14		
NA	VCCINT	R13		
NA	VCCINT	R12		
NA	VCCINT	R11		

BG728/BGG728 Standard BGA Package Specifications (1.27mm pitch)



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	2.33	2.60
A_1	0.50	0.60	0.70
D/E	35.00 BSC		
D_1/E_1	33.02 REF		
e	1.27BSC		
øb	0.60	0.75	0.90
aaa	---	---	0.20
ccc	---	---	0.35
ddd	---	---	0.30
eee	---	---	0.15
M	27		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-BAR-1
4. NO SOLDER BALL AND LAND ON A1.

728-BALL MOLDED BGA (BG728/BGG728)

Figure 6: **BG728/BGG728 Standard BGA Package Specifications**

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
1	IO_L68P_1	G12	NC	
1	IO_L67N_1	A9	NC	
1	IO_L67P_1	A10	NC	
1	IO_L54N_1	E10		
1	IO_L54P_1	E11		
1	IO_L53N_1	H12		
1	IO_L53P_1	H11		
1	IO_L52N_1	D9		
1	IO_L52P_1	D10		
1	IO_L51N_1/VREF_1	C9		
1	IO_L51P_1	C8		
1	IO_L50N_1	F11		
1	IO_L50P_1	F10		
1	IO_L49N_1	B8		
1	IO_L49P_1	B9		
1	IO_L24N_1	E8		
1	IO_L24P_1	E9		
1	IO_L23N_1	G11		
1	IO_L23P_1	H10		
1	IO_L22N_1	B7		
1	IO_L22P_1	A7		
1	IO_L21N_1/VREF_1	D8		
1	IO_L21P_1	E7		
1	IO_L20N_1	G10		
1	IO_L20P_1	G9		
1	IO_L19N_1	A5		
1	IO_L19P_1	A6		
1	IO_L06N_1	C6		
1	IO_L06P_1	C7		
1	IO_L05N_1	F9		
1	IO_L05P_1	G8		
1	IO_L04N_1	B6		
1	IO_L04P_1/VREF_1	C5		
1	IO_L03N_1/VRP_1	D7		
1	IO_L03P_1/VRN_1	D6		
1	IO_L02N_1	F8		
1	IO_L02P_1	F7		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
3	IO_L73P_3	W4	NC	NC
3	IO_L72N_3	W7	NC	
3	IO_L72P_3	V7	NC	
3	IO_L71N_3	V5	NC	
3	IO_L71P_3	W6	NC	
3	IO_L70N_3	W3	NC	
3	IO_L70P_3	Y3	NC	
3	IO_L69N_3/VREF_3	V8	NC	
3	IO_L69P_3	W8	NC	
3	IO_L68N_3	AA1	NC	
3	IO_L68P_3	AB1	NC	
3	IO_L67N_3	Y4	NC	
3	IO_L67P_3	AA4	NC	
3	IO_L54N_3	AA6		
3	IO_L54P_3	Y6		
3	IO_L53N_3	AA2		
3	IO_L53P_3	AB2		
3	IO_L52N_3	Y5		
3	IO_L52P_3	AA5		
3	IO_L51N_3/VREF_3	Y8		
3	IO_L51P_3	AA8		
3	IO_L50N_3	AC2		
3	IO_L50P_3	AD2		
3	IO_L49N_3	Y7		
3	IO_L49P_3	AA7		
3	IO_L48N_3	AC6		
3	IO_L48P_3	AB6		
3	IO_L47N_3	AD1		
3	IO_L47P_3	AE1		
3	IO_L46N_3	AB3		
3	IO_L46P_3	AC3		
3	IO_L45N_3/VREF_3	AB7		
3	IO_L45P_3	AC7		
3	IO_L44N_3	AB4		
3	IO_L44P_3	AC4		
3	IO_L43N_3	AB5		
3	IO_L43P_3	AC5		

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
7	IO_L45N_7	J34	
7	IO_L44P_7	M27	
7	IO_L44N_7	L27	
7	IO_L43P_7	H31	
7	IO_L43N_7	J31	
7	IO_L30P_7	F32	
7	IO_L30N_7	G32	
7	IO_L29P_7	N25	
7	IO_L29N_7	M25	
7	IO_L28P_7	F34	
7	IO_L28N_7	G34	
7	IO_L27P_7/VREF_7	J30	
7	IO_L27N_7	H30	
7	IO_L26P_7	K28	
7	IO_L26N_7	L28	
7	IO_L25P_7	H28	
7	IO_L25N_7	J29	
7	IO_L24P_7	G29	
7	IO_L24N_7	H29	
7	IO_L23P_7	L26	
7	IO_L23N_7	K26	
7	IO_L22P_7	F33	
7	IO_L22N_7	G33	
7	IO_L21P_7/VREF_7	J28	
7	IO_L21N_7	J27	
7	IO_L20P_7	K27	
7	IO_L20N_7	J26	
7	IO_L19P_7	E31	
7	IO_L19N_7	F31	
7	IO_L06P_7	D32	
7	IO_L06N_7	E32	
7	IO_L05P_7	L25	
7	IO_L05N_7	K24	
7	IO_L04P_7	D34	
7	IO_L04N_7	E34	
7	IO_L03P_7/VREF_7	G30	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
2	VCCO_2	R11	
2	VCCO_2	R5	
2	VCCO_2	P12	
2	VCCO_2	P11	
2	VCCO_2	N12	
2	VCCO_2	N11	
2	VCCO_2	M11	
2	VCCO_2	K1	
2	VCCO_2	G4	
3	VCCO_3	AH4	
3	VCCO_3	AE1	
3	VCCO_3	AC11	
3	VCCO_3	AB12	
3	VCCO_3	AB11	
3	VCCO_3	AA12	
3	VCCO_3	AA11	
3	VCCO_3	Y12	
3	VCCO_3	Y11	
3	VCCO_3	Y5	
3	VCCO_3	W12	
3	VCCO_3	W1	
3	VCCO_3	V12	
4	VCCO_4	AP16	
4	VCCO_4	AP10	
4	VCCO_4	AL7	
4	VCCO_4	AK15	
4	VCCO_4	AD15	
4	VCCO_4	AD14	
4	VCCO_4	AD13	
4	VCCO_4	AD12	
4	VCCO_4	AC17	
4	VCCO_4	AC16	
4	VCCO_4	AC15	
4	VCCO_4	AC14	
4	VCCO_4	AC13	
5	VCCO_5	AP25	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
0	IO_L49N_0	C23	
0	IO_L49P_0	C22	
0	IO_L50N_0	E22	
0	IO_L50P_0	E21	
0	IO_L51N_0	F21	
0	IO_L51P_0/VREF_0	F20	
0	IO_L52N_0	A24	
0	IO_L52P_0	A23	
0	IO_L53N_0	E20	
0	IO_L53P_0	E19	
0	IO_L54N_0	B22	
0	IO_L54P_0	B21	
0	IO_L67N_0	D21	
0	IO_L67P_0	D20	
0	IO_L68N_0	J20	
0	IO_L68P_0	J19	
0	IO_L69N_0	F19	
0	IO_L69P_0/VREF_0	F18	
0	IO_L70N_0	A22	
0	IO_L70P_0	A21	
0	IO_L71N_0	H19	
0	IO_L71P_0	H17	
0	IO_L72N_0	C21	
0	IO_L72P_0	C20	
0	IO_L73N_0	B20	
0	IO_L73P_0	B19	
0	IO_L74N_0	G18	
0	IO_L74P_0	G17	
0	IO_L75N_0	E18	
0	IO_L75P_0/VREF_0	D17	
0	IO_L76N_0	A20	
0	IO_L76P_0	A19	
0	IO_L77N_0	D19	
0	IO_L77P_0	D18	
0	IO_L78N_0	C19	
0	IO_L78P_0	C17	
0	IO_L91N_0/VREF_0	K18	
0	IO_L91P_0	J18	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
0	IO_L92N_0	F17	
0	IO_L92P_0	F16	
0	IO_L93N_0	B18	
0	IO_L93P_0	B17	
0	IO_L94N_0/VREF_0	J17	
0	IO_L94P_0	J16	
0	IO_L95N_0/GCLK7P	E17	
0	IO_L95P_0/GCLK6S	E16	
0	IO_L96N_0/GCLK5P	A18	
0	IO_L96P_0/GCLK4S	A17	
1	IO_L96N_1/GCLK3P	C16	
1	IO_L96P_1/GCLK2S	C15	
1	IO_L95N_1/GCLK1P	H16	
1	IO_L95P_1/GCLK0S	H15	
1	IO_L94N_1	A15	
1	IO_L94P_1/VREF_1	A14	
1	IO_L93N_1	F15	
1	IO_L93P_1	F14	
1	IO_L92N_1	G15	
1	IO_L92P_1	G14	
1	IO_L91N_1	B15	
1	IO_L91P_1/VREF_1	B14	
1	IO_L78N_1	D15	
1	IO_L78P_1	E15	
1	IO_L77N_1	J15	
1	IO_L77P_1	K14	
1	IO_L76N_1	D14	
1	IO_L76P_1	D13	
1	IO_L75N_1/VREF_1	E14	
1	IO_L75P_1	E13	
1	IO_L74N_1	A13	
1	IO_L74P_1	A12	
1	IO_L73N_1	F13	
1	IO_L73P_1	F12	
1	IO_L72N_1	J14	
1	IO_L72P_1	J13	
1	IO_L71N_1	B13	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
3	IO_L03P_3	AD7	
3	IO_L02N_3/VRP_3	AE6	
3	IO_L02P_3/VRN_3	AF5	
3	IO_L01N_3	AH2	
3	IO_L01P_3	AH3	
4	IO_L01N_4/BUSY/DOUT(1)	AD9	
4	IO_L01P_4/INIT_B	AD10	
4	IO_L02N_4/D0/DIN(1)	AF7	
4	IO_L02P_4/D1	AG7	
4	IO_L03N_4/D2/ALT_VRP_4	AK3	
4	IO_L03P_4/D3/ALT_VRN_4	AJ5	
4	IO_L04N_4/VREF_4	AE8	
4	IO_L04P_4	AF8	
4	IO_L05N_4/VRP_4	AK4	
4	IO_L05P_4/VRN_4	AK5	
4	IO_L06N_4	AH6	
4	IO_L06P_4	AH7	
4	IO_L19N_4	AC10	
4	IO_L19P_4	AC11	
4	IO_L20N_4	AE9	
4	IO_L20P_4	AE10	
4	IO_L21N_4	AL4	
4	IO_L21P_4/VREF_4	AL5	
4	IO_L22N_4	AB12	
4	IO_L22P_4	AB13	
4	IO_L23N_4	AJ6	
4	IO_L23P_4	AJ8	
4	IO_L24N_4	AK6	
4	IO_L24P_4	AK7	
4	IO_L25N_4	AG8	NC
4	IO_L25P_4	AG9	NC
4	IO_L26N_4	AF9	NC
4	IO_L26P_4	AF11	NC
4	IO_L27N_4	AH8	NC
4	IO_L27P_4/VREF_4	AH9	NC
4	IO_L28N_4	AD11	NC
4	IO_L28P_4	AD12	NC

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
5	IO_L24P_5	AG23	
5	IO_L23N_5	AE22	
5	IO_L23P_5	AE23	
5	IO_L22N_5	AK25	
5	IO_L22P_5	AK26	
5	IO_L21N_5/VREF_5	AH25	
5	IO_L21P_5	AG25	
5	IO_L20N_5	AB21	
5	IO_L20P_5	AC22	
5	IO_L19N_5	AL27	
5	IO_L19P_5	AL28	
5	IO_L06N_5	AK27	
5	IO_L06P_5	AJ27	
5	IO_L05N_5/VRP_5	AD23	
5	IO_L05P_5/VRN_5	AE24	
5	IO_L04N_5	AJ26	
5	IO_L04P_5/VREF_5	AH26	
5	IO_L03N_5/D4/ALT_VRP_5	AF23	
5	IO_L03P_5/D5/ALT_VRN_5	AF24	
5	IO_L02N_5/D6	AG24	
5	IO_L02P_5/D7	AF25	
5	IO_L01N_5/RDWR_B	AK28	
5	IO_L01P_5/CS_B	AK29	
6	IO_L01P_6	AF27	
6	IO_L01N_6	AF28	
6	IO_L02P_6/VRN_6	AE26	
6	IO_L02N_6/VRP_6	AE27	
6	IO_L03P_6	AH29	
6	IO_L03N_6/VREF_6	AH30	
6	IO_L04P_6	AB22	
6	IO_L04N_6	AB23	
6	IO_L05P_6	AG28	
6	IO_L05N_6	AG29	
6	IO_L06P_6	AH31	
6	IO_L06N_6	AG31	
6	IO_L19P_6	AA22	
6	IO_L19N_6	Y22	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
7	IO_L53N_7	K30	
7	IO_L52P_7	L28	
7	IO_L52N_7	J28	
7	IO_L51P_7/VREF_7	M24	
7	IO_L51N_7	L24	
7	IO_L50P_7	L29	
7	IO_L50N_7	K29	
7	IO_L49P_7	M25	
7	IO_L49N_7	L25	
7	IO_L48P_7	L26	
7	IO_L48N_7	J26	
7	IO_L47P_7	J31	
7	IO_L47N_7	H31	
7	IO_L46P_7	J29	
7	IO_L46N_7	H29	
7	IO_L45P_7/VREF_7	M22	
7	IO_L45N_7	L22	
7	IO_L44P_7	J30	
7	IO_L44N_7	G30	
7	IO_L43P_7	K27	
7	IO_L43N_7	J27	
7	IO_L27P_7/VREF_7	L23	NC
7	IO_L27N_7	K23	NC
7	IO_L25P_7	G31	NC
7	IO_L25N_7	F31	NC
7	IO_L24P_7	F30	
7	IO_L24N_7	E30	
7	IO_L23P_7	K25	
7	IO_L23N_7	J25	
7	IO_L22P_7	H28	
7	IO_L22N_7	G28	
7	IO_L21P_7/VREF_7	H27	
7	IO_L21N_7	G27	
7	IO_L20P_7	K24	
7	IO_L20N_7	J24	
7	IO_L19P_7	E31	
7	IO_L19N_7	D31	
7	IO_L06P_7	F28	