AMD Xilinx - XC2V80-5FGG256I Datasheet

Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	128
Number of Logic Elements/Cells	-
Total RAM Bits	147456
Number of I/O	120
Number of Gates	80000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v80-5fgg256i

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
11/07/00	1.0	Early access draft.
12/06/00	1.1	Initial release.
01/15/01	1.2	Added values to the tables in the Virtex-II Performance Characteristics and Virtex-II Switching Characteristics sections.
01/25/01	1.3	The data sheet was divided into four modules (per the current style standard).
04/02/01	1.5	Skipped v1.4 to sync up modules. Reverted to traditional double-column format.
07/30/01	1.6	Made minor changes to items listed under Summary of Virtex-II™ Features.
10/02/01	1.7	Minor edits.
07/16/02	1.8	Updated Virtex-II Device/Package Combinations shown in Table 6.
09/26/02	1.9	Updated Table 2 and Table 6 to reflect supported Virtex-II Device/Package Combinations.
08/01/03	2.0	All Virtex-II devices and speed grades now Production. See Table 13, Module 3.
03/29/04	2.0.1	Recompiled for backward compatibility with Acrobat 4 and above. No content changes.
06/24/04	3.3	Added references to available Pb-free wire-bond packages. (Revision number advanced to level of complete data sheet.)
03/01/05	3.4	*No changes in Module 1 for this revision.*
11/05/07	3.5	Updated copyright notice and legal disclaimer.

Notice of Disclaimer

THE XILINX HARDWARE FPGA AND CPLD DEVICES REFERRED TO HEREIN ("PRODUCTS") ARE SUBJECT TO THE TERMS AND CONDITIONS OF THE XILINX LIMITED WARRANTY WHICH CAN BE VIEWED AT http://www.xilinx.com/warranty.htm. THIS LIMITED WARRANTY DOES NOT EXTEND TO ANY USE OF PRODUCTS IN AN APPLICATION OR ENVIRONMENT THAT IS NOT WITHIN THE SPECIFICATIONS STATED IN THE XILINX DATA SHEET. ALL SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE. PRODUCTS ARE NOT DESIGNED OR INTENDED TO BE FAIL-SAFE OR FOR USE IN ANY APPLICATION REQUIRING FAIL-SAFE PERFORMANCE, SUCH AS LIFE-SUPPORT OR SAFETY DEVICES OR SYSTEMS, OR ANY OTHER APPLICATION THAT INVOKES THE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). USE OF PRODUCTS IN CRITICAL APPLICATIONS IS AT THE SOLE RISK OF CUSTOMER, SUBJECT TO APPLICABLE LAWS AND REGULATIONS.

Virtex-II Data Sheet

The Virtex-II Data Sheet contains the following modules:

- Virtex-II Platform FPGAs: Introduction and Overview (Module 1)
- Virtex-II Platform FPGAs: Functional Description (Module 2)
- Virtex-II Platform FPGAs: DC and Switching Characteristics (Module 3)
- Virtex-II Platform FPGAs: Pinout Information (Module 4)

Table 15: **IOB Input Switching Characteristics Standard Adjustments** ***(Continued)***

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-6	-5	-4	
LVDCI, 3.3V, Half-Impedance	LVDCI_DV2_33	$T_{ILVDCI\_DV2\_33}$	0.00	0.00	0.00	ns
LVDCI, 2.5V, Half-Impedance	LVDCI_DV2_25	$T_{ILVDCI\_DV2\_25}$	0.11	0.11	0.12	ns
LVDCI, 1.8V, Half-Impedance	LVDCI_DV2_18	$T_{ILVDCI\_DV2\_18}$	0.42	0.43	0.49	ns
LVDCI, 1.5V, Half-Impedance	LVDCI_DV2_15	$T_{ILVDCI\_DV2\_15}$	0.98	1.00	1.14	ns
HSLVDCI (High-Speed Low-Voltage DCI), 1.5V	HSLVDCI_15	$T_{IHSLVDCI\_15}$	0.42	0.42	0.48	ns
HSLVDCI, 1.8V	HSLVDCI_18	$T_{IHSLVDCI\_18}$	0.52	0.53	0.60	ns
HSLVDCI, 2.5V	HSLVDCI_25	$T_{IHSLVDCI\_25}$	0.42	0.42	0.48	ns
HSLVDCI, 3.3V	HSLVDCI_33	$T_{IHSLVDCI\_33}$	0.42	0.42	0.48	ns
GTL (Gunning Transceiver Logic) with DCI	GTL_DCI	T_{IGTL_DCI}	0.42	0.42	0.48	ns
GTL Plus with DCI	GTLP_DCI	T_{IGTLP_DCI}	0.42	0.42	0.48	ns
HSTL (High-Speed Transceiver Logic), Class I, with DCI	HSTL_I_DCI	$T_{IHSTL\_I\_DCI}$	0.42	0.42	0.48	ns
HSTL, Class II, with DCI	HSTL_II_DCI	$T_{IHSTL\_II\_DCI}$	0.42	0.42	0.48	ns
HSTL, Class III, with DCI	HSTL_III_DCI	$T_{IHSTL\_III\_DCI}$	0.42	0.42	0.48	ns
HSTL, Class IV, with DCI	HSTL_IV_DCI	$T_{IHSTL\_IV\_DCI}$	0.42	0.42	0.48	ns
HSTL, Class I, 1.8V, with DCI	HSTL_I_DCI_18	$T_{IHSTL\_I\_DCI\_18}$	0.42	0.42	0.48	ns
HSTL, Class II, 1.8V, with DCI	HSTL_II_DCI_18	$T_{IHSTL\_II\_DCI\_18}$	0.42	0.42	0.48	ns
HSTL, Class III, 1.8V, with DCI	HSTL_III_DCI_18	$T_{IHSTL\_III\_DCI\_18}$	0.42	0.42	0.48	ns
HSTL, Class IV, 1.8V, with DCI	HSTL_IV_DCI_18	$T_{IHSTL\_IV\_DCI\_18}$	0.42	0.42	0.48	ns
SSTL (Stub Series Terminated Logic), Class I, 1.8V, with DCI	SSTL18_I_DCI	$T_{ISSTL18\_I\_DCI}$	0.42	0.42	0.48	ns
SSTL, Class II, 1.8V, with DCI	SSTL18_II_DCI	$T_{ISSTL18\_II\_DCI}$	0.42	0.42	0.48	ns
SSTL, Class I, 2.5V, with DCI	SSTL2_I_DCI	$T_{ISSTL2\_I\_DCI}$	0.42	0.42	0.48	ns
SSTL, Class II, 2.5V, with DCI	SSTL2_II_DCI	$T_{ISSTL2\_II\_DCI}$	0.42	0.42	0.48	ns
SSTL, Class I, 3.3V, with DCI	SSTL3_I_DCI	$T_{ISSTL3\_I\_DCI}$	0.35	0.35	0.40	ns
SSTL, Class II, 3.3V, with DCI	SSTL3_II_DCI	$T_{ISSTL3\_II\_DCI}$	0.35	0.35	0.40	ns
LVDS (Low-Voltage Differential Signaling), 2.5V, with DCI	LVDS_25_DCI	$T_{ILVDS\_25\_DCI}$	0.60	0.60	0.69	ns
LVDS, 3.3V, with DCI	LVDS_33_DCI	$T_{ILVDS\_33\_DCI}$	0.60	0.60	0.69	ns
LVDSEXT (LVDS Extended Mode), 2.5V, with DCI	LVDSEXT_25_DCI	$T_{ILVDSEXT\_25\_DCI}$	0.58	0.59	0.79	ns
LVDSEXT, 3.3V, with DCI	LVDSEXT_33_DCI	$T_{ILVDSEXT\_33\_DCI}$	0.56	0.56	0.65	ns

Notes:
1. Input timing for LVTTL is measured at 1.4V. For other I/O standards, see Table 18.

Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. (See ***Virtex-II Platform FPGA User Guide*** for details.) The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setup shown in Figure 1.

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. (IBIS models can be found on the web at **http://support.xilinx.com/support/sw_ibis.htm**.) Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 19.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. The increase or decrease in delay should be added to or subtracted from the I/O Output Standard Adjustment value (Table 17) to yield the actual worst-case propagation delay (clock-to-input) of the PCB trace.

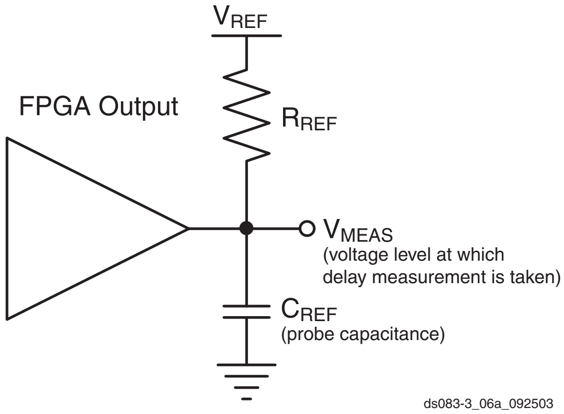

Figure 1: **Generalized Test Setup**

Table 19: **Output Delay Measurement Methodology**

Description	IOSTANDARD Attribute	R_{REF} (Ω)	$C_{REF}^{(1)}$ (pF)	V_{MEAS} (V)	V_{REF} (V)
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL (all)	1M	0	1.4	0
LVCMOS (Low-Voltage CMOS), 3.3V	LVCMOS33	1M	0	1.65	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3 (rising edge)	25	$10^{(2)}$	0.94	0
	PCI33_3 (falling edge)	25	$10^{(2)}$	2.03	3.3
PCI, 66 MHz, 3.3V	PCI66_3 (rising edge)	25	$10^{(2)}$	0.94	0
	PCI66_3 (falling edge)	25	$10^{(2)}$	2.03	3.3
PCI-X, 133 MHz, 3.3V	PCIX (rising edge)	25	$10^{(3)}$	0.94	
	PCIX (falling edge	25	$10^{(3)}$	2.03	3.3
GTL (Gunning Transceiver Logic)	GTL	25	0	0.8	1.2
GTL Plus	GTLP	25	0	1.0	1.5
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class III	HSTL_III	50	0	0.9	1.5
HSTL, Class IV	HSTL_IV	25	0	0.9	1.5
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSTL, Class III, 1.8V	HSTL_III_18	50	0	1.1	1.8
HSTL, Class IV, 1.8V	HSTL_IV_18	25	0	1.1	1.8

Clock Distribution Switching Characteristics

Table 20: **Clock Distribution Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Global Clock Buffer I input to O output	T_{GIO}	0.47	0.52	0.59	ns, Max
Global Clock Buffer S input Setup/Hold to I1 an I2 inputs	T_{GSI}/T_{GIS}	0.55/ 0	0.61/ 0	0.70/ 0	ns, Max

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used (see Figure 16 in Module 2). The values listed below are worst-case. Precise values are provided by the timing analyzer.

Table 21: **CLB Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Combinatorial Delays					
4-input function: F/G inputs to X/Y outputs	T_{ILO}	0.35	0.39	0.44	ns, Max
5-input function: F/G inputs to F5 output	T_{IF5}	0.57	0.63	0.72	ns, Max
5-input function: F/G inputs to X output	T_{IF5X}	0.76	0.83	0.95	ns, Max
FXINA or FXINB inputs to Y output via MUXFX	T_{IFXY}	0.36	0.39	0.45	ns, Max
FXINA input to FX output via MUXFX	T_{INAFX}	0.26	0.28	0.32	ns, Max
FXINB input to FX output via MUXFX	T_{INBFX}	0.26	0.28	0.32	ns, Max
SOPIN input to SOPOUT output via ORCY	T_{SOPSOP}	0.35	0.38	0.44	ns, Max
Incremental delay routing through transparent latch to XQ/YQ outputs	T_{IFNCTL}	0.41	0.45	0.51	ns, Max
Sequential Delays					
FF Clock CLK to XQ/YQ outputs	T_{CKO}	0.45	0.50	0.57	ns, Max
Latch Clock CLK to XQ/YQ outputs	T_{CKLO}	0.54	0.59	0.68	ns, Max
Setup and Hold Times Before/After Clock CLK					
BX/BY inputs	T_{DICK}/T_{CKDI}	0.30/–0.07	0.33/–0.08	0.37/–0.09	ns, Min
DY inputs	T_{DYCK}/T_{CKDY}	0.30/–0.07	0.33/–0.08	0.37/–0.09	ns, Min
DX inputs	T_{DXCK}/T_{CKDX}	0.30/–0.07	0.33/–0.08	0.37/–0.09	ns, Min
CE input	T_{CECK}/T_{CKCE}	0.19/–0.06	0.21/–0.07	0.24/–0.08	ns, Min
SR/BY inputs (synchronous)	T_{SRCK}/T_{SCKR}	0.21/–0.02	0.23/–0.03	0.26/–0.03	ns, Min
Clock CLK					
Minimum Pulse Width, High	T_{CH}	0.61	0.67	0.77	ns, Min
Minimum Pulse Width, Low	T_{CL}	0.61	0.67	0.77	ns, Min
Set/Reset					
Minimum Pulse Width, SR/BY inputs (asynchronous)	T_{RPW}	0.61	0.67	0.77	ns, Min
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	T_{RQ}	1.06	1.17	1.34	ns, Max
Toggle Frequency (MHz) (for export control)	F_{TOG}	820	750	650	MHz

JTAG Test Access Port Switching Characteristics

Characterization data for some of the most commonly requested timing parameters shown in Figure 6 is listed in Table 33.

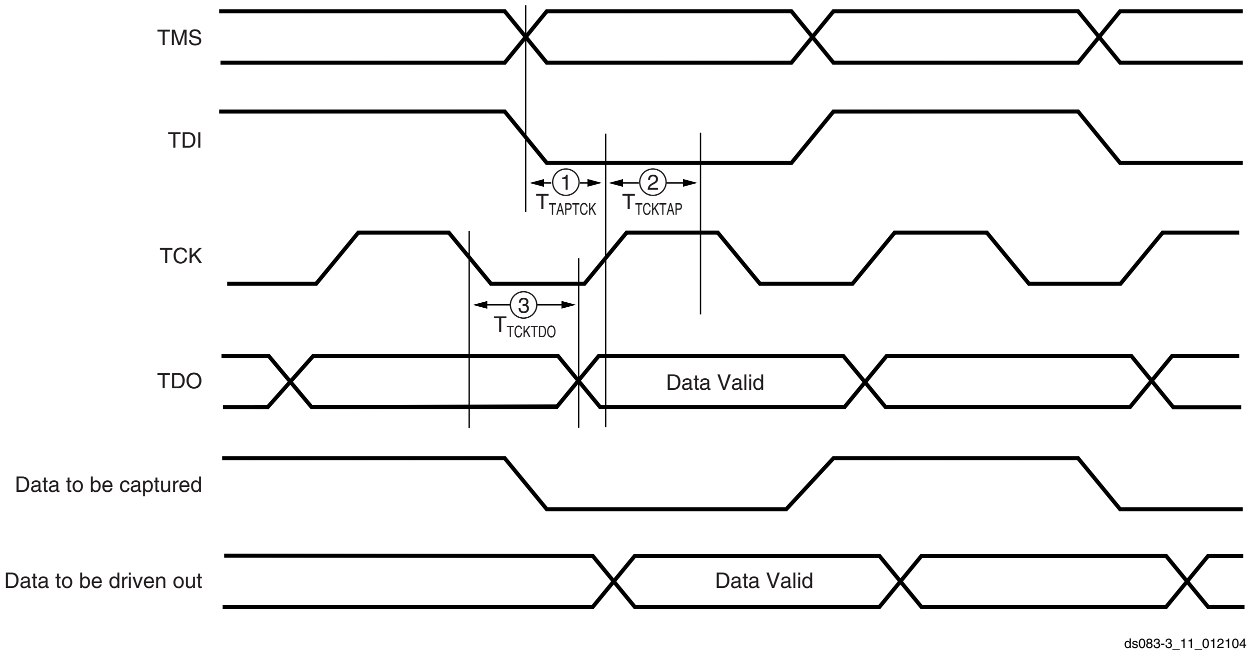

Figure 6: **Virtex-II Pro Boundary Scan Port Timing Waveforms**

Table 33: **Boundary-Scan Port Timing Specifications**

	Description	Figure References	Symbol	Value	Units
TCK	TMS and TDI setup time	1	T_{TAPTCK}	5.5	ns, min
	TMS and TDI hold times	2	T_{TCKTAP}	0.0	ns, min
	Falling edge to TDO output valid	3	T_{TCKTDO}	10.0	ns, max
	Maximum frequency		F_{TCK}	33.0	MHz, max

Table 6: **FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
4	IO_L91N_4/VREF_4	R11	NC	NC
4	IO_L91P_4	T11	NC	NC
4	IO_L92N_4	M11	NC	NC
4	IO_L92P_4	M10	NC	NC
4	IO_L93N_4	N10	NC	NC
4	IO_L93P_4	P10	NC	NC
4	IO_L94N_4/VREF_4	R10		
4	IO_L94P_4	T10		
4	IO_L95N_4/GCLK3S	N9		
4	IO_L95P_4/GCLK2P	P9		
4	IO_L96N_4/GCLK1S	R9		
4	IO_L96P_4/GCLK0P	T9		
5	IO_L96N_5/GCLK7S	T8		
5	IO_L96P_5/GCLK6P	R8		
5	IO_L95N_5/GCLK5S	P8		
5	IO_L95P_5/GCLK4P	N8		
5	IO_L94N_5	T7		
5	IO_L94P_5/VREF_5	R7		
5	IO_L93N_5	P7	NC	NC
5	IO_L93P_5	N7	NC	NC
5	IO_L92N_5	M7	NC	NC
5	IO_L92P_5	M6	NC	NC
5	IO_L91N_5	T6	NC	NC
5	IO_L91P_5/VREF_5	R6	NC	NC
5	IO_L05N_5/VRP_5	P6	NC	NC
5	IO_L05P_5/VRN_5	N6	NC	NC
5	IO_L04N_5	T5	NC	NC
5	IO_L04P_5/VREF_5	R5	NC	NC
5	IO_L03N_5/D4/ALT_VRP_5	P5		
5	IO_L03P_5/D5/ALT_VRN_5	N5		
5	IO_L02N_5/D6	R4		
5	IO_L02P_5/D7	P4		
5	IO_L01N_5/RDWR_B	T4		

Table 6: **FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
6	VCCO_6	J5		
7	VCCO_7	H6		
7	VCCO_7	H5		
7	VCCO_7	G6		
NA	CCLK	P15		
NA	PROG_B	A2		
NA	DONE	R14		
NA	M0	T2		
NA	M1	P2		
NA	M2	R3		
NA	HSWAP_EN	B3		
NA	TCK	A15		
NA	TDI	C2		
NA	TDO	C15		
NA	TMS	B14		
NA	PWRDWN_B	T15		
NA	RSVD	A4		
NA	RSVD	A3		
NA	VBATT	A14		
NA	RSVD	A13		
NA	VCCAUX	R16		
NA	VCCAUX	R1		
NA	VCCAUX	B16		
NA	VCCAUX	B1		
NA	VCCINT	N13		
NA	VCCINT	N4		
NA	VCCINT	M12		
NA	VCCINT	M5		
NA	VCCINT	E12		
NA	VCCINT	E5		
NA	VCCINT	D13		
NA	VCCINT	D4		

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
1	IO_L21P_1	D16	NC	NC
1	IO_L06N_1	E16		
1	IO_L06P_1	E17		
1	IO_L05N_1	A17		
1	IO_L05P_1	B17		
1	IO_L04N_1	C17		
1	IO_L04P_1/VREF_1	D17		
1	IO_L03N_1/VRP_1	A18		
1	IO_L03P_1/VRN_1	B18		
1	IO_L02N_1	C18		
1	IO_L02P_1	D18		
1	IO_L01N_1	A19		
1	IO_L01P_1	B19		
2	IO_L01N_2	C21		
2	IO_L01P_2	C22		
2	IO_L02N_2/VRP_2	E18		
2	IO_L02P_2/VRN_2	F18		
2	IO_L03N_2	D21		
2	IO_L03P_2/VREF_2	D22		
2	IO_L04N_2	E19		
2	IO_L04P_2	E20		
2	IO_L06N_2	E21		
2	IO_L06P_2	E22		
2	IO_L19N_2	F19	NC	NC
2	IO_L19P_2	F20	NC	NC
2	IO_L21N_2	F21	NC	NC
2	IO_L21P_2/VREF_2	F22	NC	NC
2	IO_L22N_2	G18	NC	NC
2	IO_L22P_2	H18	NC	NC
2	IO_L24N_2	G19	NC	NC
2	IO_L24P_2	G20	NC	NC
2	IO_L43N_2	G21		
2	IO_L43P_2	G22		

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
2	IO_L69P_2/VREF_2	L18	NC	
2	IO_L70N_2	K23	NC	
2	IO_L70P_2	L24	NC	
2	IO_L72N_2	K22	NC	
2	IO_L72P_2	L22	NC	
2	IO_L73N_2	L21	NC	NC
2	IO_L73P_2	L20	NC	NC
2	IO_L91N_2	M23		
2	IO_L91P_2	N24		
2	IO_L93N_2	M21		
2	IO_L93P_2/VREF_2	M22		
2	IO_L94N_2	M19		
2	IO_L94P_2	M20		
2	IO_L96N_2	M17		
2	IO_L96P_2	M18		
3	IO_L96N_3	N23		
3	IO_L96P_3	N22		
3	IO_L94N_3	N20		
3	IO_L94P_3	N21		
3	IO_L93N_3/VREF_3	N19		
3	IO_L93P_3	N18		
3	IO_L91N_3	N17		
3	IO_L91P_3	P17		
3	IO_L73N_3	P24	NC	NC
3	IO_L73P_3	R24	NC	NC
3	IO_L72N_3	R23	NC	
3	IO_L72P_3	R22	NC	
3	IO_L70N_3	P22	NC	
3	IO_L70P_3	P21	NC	
3	IO_L69N_3/VREF_3	P20	NC	
3	IO_L69P_3	P18	NC	
3	IO_L67N_3	T24	NC	
3	IO_L67P_3	U24	NC	
3	IO_L54N_3	T23		
3	IO_L54P_3	T22		

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
2	IO_L70P_2	N19
2	IO_L72N_2	M22
2	IO_L72P_2	M23
2	IO_L73N_2	M24
2	IO_L73P_2	N24
2	IO_L75N_2	M26
2	IO_L75P_2/VREF_2	M27
2	IO_L76N_2	N20
2	IO_L76P_2	N21
2	IO_L78N_2	N22
2	IO_L78P_2	N23
2	IO_L91N_2	N25
2	IO_L91P_2	P25
2	IO_L93N_2	N26
2	IO_L93P_2/VREF_2	N27
2	IO_L94N_2	P20
2	IO_L94P_2	P21
2	IO_L96N_2	P22
2	IO_L96P_2	P23
3	IO_L96N_3	R27
3	IO_L96P_3	R26
3	IO_L94N_3	R25
3	IO_L94P_3	R24
3	IO_L93N_3/VREF_3	R23
3	IO_L93P_3	T23
3	IO_L91N_3	R22
3	IO_L91P_3	R21
3	IO_L78N_3	R20
3	IO_L78P_3	R19
3	IO_L76N_3	T27
3	IO_L76P_3	T26
3	IO_L75N_3/VREF_3	T24
3	IO_L75P_3	U24
3	IO_L73N_3	T22
3	IO_L73P_3	U22

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
2	VCCO_2	L10		
2	VCCO_2	L9		
2	VCCO_2	K9		
2	VCCO_2	E2		
3	VCCO_3	AF2		
3	VCCO_3	AA9		
3	VCCO_3	Y10		
3	VCCO_3	Y9		
3	VCCO_3	W10		
3	VCCO_3	W9		
3	VCCO_3	V10		
3	VCCO_3	V9		
3	VCCO_3	V3		
3	VCCO_3	U10		
3	VCCO_3	T10		
4	VCCO_4	AJ5		
4	VCCO_4	AH13		
4	VCCO_4	AB13		
4	VCCO_4	AB12		
4	VCCO_4	AB11		
4	VCCO_4	AB10		
4	VCCO_4	AA15		
4	VCCO_4	AA14		
4	VCCO_4	AA13		
4	VCCO_4	AA12		
4	VCCO_4	AA11		
5	VCCO_5	AJ26		
5	VCCO_5	AH18		
5	VCCO_5	AB21		
5	VCCO_5	AB20		
5	VCCO_5	AB19		
5	VCCO_5	AB18		
5	VCCO_5	AA20		
5	VCCO_5	AA19		
5	VCCO_5	AA18		
5	VCCO_5	AA17		
5	VCCO_5	AA16		

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
3	IO_L83P_3	Y4	NC
3	IO_L82N_3	W11	NC
3	IO_L82P_3	V11	NC
3	IO_L81N_3/VREF_3	W8	NC
3	IO_L81P_3	Y8	NC
3	IO_L80N_3	W2	NC
3	IO_L80P_3	Y1	NC
3	IO_L79N_3	AA3	NC
3	IO_L79P_3	AB3	NC
3	IO_L78N_3	Y6	
3	IO_L78P_3	AA6	
3	IO_L77N_3	AA4	
3	IO_L77P_3	AB4	
3	IO_L76N_3	Y7	
3	IO_L76P_3	AA8	
3	IO_L75N_3/VREF_3	Y10	
3	IO_L75P_3	AA10	
3	IO_L74N_3	AA1	
3	IO_L74P_3	AB1	
3	IO_L73N_3	AA5	
3	IO_L73P_3	AB5	
3	IO_L72N_3	AA9	
3	IO_L72P_3	Y9	
3	IO_L71N_3	AA2	
3	IO_L71P_3	AB2	
3	IO_L70N_3	AB6	
3	IO_L70P_3	AC6	
3	IO_L69N_3/VREF_3	AD1	
3	IO_L69P_3	AC1	
3	IO_L68N_3	AC3	
3	IO_L68P_3	AD3	
3	IO_L67N_3	AC4	
3	IO_L67P_3	AD4	
3	IO_L54N_3	AB7	
3	IO_L54P_3	AC7	
3	IO_L53N_3	AC2	

FF1517 Flip-Chip Fine-Pitch BGA Package

As shown in Table 13, XC2V4000, XC2V6000, and XC2V8000 Virtex-II devices are available in the FF1517 flip-chip fine-pitch BGA package. Pins in each of these devices are the same, except for the pin differences in the XC2V4000 and XC2V6000 devices shown in the No Connect columns. Following this table are the FF1517 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
0	IO_L01N_0	B36		
0	IO_L01P_0	C36		
0	IO_L02N_0	J30		
0	IO_L02P_0	J29		
0	IO_L03N_0/VRP_0	D33		
0	IO_L03P_0/VRN_0	D34		
0	IO_L04N_0/VREF_0	C34		
0	IO_L04P_0	C35		
0	IO_L05N_0	H30		
0	IO_L05P_0	G30		
0	IO_L06N_0	D32		
0	IO_L06P_0	E33		
0	IO_L07N_0	A35	NC	
0	IO_L07P_0	A36	NC	
0	IO_L08N_0	K28	NC	
0	IO_L08P_0	J28	NC	
0	IO_L09N_0	E32	NC	
0	IO_L09P_0/VREF_0	F32	NC	
0	IO_L10N_0	B34	NC	
0	IO_L10P_0	B35	NC	
0	IO_L11N_0	H29	NC	
0	IO_L11P_0	H28	NC	
0	IO_L12N_0	F31	NC	
0	IO_L12P_0	G31	NC	
0	IO_L19N_0	C32		
0	IO_L19P_0	C33		
0	IO_L20N_0	M26		
0	IO_L20P_0	M25		
0	IO_L21N_0	E30		
0	IO_L21P_0/VREF_0	E31		
0	IO_L22N_0	A33		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
1	IO_L33N_1/VREF_1	D11	NC	
1	IO_L33P_1	D12	NC	
1	IO_L32N_1	H14	NC	
1	IO_L32P_1	H13	NC	
1	IO_L31N_1	A8	NC	
1	IO_L31P_1	A9	NC	
1	IO_L30N_1	F11		
1	IO_L30P_1	F12		
1	IO_L29N_1	K14		
1	IO_L29P_1	L14		
1	IO_L28N_1	C9		
1	IO_L28P_1	C10		
1	IO_L27N_1/VREF_1	G11		
1	IO_L27P_1	G12		
1	IO_L26N_1	M15		
1	IO_L26P_1	M14		
1	IO_L25N_1	B7		
1	IO_L25P_1	B8		
1	IO_L24N_1	D9		
1	IO_L24P_1	D10		
1	IO_L23N_1	J13		
1	IO_L23P_1	J12		
1	IO_L22N_1	A6		
1	IO_L22P_1	A7		
1	IO_L21N_1/VREF_1	E9		
1	IO_L21P_1	E10		
1	IO_L20N_1	D8		
1	IO_L20P_1	E7		
1	IO_L19N_1	C7		
1	IO_L19P_1	C8		
1	IO_L12N_1	F9	NC	
1	IO_L12P_1	F10	NC	
1	IO_L11N_1	H12	NC	
1	IO_L11P_1	H11	NC	
1	IO_L10N_1	B5	NC	
1	IO_L10P_1	B6	NC	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	DONE	AP7		
NA	M0	AN32		
NA	M1	AP33		
NA	M2	AT35		
NA	HSWAP_EN	E34		
NA	TCK	G8		
NA	TDI	D35		
NA	TDO	E6		
NA	TMS	F7		
NA	PWRDWN_B	AN8		
NA	DXN	G32		
NA	DXP	F33		
NA	VBATT	D5		
NA	RSVD	H9		
NA	VCCAUX	AV20		
NA	VCCAUX	AT37		
NA	VCCAUX	AT3		
NA	VCCAUX	Y38		
NA	VCCAUX	Y2		
NA	VCCAUX	D37		
NA	VCCAUX	D3		
NA	VCCAUX	B20		
NA	VCCINT	AG27		
NA	VCCINT	AG20		
NA	VCCINT	AG13		
NA	VCCINT	AF26		
NA	VCCINT	AF20		
NA	VCCINT	AF14		
NA	VCCINT	AE25		
NA	VCCINT	AE24		
NA	VCCINT	AE23		
NA	VCCINT	AE22		
NA	VCCINT	AE21		
NA	VCCINT	AE20		
NA	VCCINT	AE19		

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
5	IO_L24P_5	AG23	
5	IO_L23N_5	AE22	
5	IO_L23P_5	AE23	
5	IO_L22N_5	AK25	
5	IO_L22P_5	AK26	
5	IO_L21N_5/VREF_5	AH25	
5	IO_L21P_5	AG25	
5	IO_L20N_5	AB21	
5	IO_L20P_5	AC22	
5	IO_L19N_5	AL27	
5	IO_L19P_5	AL28	
5	IO_L06N_5	AK27	
5	IO_L06P_5	AJ27	
5	IO_L05N_5/VRP_5	AD23	
5	IO_L05P_5/VRN_5	AE24	
5	IO_L04N_5	AJ26	
5	IO_L04P_5/VREF_5	AH26	
5	IO_L03N_5/D4/ALT_VRP_5	AF23	
5	IO_L03P_5/D5/ALT_VRN_5	AF24	
5	IO_L02N_5/D6	AG24	
5	IO_L02P_5/D7	AF25	
5	IO_L01N_5/RDWR_B	AK28	
5	IO_L01P_5/CS_B	AK29	
6	IO_L01P_6	AF27	
6	IO_L01N_6	AF28	
6	IO_L02P_6/VRN_6	AE26	
6	IO_L02N_6/VRP_6	AE27	
6	IO_L03P_6	AH29	
6	IO_L03N_6/VREF_6	AH30	
6	IO_L04P_6	AB22	
6	IO_L04N_6	AB23	
6	IO_L05P_6	AG28	
6	IO_L05N_6	AG29	
6	IO_L06P_6	AH31	
6	IO_L06N_6	AG31	
6	IO_L19P_6	AA22	
6	IO_L19N_6	Y22	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
NA	VCCINT	T21	
NA	VCCINT	U10	
NA	VCCINT	U13	
NA	VCCINT	U19	
NA	VCCINT	U22	
NA	VCCINT	V13	
NA	VCCINT	V19	
NA	VCCINT	W13	
NA	VCCINT	W14	
NA	VCCINT	W15	
NA	VCCINT	W16	
NA	VCCINT	W17	
NA	VCCINT	W18	
NA	VCCINT	W19	
NA	VCCINT	Y12	
NA	VCCINT	Y16	
NA	VCCINT	Y20	
NA	VCCINT	AA11	
NA	VCCINT	AA16	
NA	VCCINT	AA21	
NA	VCCINT	AB15	
NA	VCCINT	AB17	
NA	GND	A2	
NA	GND	A3	
NA	GND	A16	
NA	GND	A29	
NA	GND	A30	
NA	GND	B1	
NA	GND	B2	
NA	GND	B8	
NA	GND	B24	
NA	GND	B30	
NA	GND	B31	
NA	GND	C1	
NA	GND	C3	
NA	GND	C29	
NA	GND	C31	
NA	GND	D4	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
NA	GND	D10	
NA	GND	D16	
NA	GND	D22	
NA	GND	D28	
NA	GND	E5	
NA	GND	E27	
NA	GND	F6	
NA	GND	F26	
NA	GND	G7	
NA	GND	G13	
NA	GND	G16	
NA	GND	G19	
NA	GND	G25	
NA	GND	H2	
NA	GND	H8	
NA	GND	H24	
NA	GND	H30	
NA	GND	J9	
NA	GND	J23	
NA	GND	K4	
NA	GND	K16	
NA	GND	K28	
NA	GND	N7	
NA	GND	N25	
NA	GND	P14	
NA	GND	P15	
NA	GND	P16	
NA	GND	P17	
NA	GND	P18	
NA	GND	R14	
NA	GND	R15	
NA	GND	R16	
NA	GND	R17	
NA	GND	R18	
NA	GND	T1	
NA	GND	T4	
NA	GND	T7	
NA	GND	T10	