AMD Xilinx - XC2V8000-4FF1517I Datasheet

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	11648
Number of Logic Elements/Cells	-
Total RAM Bits	3096576
Number of I/O	1108
Number of Gates	8000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FCBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v8000-4ff1517i

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Virtex-II Data Sheet

The Virtex-II Data Sheet contains the following modules:

- Virtex-II Platform FPGAs: Introduction and Overview (Module 1)
- Virtex-II Platform FPGAs: Functional Description (Module 2)
- Virtex-II Platform FPGAs: DC and Switching Characteristics (Module 3)
- Virtex-II Platform FPGAs: Pinout Information (Module 4)

Table 2: **Recommended Operating Conditions**

Symbol	Description	Temperature Range and Grade		Min	Max	Units
V_{CCINT}	Internal supply voltage relative to GND	T_J = 0 °C to +85°C	Commercial	1.425	1.575	V
		T_J = –40°C to +100°C	Industrial	1.425	1.575	V
V_{CCAUX}	Auxiliary supply voltage relative to GND	T_J = 0 °C to +85°C	Commercial	3.135	3.465	V
		T_J = –40°C to +100°C	Industrial	3.135	3.465	V
V_{CCO}	Supply voltage relative to GND	T_J = 0 °C to +85°C	Commercial	1.2	3.6	V
		T_J = –40°C to +100°C	Industrial	1.2	3.6	V
V_{BATT}(1)	Battery voltage relative to GND	T_J = 0 °C to +85°C	Commercial	1.0	3.6	V
		T_J = –40°C to +100°C	Industrial	1.0	3.6	V

Notes:
1. If battery is not used, connect V_{BATT} to GND or V_{CCAUX}.
2. Recommended maximum voltage droop for V_{CCAUX} is 10 mV/ms.
3. The thresholds for Power On Reset are V_{CCINT} > 1.2V, V_{CCAUX} > 2.5V, and V_{CCO} (Bank 4) > 1.5 V.
4. Limit the noise at the power supply to be within 200 mV peak-to-peak.
5. For power bypassing guidelines, see XAPP623 at www.xilinx.com.

Table 3: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Device	Min	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage	All	1.2		V
V_{DRI}	Data retention V_{CCAUX} voltage	All	2.5		V
I_{REF}	V_{REF} current per pin	All	–10	+10	µA
I_L	Input leakage current	All	–10	+10	µA
C_{IN}	Input capacitance	All		10	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0 V, V_{CCO} = 3.3 V (sample tested)	All	Note (1)	250	µA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 3.6 V (sample tested)	All	Note (1)	250	µA
I_{BATT}	Battery supply current	All	(Note 2)		nA

Notes:
1. Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits.
2. Battery supply current (I_{BATT}):

	Device Unpowered	Device Powered	Units
25°C:	< 50	< 10	nA
85°C:	N/A	< 10	nA

Table 19: **Output Delay Measurement Methodology**

Description	IOSTANDARD Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	50	0	V_{REF}	0.9
SSTL, Class II, 1.8V	SSTL18_II	25	0	V_{REF}	0.9
SSTL, Class I, 2.5V	SSTL2_I	50	0	V_{REF}	1.25
SSTL, Class II, 2.5V	SSTL2_II	25	0	V_{REF}	1.25
SSTL, Class I, 3.3V	SSTL3_I	50	0	V_{REF}	1.5
SSTL, Class II, 3.3V	SSTL3_II	25	0	V_{REF}	1.5
AGP-2X/AGP (Accelerated Graphics Port)	AGP-2X/AGP (rising edge)	50	0	0.94	0
	AGP-2X/AGP (falling edge)	50	0	2.03	3.3
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	50	0	V_{REF}	1.2
LVDS, 3.3V	LVDSEXT_25	50	0	V_{REF}	1.2
LVDSEXT (LVDS Extended Mode), 2.5V	LVDS_33	50	0	V_{REF}	1.2
LVDSEXT, 3.3V	LVDSEXT_33	50	0	V_{REF}	1.2
BLVDS (Bus LVDS), 2.5V	BLVDS_25	1M	0	1.2	0
LDT (HyperTransport), 2.5V	LDT_25	50	0	V_{REF}	0.6
LVPECL (Low-Voltage Positive Electron-Coupled Logic), 3.3V	LVPECL_33	1M	0	1.23	0
LVDCI/HSLVDCI (Low-Voltage Digitally Controlled Impedance), 3.3V	LVDCI_33, HSLVDCI_33	1M	0	1.65	0
LVDCI/HSLVDCI, 2.5V	LVDCI_25, HSLVDCI_25	1M	0	1.25	0
LVDCI/HSLVDCI, 1.8V	LVDCI_18, HSLVDCI_18	1M	0	0.9	0
LVDCI/HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I & II, with DCI	HSTL_I_DCI, HSTL_II_DCI	50	0	V_{REF}	0.75
HSTL, Class III & IV, with DCI	HSTL_III_DCI, HSTL_IV_DCI	50	0	0.9	1.5
HSTL, Class I & II, 1.8V, with DCI	HSTL_I_DCI_18, HSTL_II_DCI_18	50	0	V_{REF}	0.9
HSTL, Class III & IV, 1.8V, with DCI	HSTL_III_DCI_18, HSTL_IV_DCI_18	50	0	1.1	1.8
SSTL (Stub Series Termi.Logic), Class I & II, 1.8V, with DCI	SSTL18_I_DCI, SSTL18_II_DCI	50	0	V_{REF}	0.9
SSTL, Class I & II, 2.5V, with DCI	SSTL2_I_DCI, SSTL2_II_DCI	50	0	V_{REF}	1.25
SSTL, Class I & II, 3.3V, with DCI	SSTL3_I_DCI, SSTL3_II_DCI	50	0	V_{REF}	1.5
GTL (Gunning Transceiver Logic) with DCI	GTL_DCI	50	0	0.8	1.2
GTL Plus with DCI	GTLP_DCI	50	0	1.0	1.5

Notes:
1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. Per PCI specifications.
3. Per PCI-X specifications.

Pin Definitions

Table 4 provides a description of each pin type listed in Virtex-II pinout tables.

Table 4: **Virtex-II Pin Definitions**

Pin Name	Direction	Description
User I/O Pins		
IO_LXXY_#	Input/Output/ Bidirectional	All user I/O pins are capable of differential signalling and can implement LVDS, ULVDS, BLVDS, LVPECL, or LDT pairs. Each user I/O is labeled "**IO_LXXY_#**", where: **IO** indicates a user I/O pin. **LXXY** indicates a differential pair, with **XX** a unique pair in the bank and **Y = P/N** for the positive and negative sides of the differential pair. **#** indicates the bank number (0 through 7)
Dual-Function Pins		
IO_LXXY_#/ZZZ		The dual-function pins are labelled "**IO_LXXY_#/ZZZ**", where **ZZZ** can be one of the following pins: Per Bank - **VRP, VRN,** or **VREF** Globally - **GCLKX(S/P), BUSY/DOUT, INIT_B, D0/DIN – D7, RDWR_B,** or **CS_B**
With /ZZZ:		
D0/DIN, D1, D2, D3, D4, D5, D6, D7	Input/Output	• *In* SelectMAP *mode,* D0 through D7 are configuration data pins. These pins become user I/Os after configuration, unless the SelectMAP port is retained. • *In bit-serial modes,* DIN (D0) is the single-data input. This pin becomes a user I/O after configuration.
CS_B	Input	In SelectMAP mode, this is the active-low Chip Select signal. The pin becomes a user I/O after configuration, unless the SelectMAP port is retained.
RDWR_B	Input	In SelectMAP mode, this is the active-low Write Enable signal. The pin becomes a user I/O after configuration, unless the SelectMAP port is retained.
BUSY/DOUT	Output	• *In* SelectMAP *mode,* BUSY controls the rate at which configuration data is loaded. The pin becomes a user I/O after configuration, unless the SelectMAP port is retained. • *In bit-serial modes,* DOUT provides preamble and configuration data to downstream devices in a daisy-chain. The pin becomes a user I/O after configuration.
INIT_B	Bidirectional (open-drain)	When Low, this pin indicates that the configuration memory is being cleared. When held Low, the start of configuration is delayed. During configuration, a Low on this output indicates that a configuration data error has occurred. The pin becomes a user I/O after configuration.
GCLKx (S/P)	Input/Output	These are clock input pins that connect to Global Clock Buffers. These pins become regular user I/Os when not needed for clocks.
VRP	Input	This pin is for the DCI voltage reference resistor of P transistor (per bank).
VRN	Input	This pin is for the DCI voltage reference resistor of N transistor (per bank).
ALT_VRP	Input	This is the alternative pin for the DCI voltage reference resistor of P transistor.
ALT_VRN	Input	This is the alternative pin for the DCI voltage reference resistor of N transistor.
V_{REF}	Input	These are input threshold voltage pins. They become user I/Os when an external threshold voltage is not needed (per bank).
Dedicated Pins(1)		
CCLK	Input/Output	Configuration clock. Output in Master mode or Input in Slave mode.

Table 6: **FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
1	IO_L92P_1	E11	NC	NC
1	IO_L05N_1	A11	NC	NC
1	IO_L05P_1	B11	NC	NC
1	IO_L04N_1	C11	NC	NC
1	IO_L04P_1/VREF_1	D11	NC	NC
1	IO_L03N_1/VRP_1	A12		
1	IO_L03P_1/VRN_1	B12		
1	IO_L02N_1	C12		
1	IO_L02P_1	D12		
1	IO_L01N_1	B13		
1	IO_L01P_1	C13		
2	IO_L01N_2	C16		
2	IO_L01P_2	D16		
2	IO_L02N_2/VRP_2	D14		
2	IO_L02P_2/VRN_2	D15		
2	IO_L03N_2	E13		
2	IO_L03P_2/VREF_2	E14		
2	IO_L04N_2	E15	NC	
2	IO_L04P_2	E16	NC	
2	IO_L06N_2	F13	NC	
2	IO_L06P_2	F14	NC	
2	IO_L43N_2	F15	NC	NC
2	IO_L43P_2	F16	NC	NC
2	IO_L45N_2	F12	NC	NC
2	IO_L45P_2/VREF_2	G12	NC	NC
2	IO_L91N_2	G13	NC	
2	IO_L91P_2	G14	NC	
2	IO_L93N_2	G15	NC	
2	IO_L93P_2/VREF_2	G16	NC	
2	IO_L94N_2	H13		
2	IO_L94P_2	H14		
2	IO_L96N_2	H15		
2	IO_L96P_2	H16		

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
1	IO_L92P_1	A15		
1	IO_L91N_1	B15		
1	IO_L91P_1/VREF_1	C15		
1	IO_L78N_1	D15	NC	
1	IO_L78P_1	E15	NC	
1	IO_L76N_1	F15	NC	
1	IO_L76P_1	G15	NC	
1	IO_L75N_1/VREF_1	G16	NC	
1	IO_L75P_1	F16	NC	
1	IO_L73N_1	A16	NC	
1	IO_L73P_1	A17	NC	
1	IO_L72N_1	B16		
1	IO_L72P_1	C16		
1	IO_L70N_1	D16		
1	IO_L70P_1	E16		
1	IO_L69N_1/VREF_1	C17		
1	IO_L69P_1	D17		
1	IO_L67N_1	H16		
1	IO_L67P_1	G17		
1	IO_L54N_1	E17		
1	IO_L54P_1	F17		
1	IO_L52N_1	A18		
1	IO_L52P_1	A19		
1	IO_L51N_1/VREF_1	E18		
1	IO_L51P_1	D18		
1	IO_L49N_1	B18		
1	IO_L49P_1	C18		
1	IO_L27N_1/VREF_1	F19	NC	NC
1	IO_L27P_1	F18	NC	NC
1	IO_L25N_1	G18	NC	NC
1	IO_L25P_1	G19	NC	NC
1	IO_L24N_1	B19		
1	IO_L24P_1	C19		
1	IO_L22N_1	D19		
1	IO_L22P_1	E19		
1	IO_L21N_1/VREF_1	A20		
1	IO_L21P_1	A21		

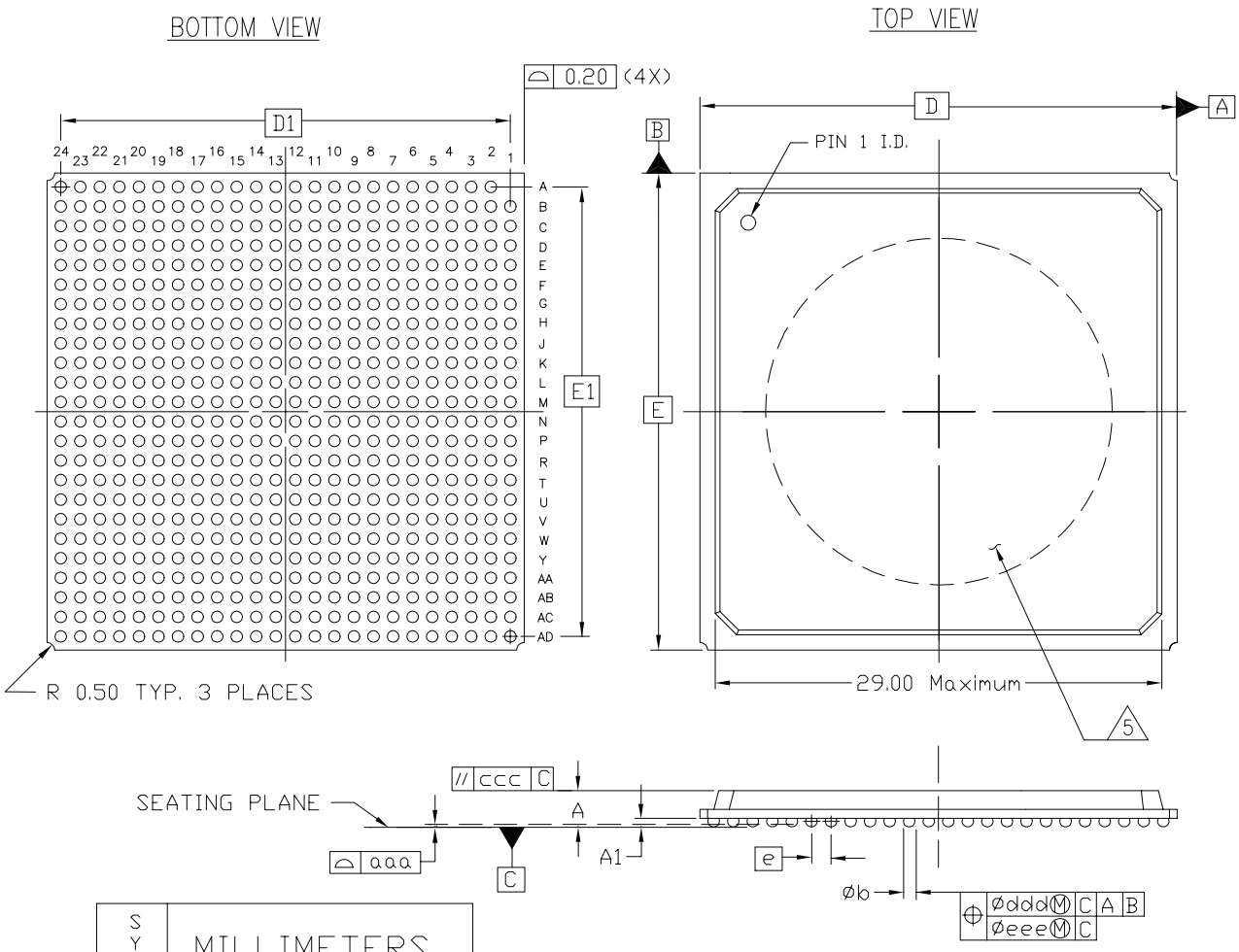
Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
2	IO_L96P_2	N23		
3	IO_L96N_3	N26		
3	IO_L96P_3	P26		
3	IO_L94N_3	P23		
3	IO_L94P_3	P22		
3	IO_L93N_3/VREF_3	P19		
3	IO_L93P_3	N19		
3	IO_L91N_3	P21		
3	IO_L91P_3	P20		
3	IO_L78N_3	R26	NC	
3	IO_L78P_3	R25	NC	
3	IO_L76N_3	R20	NC	
3	IO_L76P_3	R19	NC	
3	IO_L75N_3/VREF_3	R24	NC	
3	IO_L75P_3	R23	NC	
3	IO_L73N_3	R22	NC	
3	IO_L73P_3	R21	NC	
3	IO_L72N_3	T26		
3	IO_L72P_3	T25		
3	IO_L70N_3	T20		
3	IO_L70P_3	T19		
3	IO_L69N_3/VREF_3	T24		
3	IO_L69P_3	T23		
3	IO_L67N_3	T22		
3	IO_L67P_3	T21		
3	IO_L54N_3	U26		
3	IO_L54P_3	V26		
3	IO_L52N_3	U24		
3	IO_L52P_3	U23		
3	IO_L51N_3/VREF_3	U22		
3	IO_L51P_3	U21		
3	IO_L49N_3	V25		
3	IO_L49P_3	V24		
3	IO_L48N_3	V23		
3	IO_L48P_3	V22		
3	IO_L46N_3	W26		

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
NA	VCCINT	H19		
NA	VCCINT	H8		
NA	GND	AF26		
NA	GND	AF1		
NA	GND	AE25		
NA	GND	AE14		
NA	GND	AE13		
NA	GND	AE2		
NA	GND	AD24		
NA	GND	AD3		
NA	GND	AC23		
NA	GND	AC4		
NA	GND	AB22		
NA	GND	AB5		
NA	GND	AA21		
NA	GND	AA6		
NA	GND	U17		
NA	GND	U16		
NA	GND	U15		
NA	GND	U14		
NA	GND	U13		
NA	GND	U12		
NA	GND	U11		
NA	GND	U10		
NA	GND	T17		
NA	GND	T16		
NA	GND	T15		
NA	GND	T14		
NA	GND	T13		
NA	GND	T12		
NA	GND	T11		
NA	GND	T10		
NA	GND	R17		
NA	GND	R16		
NA	GND	R15		
NA	GND	R14		
NA	GND	R13		

BG575/BGG575 Standard BGA Package Specifications (1.27mm pitch)



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A		2.33	2.60
A_1	0.50	0.60	0.70
D/E	31.00 BSC		
D_1/E_1	29.21 REF		
e	1.27BSC		
Øb	0.60	0.75	0.90
aaa			0.20
ccc			0.35
ddd			0.30
eee			0.15
M	24		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-BAN-1 (DEPOPULATED)
4. NO SOLDER BALL AND LAND ON A1.

5 HEAT SINK OPTION

575-BALL MOLDED BGA (BG575/BGG575)

Figure 5: **BG575/BGG575 Standard BGA Package Specifications**

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
2	IO_L21N_2	H7	
2	IO_L21P_2/VREF_2	J7	
2	IO_L22N_2	H6	
2	IO_L22P_2	G6	
2	IO_L23N_2	L10	
2	IO_L23P_2	L9	
2	IO_L24N_2	G3	
2	IO_L24P_2	F3	
2	IO_L25N_2	G2	
2	IO_L25P_2	F2	
2	IO_L26N_2	M10	
2	IO_L26P_2	N10	
2	IO_L27N_2	J6	
2	IO_L27P_2/VREF_2	K6	
2	IO_L28N_2	J5	
2	IO_L28P_2	H5	
2	IO_L29N_2	L7	
2	IO_L29P_2	K7	
2	IO_L30N_2	J4	
2	IO_L30P_2	H4	
2	IO_L43N_2	G1	
2	IO_L43P_2	F1	
2	IO_L44N_2	L8	
2	IO_L44P_2	M8	
2	IO_L45N_2	J1	
2	IO_L45P_2/VREF_2	H2	
2	IO_L46N_2	J3	
2	IO_L46P_2	H3	
2	IO_L47N_2	M9	
2	IO_L47P_2	N9	
2	IO_L48N_2	L5	
2	IO_L48P_2	K5	
2	IO_L49N_2	K2	
2	IO_L49P_2	J2	
2	IO_L50N_2	N7	
2	IO_L50P_2	M7	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
2	IO_L81N_2	R7	NC
2	IO_L81P_2/VREF_2	R6	NC
2	IO_L82N_2	U5	NC
2	IO_L82P_2	T5	NC
2	IO_L83N_2	T10	NC
2	IO_L83P_2	U10	NC
2	IO_L84N_2	U4	NC
2	IO_L84P_2	T4	NC
2	IO_L91N_2	T2	
2	IO_L91P_2	R1	
2	IO_L92N_2	U7	
2	IO_L92P_2	T7	
2	IO_L93N_2	T6	
2	IO_L93P_2/VREF_2	U6	
2	IO_L94N_2	U1	
2	IO_L94P_2	U2	
2	IO_L95N_2	U9	
2	IO_L95P_2	U8	
2	IO_L96N_2	U3	
2	IO_L96P_2	V4	
3	IO_L96N_3	V6	
3	IO_L96P_3	W6	
3	IO_L95N_3	V5	
3	IO_L95P_3	W5	
3	IO_L94N_3	V7	
3	IO_L94P_3	W7	
3	IO_L93N_3/VREF_3	V10	
3	IO_L93P_3	W10	
3	IO_L92N_3	V1	
3	IO_L92P_3	V2	
3	IO_L91N_3	W3	
3	IO_L91P_3	Y3	
3	IO_L84N_3	V9	NC
3	IO_L84P_3	V8	NC
3	IO_L83N_3	W4	NC

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
3	IO_L23P_3	AJ3	
3	IO_L22N_3	AF7	
3	IO_L22P_3	AG7	
3	IO_L21N_3/VREF_3	AL1	
3	IO_L21P_3	AK1	
3	IO_L20N_3	AH2	
3	IO_L20P_3	AJ2	
3	IO_L19N_3	AJ4	
3	IO_L19P_3	AK4	
3	IO_L06N_3	AE10	
3	IO_L06P_3	AD10	
3	IO_L05N_3	AK2	
3	IO_L05P_3	AL2	
3	IO_L04N_3	AH6	
3	IO_L04P_3	AJ5	
3	IO_L03N_3/VREF_3	AE11	
3	IO_L03P_3	AF11	
3	IO_L02N_3/VRP_3	AK3	
3	IO_L02P_3/VRN_3	AL3	
3	IO_L01N_3	AF10	
3	IO_L01P_3	AG9	
4	IO_L01N_4/BUSY/DOUT(1)	AM4	
4	IO_L01P_4/INIT_B	AL5	
4	IO_L02N_4/D0/DIN(1)	AG10	
4	IO_L02P_4/D1	AH11	
4	IO_L03N_4/D2/ALT_VRP_4	AK7	
4	IO_L03P_4/D3/ALT_VRN_4	AK8	
4	IO_L04N_4/VREF_4	AL6	
4	IO_L04P_4	AM6	
4	IO_L05N_4/VRP_4	AK9	
4	IO_L05P_4/VRN_4	AJ8	
4	IO_L06N_4	AM8	
4	IO_L06P_4	AM7	
4	IO_L19N_4	AN3	
4	IO_L19P_4	AM2	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
4	IO_L91N_4/VREF_4	AL16	
4	IO_L91P_4	AL17	
4	IO_L92N_4	AJ17	
4	IO_L92P_4	AJ16	
4	IO_L93N_4	AM15	
4	IO_L93P_4	AM14	
4	IO_L94N_4/VREF_4	AM16	
4	IO_L94P_4	AM17	
4	IO_L95N_4/GCLK3S	AF17	
4	IO_L95P_4/GCLK2P	AG17	
4	IO_L96N_4/GCLK1S	AK16	
4	IO_L96P_4/GCLK0P	AK17	
5	IO_L96N_5/GCLK7S	AK18	
5	IO_L96P_5/GCLK6P	AK19	
5	IO_L95N_5/GCLK5S	AG18	
5	IO_L95P_5/GCLK4P	AF18	
5	IO_L94N_5	AL18	
5	IO_L94P_5/VREF_5	AL19	
5	IO_L93N_5	AJ19	
5	IO_L93P_5	AJ18	
5	IO_L92N_5	AH19	
5	IO_L92P_5	AH18	
5	IO_L91N_5	AM19	
5	IO_L91P_5/VREF_5	AM20	
5	IO_L84N_5	AL21	NC
5	IO_L84P_5	AL20	NC
5	IO_L83N_5	AM22	NC
5	IO_L83P_5	AM21	NC
5	IO_L82N_5	AN18	NC
5	IO_L82P_5	AP18	NC
5	IO_L81N_5/VREF_5	AP20	NC
5	IO_L81P_5	AN19	NC
5	IO_L80N_5	AE18	NC
5	IO_L80P_5	AE19	NC
5	IO_L79N_5	AP22	NC

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
NA	GND	V19	
NA	GND	V18	
NA	GND	V17	
NA	GND	V16	
NA	GND	V15	
NA	GND	V14	
NA	GND	U21	
NA	GND	U20	
NA	GND	U19	
NA	GND	U18	
NA	GND	U17	
NA	GND	U16	
NA	GND	U15	
NA	GND	U14	
NA	GND	T26	
NA	GND	T21	
NA	GND	T20	
NA	GND	T19	
NA	GND	T18	
NA	GND	T17	
NA	GND	T16	
NA	GND	T15	
NA	GND	T14	
NA	GND	T9	
NA	GND	R33	
NA	GND	R21	
NA	GND	R20	
NA	GND	R19	
NA	GND	R18	
NA	GND	R17	
NA	GND	R16	
NA	GND	R15	
NA	GND	R14	
NA	GND	R2	
NA	GND	P28	
NA	GND	P21	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
4	IO_L68P_4	AL17		
4	IO_L69N_4	AT16		
4	IO_L69P_4/VREF_4	AT15		
4	IO_L70N_4	AU14		
4	IO_L70P_4	AU13		
4	IO_L71N_4	AH18		
4	IO_L71P_4	AH19		
4	IO_L72N_4	AN17		
4	IO_L72P_4	AN16		
4	IO_L73N_4	AW15		
4	IO_L73P_4	AW14		
4	IO_L74N_4	AJ18		
4	IO_L74P_4	AJ19		
4	IO_L75N_4	AP17		
4	IO_L75P_4/VREF_4	AP16		
4	IO_L76N_4	AV15		
4	IO_L76P_4	AU15		
4	IO_L77N_4	AK18		
4	IO_L77P_4	AK19		
4	IO_L78N_4	AR18		
4	IO_L78P_4	AR17		
4	IO_L79N_4	AU17		
4	IO_L79P_4	AU16		
4	IO_L80N_4	AL18		
4	IO_L80P_4	AL19		
4	IO_L81N_4	AN19		
4	IO_L81P_4/VREF_4	AN18		
4	IO_L82N_4	AV17		
4	IO_L82P_4	AV16		
4	IO_L83N_4	AM18		
4	IO_L83P_4	AM19		
4	IO_L84N_4	AP19		
4	IO_L84P_4	AP18		
4	IO_L85N_4	AW17	NC	NC
4	IO_L85P_4	AW16	NC	NC
4	IO_L91N_4/VREF_4	AV19		

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
2	IO_L23N_2	E2	
2	IO_L23P_2	F2	
2	IO_L24N_2	H4	
2	IO_L24P_2	J4	
2	IO_L25N_2	K8	NC
2	IO_L25P_2	L8	NC
2	IO_L27N_2	J7	NC
2	IO_L27P_2/VREF_2	K7	NC
2	IO_L43N_2	F1	
2	IO_L43P_2	G1	
2	IO_L44N_2	L9	
2	IO_L44P_2	M9	
2	IO_L45N_2	G2	
2	IO_L45P_2/VREF_2	J2	
2	IO_L46N_2	H3	
2	IO_L46P_2	J3	
2	IO_L47N_2	J6	
2	IO_L47P_2	L6	
2	IO_L48N_2	J5	
2	IO_L48P_2	K5	
2	IO_L49N_2	H1	
2	IO_L49P_2	J1	
2	IO_L50N_2	N10	
2	IO_L50P_2	P10	
2	IO_L51N_2	L7	
2	IO_L51P_2/VREF_2	M7	
2	IO_L52N_2	K3	
2	IO_L52P_2	L3	
2	IO_L53N_2	M8	
2	IO_L53P_2	N8	
2	IO_L54N_2	L5	
2	IO_L54P_2	M5	
2	IO_L67N_2	K2	
2	IO_L67P_2	L2	
2	IO_L68N_2	M6	
2	IO_L68P_2	N6	
2	IO_L69N_2	L4	
2	IO_L69P_2/VREF_2	M4	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
3	IO_L93P_3	V1	
3	IO_L92N_3	U8	
3	IO_L92P_3	W8	
3	IO_L91N_3	U2	
3	IO_L91P_3	V2	
3	IO_L78N_3	U7	
3	IO_L78P_3	V7	
3	IO_L77N_3	U4	
3	IO_L77P_3	V4	
3	IO_L76N_3	W1	
3	IO_L76P_3	Y1	
3	IO_L75N_3/VREF_3	V5	
3	IO_L75P_3	W5	
3	IO_L74N_3	W2	
3	IO_L74P_3	Y2	
3	IO_L73N_3	W6	
3	IO_L73P_3	Y6	
3	IO_L72N_3	Y5	
3	IO_L72P_3	AA5	
3	IO_L71N_3	W3	
3	IO_L71P_3	Y3	
3	IO_L70N_3	W4	
3	IO_L70P_3	Y4	
3	IO_L69N_3/VREF_3	U9	
3	IO_L69P_3	V9	
3	IO_L68N_3	AA1	
3	IO_L68P_3	AB1	
3	IO_L67N_3	Y7	
3	IO_L67P_3	AA7	
3	IO_L54N_3	AA6	
3	IO_L54P_3	AC6	
3	IO_L53N_3	AA2	
3	IO_L53P_3	AB2	
3	IO_L52N_3	AA4	
3	IO_L52P_3	AC4	
3	IO_L51N_3/VREF_3	V10	
3	IO_L51P_3	W10	
3	IO_L50N_3	AA3	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
5	VCCO_5	AJ18	
5	VCCO_5	AJ25	
6	VCCO_6	U20	
6	VCCO_6	U21	
6	VCCO_6	V20	
6	VCCO_6	V21	
6	VCCO_6	V24	
6	VCCO_6	V29	
6	VCCO_6	W20	
6	VCCO_6	W21	
6	VCCO_6	Y21	
6	VCCO_6	AB26	
6	VCCO_6	AE29	
7	VCCO_7	G29	
7	VCCO_7	K26	
7	VCCO_7	M21	
7	VCCO_7	N20	
7	VCCO_7	N21	
7	VCCO_7	P20	
7	VCCO_7	P21	
7	VCCO_7	P24	
7	VCCO_7	P29	
7	VCCO_7	R20	
7	VCCO_7	R21	
NA	CCLK	AJ4	
NA	PROG_B	D27	
NA	DONE	AG6	
NA	M0	AH27	
NA	M1	AJ28	
NA	M2	AG26	
NA	HSWAP_EN	E26	
NA	TCK	K11	
NA	TDI	C28	
NA	TDO	C4	
NA	TMS	J10	
NA	PWRDWN_B	AH5	
NA	DXN	F25	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
NA	DXP	B28	
NA	VBATT	D5	
NA	RSVD	B4	
NA	VCCAUX	B16	
NA	VCCAUX	C2	
NA	VCCAUX	C30	
NA	VCCAUX	T2	
NA	VCCAUX	T30	
NA	VCCAUX	AJ2	
NA	VCCAUX	AJ30	
NA	VCCAUX	AK16	
NA	VCCINT	K15	
NA	VCCINT	K17	
NA	VCCINT	L11	
NA	VCCINT	L16	
NA	VCCINT	L21	
NA	VCCINT	M12	
NA	VCCINT	M16	
NA	VCCINT	M20	
NA	VCCINT	N13	
NA	VCCINT	N14	
NA	VCCINT	N15	
NA	VCCINT	N16	
NA	VCCINT	N17	
NA	VCCINT	N18	
NA	VCCINT	N19	
NA	VCCINT	P13	
NA	VCCINT	P19	
NA	VCCINT	R10	
NA	VCCINT	R13	
NA	VCCINT	R19	
NA	VCCINT	R22	
NA	VCCINT	T11	
NA	VCCINT	T12	
NA	VCCINT	T13	
NA	VCCINT	T19	
NA	VCCINT	T20	

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
11/07/00	1.0	Early access draft.
11/22/00	1.1	Initial Xilinx release. Made the following corrections: CS144 package - Table 5, page 5: • Added missing pin D10 in Bank 1. • Changed dedicated pins A2 and B2 to RSVD (from DXN and DXP). FG256 package - Table 6, page 10: • Changed dedicated pins A3 and A4 to RSVD (from DXN and DXP). FG896 package - Table 11, page 94: • Corrected pin AG1 in Bank 4 to be AG12. FF1152 package - Table 12, page 120: • Corrected pin Y3 in Bank 6 to be Y32.
12/19/00	1.2	Reverse designations were fixed for pins in every package.
01/25/01	1.3	Data sheet divided into four modules (per current style standard). DXN and DXP pin information added for CS144 package (Table 5) and FG256 package (Table 6).
02/07/01	1.4	DXN and DXP pin information was changed back to RSVD for the CS144 package (Table 5) and the FG256 package (Table 6).
04/02/01	1.5	• ALT_VRN and ALT_VRP pin information was added for each package. • Table 8, page 34 – added No Connect designations for the XC2V1500 device in the FG676 package. • Reverted to traditional double-column format.
11/07/01	1.6	• Updated list of devices supported in the FF1152, FF1517, and BF957 packages.
09/26/02	1.7	• Updated Table 3 to reflect devices supported in the BG728 and BF957 packages. • Added mention of LVPECL to pin definition in Table 4.
10/07/02	1.8	• Corrected Table 10 heading to reflect supported devices in the BG728 package.
12/06/02	1.8.1	• Enhanced the description of the PWRDWN_B pin in Table 4.
05/07/03	1.8.2	• Added clarification to Table 4 and all device pinout tables regarding the dual-use nature of pins D0/DIN and BUSY/DOUT during configuration.
06/19/03	1.8.3	• The final GND pin in each of five pinout tables was inadvertently deleted in v1.8.2. This revision restores the deleted GND pins as follows: - Pin C5, Table 5, page 5 (CS144) - Pin A1, Table 6, page 10 (FG256) - Pin A2, Table 10, page 72 (BG728) - Pin A2, Table 12, page 120 (FF1152) - Pin AL30, Table 14, page 198 (BF957)
08/01/03	2.0	All Virtex-II devices and speed grades now Production. See Table 13, Module 3.
03/29/04	2.0.1	Recompiled for backward compatibility with Acrobat 4 and above.
06/24/04	3.3	Added references to, and new package drawings for, Pb-free wire-bond packages CSG, FGG, and BGG. (Revision number advanced to level of complete data sheet.)
03/01/05	3.4	Table 4: Changed Direction for User I/O pins (IO_LXXY_#) from “Input/Output” to “Input/Output/Bidirectional”. Added requirement to V_{BATT} to connect pin to V_{CCAUX} or GND if battery is not used.
11/05/07	3.5	Updated copyright notice and legal disclaimer.