AMD Xilinx - XC2V8000-4FFG1517C Datasheet

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	11648
Number of Logic Elements/Cells	-
Total RAM Bits	3096576
Number of I/O	1108
Number of Gates	8000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FCBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v8000-4ffg1517c

Table 5: **Summary of Voltage Supply Requirements for All Input and Output Standards**

I/O Standard	V_{CCO}		V_{REF}	Termination Type	
	Output	Input	Input	Output	Input
LVDS_33	3.3	N/R	N/R[1]	N/R	N/R
LVDSEXT_33			N/R	N/R	N/R
LVPECL_33			N/R	N/R	N/R
SSTL3_I			1.5	N/R	N/R
SSTL3_II			1.5	N/R	N/R
AGP			1.32	N/R	N/R
LVTTL		3.3	N/R	N/R	N/R
LVCMOS33			N/R	N/R	N/R
LVDCI_33			N/R	Series	N/R
LVDCI_DV2_33			N/R	Series	N/R
PCI33_3			N/R	N/R	N/R
PCI66_3			N/R	N/R	N/R
PCIX			N/R	N/R	N/R
SSTL3_I_DCI			1.5	N/R	Split
SSTL3_II_DCI			1.5	Split	Split
LVDS_25	2.5	N/R	N/R	N/R	N/R
LVDSEXT_25			N/R	N/R	N/R
LDT_25			N/R	N/R	N/R
ULVDS_25			N/R	N/R	N/R
BLVDS_25			N/R	N/R	N/R
SSTL2_I			1.25	N/R	N/R
SSTL2_II			1.25	N/R	N/R
LVCMOS25		2.5	N/R	N/R	N/R
LVDCI_25			N/R	Series	N/R
LVDCI_DV2_25			N/R	Series	N/R
LVDS_25_DCI			N/R	N/R	Split
LVDSEXT_25_DCI			N/R	N/R	Split
SSTL2_I_DCI			1.25	N/R	Split
SSTL2_II_DCI			1.25	Split	Split

Table 5: **Summary of Voltage Supply Requirements for All Input and Output Standards *(Continued)***

I/O Standard	V_{CCO}		V_{REF}	Termination Type	
	Output	Input	Input	Output	Input
HSTL_III_18	1.8	N/R	1.1	N/R	N/R
HSTL_IV_18			1.1	N/R	N/R
HSTL_I_18			0.9	N/R	N/R
HSTL_II_18			0.9	N/R	N/R
SSTL18_I			0.9	N/R	N/R
SSTL18_II			0.9	N/R	N/R
LVCMOS18		1.8	N/R	N/R	N/R
LVDCI_18			N/R	Series	N/R
LVDCI_DV2_18			N/R	Series	N/R
HSTL_III_DCI_18			1.1	N/R	Single
HSTL_IV_DCI_18			1.1	Single	Single
HSTL_I_DCI_18			0.9	N/R	Split
HSTL_II_DCI_18			0.9	Split	Split
SSTL18_I_DCI			0.9	N/R	Split
SSTL18_II_DCI			0.9	Split	Split
HSTL_III	1.5	N/R	0.9	N/R	N/R
HSTL_IV			0.9	N/R	N/R
HSTL_I			0.75	N/R	N/R
HSTL_II			0.75	N/R	N/R
LVCMOS15		1.5	N/R	N/R	N/R
LVDCI_15			N/R	Series	N/R
LVDCI_DV2_15			N/R	Series	N/R
GTLP_DCI			1	Single	Single
HSTL_III_DCI			0.9	N/R	Single
HSTL_IV_DCI			0.9	Single	Single
HSTL_I_DCI			0.75	N/R	Split
HSTL_II_DCI			0.75	Split	Split
GTL_DCI	1.2	1.2	0.8	Single	Single
GTLP	N/R	N/R	1	N/R	N/R
GTL			0.8	N/R	N/R

Notes:
1. N/R = no requirement.

Virtex-II FPGA device. Timing is similar to the Slave Serial-MAP mode except that CCLK is supplied by the Virtex-II FPGA.

Boundary-Scan (JTAG, IEEE 1532) Mode

In Boundary-Scan mode, dedicated pins are used for configuring the Virtex-II device. The configuration is done entirely through the IEEE 1149.1 Test Access Port (TAP). Virtex-II device configuration using Boundary-Scan is compatible with the IEEE 1149.1-1993 standard and the new IEEE 1532 standard for In-System Configurable (ISC) devices. The IEEE 1532 standard is backward compliant with the IEEE 1149.1-1993 TAP and state machine. The IEEE Standard 1532 for In-System Configurable (ISC) devices is intended to be programmed, reprogrammed, or tested on the board via a physical and logical protocol.

Configuration through the Boundary-Scan port is always available, independent of the mode selection. Selecting the Boundary-Scan mode simply turns off the other modes.

Table 25: **Virtex-II Configuration Mode Pin Settings**

Configuration Mode(1)	M2	M1	M0	CCLK Direction	Data Width	Serial D_{OUT}(2)
Master Serial	0	0	0	Out	1	Yes
Slave Serial	1	1	1	In	1	Yes
Master SelectMAP	0	1	1	Out	8	No
Slave SelectMAP	1	1	0	In	8	No
Boundary-Scan	1	0	1	N/A	1	No

Notes:
1. The HSWAP_EN pin controls the pull-ups. Setting M2, M1, and M0 selects the configuration mode, while the HSWAP_EN pin controls whether or not the pull-ups are used.
2. Daisy chaining is possible only in modes where Serial D_{OUT} is used. For example, in SelectMAP modes, the first device does NOT support daisy chaining of downstream devices.

Table 26 lists the total number of bits required to configure each device.

Table 26: **Virtex-II Bitstream Lengths**

Device	# of Configuration Bits
XC2V40	338,976
XC2V80	598,816
XC2V250	1,593,632
XC2V500	2,560,544
XC2V1000	4,082,592
XC2V1500	5,170,208
XC2V2000	6,812,960
XC2V3000	10,494,368
XC2V4000	15,659,936
XC2V6000	21,849,504
XC2V8000	26,194,208

Configuration Sequence

The configuration of Virtex-II devices is a three-phase process after Power On Reset or POR. POR occurs when V_{CCINT} is greater than 1.2V, V_{CCAUX} is greater than 2.5V, and V_{CCO} (bank 4) is greater than 1.5V. Once the POR voltages have been reached, the three-phase process begins.

First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process.

Configuration is automatically initiated on power-up unless it is delayed by the user. The INIT_B pin can be held Low using an open-drain driver. An open-drain is required since INIT_B is a bidirectional open-drain pin that is held Low by a Virtex-II FPGA device while the configuration memory is being cleared. Extending the time that the pin is Low causes the configuration sequencer to wait. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

The configuration process can also be initiated by asserting the PROG_B pin. The end of the memory-clearing phase is signaled by the INIT_B pin going High, and the completion of the entire process is signaled by the DONE pin going High. The Global Set/Reset (GSR) signal is pulsed after the last frame of configuration data is written but before the start-up sequence. The GSR signal resets all flip-flops on the device.

The default start-up sequence is that one CCLK cycle after DONE goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary. One CCLK cycle later, the Global Write Enable (GWE) signal is released. This permits the internal storage ele-

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 18 shows the test setup parameters used for measuring Input standard adjustments (see Table 15, page 11).

Table 18: **Input Delay Measurement Methodology**

Description	IOSTANDARD Attribute	V_L (1,2)	V_H (1,2)	V_{MEAS} (1,4,5)	V_{REF} (1,3,5)
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL	0	3.0	1.4	–
LVCMOS (Low-Voltage CMOS), 3.3V	LVCMOS33	0	3.3	1.65	–
LVCMOS, 2.5V	LVCMOS25	0	2.5	1.25	–
LVCMOS, 1.8V	LVCMOS18	0	1.8	0.9	–
LVCMOS, 1.5V	LVCMOS15	0	1.5	0.75	–
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3	Per PCI Specification			–
PCI, 66 MHz, 3.3V	PCI66_3	Per PCI Specification			–
PCI-X, 133 MHz, 3.3V	PCIX	Per PCI-X Specification			–
GTL (Gunning Transceiver Logic)	GTL	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	0.80
GTL Plus	GTLP	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	1.0
HSTL (High-Speed Transceiver Logic), Class I & II	HSTL_I, HSTL_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.75
HSTL, Class III & IV	HSTL_III, HSTL_IV	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL, Class III & IV, 1.8V	HSTL_III_18, HSTL_IV_18	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	1.08
SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V	SSTL3_I, SSTL3_II	V_{REF} – 1.00	V_{REF} + 1.00	V_{REF}	1.5
SSTL, Class I & II, 2.5V	SSTL2_I, SSTL2_II	V_{REF} – 0.75	V_{REF} + 0.75	V_{REF}	1.25
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
AGP-2X/AGP (Accelerated Graphics Port)	AGP	V_{REF} – (0.2 x V_{CCO})	V_{REF} + (0.2 x V_{CCO})	V_{REF}	AGP Spec
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	1.2 – 0.125	1.2 + 0.125	1.2	
LVDS, 3.3V	LVDS_33	1.2 – 0.125	1.2 + 0.125	1.2	
LVDSEXT (LVDS Extended Mode), 2.5V	LVDSEXT_25	1.2 – 0.125	1.2 + 0.125	1.2	
LVDSEXT, 3.3V	LVDSEXT_33	1.2 – 0.125	1.2 + 0.125	1.2	
ULVDS (Ultra LVDS), 2.5V	ULVDS_25	0.6 – 0.125	0.6 + 0.125	0.6	
LDT (HyperTransport), 2.5V	LDT_25	0.6 – 0.125	0.6 + 0.125	0.6	
LVPECL (Low-Voltage Positive Electron-Coupled Logic), 3.3V	LVPECL_33	1.6 – 0.3	1.6 + 0.3	1.6	

Notes:
1. Input delay measurement methodology parameters for LVDCI and HSLVDCI are the same as for LVCMOS standards of the same voltage. Parameters for all other DCI standards are the same as for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H.
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical. See **Virtex-II Platform FPGA User Guide** for min/max specifications.
4. Input voltage level from which measurement starts.
5. Note that this is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 1.

Input Clock Tolerances

Table 39: **Input Clock Tolerances**

Description	Symbol	Constraints F_{CLKIN}	Speed Grade						Units
			-6		-5		-4		
			Min	Max	Min	Max	Min	Max	
Input Clock Low/High Pulse Width									
PSCLK	PSCLK_PULSE	< 1MHz	25.00		25.00		25.00		ns
PSCLK and CLKIN(3)	PSCLK_PULSE and CLKIN_PULSE	1 – 10 MHz	25.00		25.00		25.00		ns
		10 – 25 MHz	10.00		10.00		10.00		ns
		25 – 50 MHz	5.00		5.00		5.00		ns
		50 – 100 MHz	3.00		3.00		3.00		ns
		100 – 150 MHz	2.40		2.40		2.40		ns
		150 – 200 MHz	2.00		2.00		2.00		ns
		200 – 250 MHz	1.80		1.80		1.80		ns
		250 – 300 MHz	1.50		1.50		1.50		ns
		300 – 350 MHz	1.30		1.30		1.30		ns
		350 – 400 MHz	1.15		1.15		1.15		ns
		> 400 MHz	1.05		1.05		1.05		ns
Input Clock Cycle-Cycle Jitter (Low Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_CYC_JITT_DLL_LF			±300		±300		±300	ps
CLKIN (using CLKFX outputs)(2)	CLKIN_CYC_JITT_FX_LF			±300		±300		±300	ps
Input Clock Cycle-Cycle Jitter (High Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_CYC_JITT_DLL_HF			±150		±150		±150	ps
CLKIN (using CLKFX outputs)(2)	CLKIN_CYC_JITT_FX_HF			±150		±150		±150	ps
Input Clock Period Jitter (Low Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_PER_JITT_DLL_LF			±1		±1		±1	ns
CLKIN (using CLKFX outputs)(2)	CLKIN_PER_JITT_FX_LF			±1		±1		±1	ns
Input Clock Period Jitter (High Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_PER_JITT_DLL_HF			±1		±1		±1	ns
CLKIN (using CLKFX outputs)(2)	CLKIN_PER_JITT_FX_HF			±1		±1		±1	ns
Feedback Clock Path Delay Variation									
CLKFB off-chip feedback	CLKFB_DELAY_VAR_EXT			±1		±1		±1	ns

Notes:
1. "DLL outputs" is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. If both DLL and CLKFX outputs are used, follow the more restrictive specification.
3. If DCM phase shift feature is used and CLKIN frequency > 200 Mhz, CLKIN duty cycle must be within ±5% (45/55 to 55/45).

Virtex-II Platform FPGAs: Pinout Information

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Product Specification

This document provides Virtex-II™ Device/Package Combinations, Maximum I/Os Available, and Virtex-II Pin Definitions, followed by pinout tables for the following packages:

- CS144/CSG144 Chip-Scale BGA Package
- FG256/FGG256 Fine-Pitch BGA Package
- FG456/FGG456 Fine-Pitch BGA Package
- FG676/FGG676 Fine-Pitch BGA Package
- BG575/BGG575 Standard BGA Package
- BG728/BGG728 Standard BGA Package
- FF896 Flip-Chip Fine-Pitch BGA Package
- FF1152 Flip-Chip Fine-Pitch BGA Package
- FF1517 Flip-Chip Fine-Pitch BGA Package
- BF957 Flip-Chip BGA Package

For device pinout diagrams and layout guidelines, refer to the ***Virtex-II Platform FPGA User Guide***. ASCII package pinout files are also available for download from the Xilinx website (**www.xilinx.com**).

Virtex-II Device/Package Combinations and Maximum I/Os Available

Wire-bond and flip-chip packages are available. Table 1 and Table 2 show the maximum number of user I/Os possible in wire-bond and flip-chip packages, respectively.

Table 3 shows the number of user I/Os available for all device/package combinations.

- CS denotes wire-bond chip-scale ball grid array (BGA) (0.80 mm pitch).
- CSG denotes Pb-free wire-bond chip-scale ball grid array (BGA) (0.80 mm pitch).
- FG denotes wire-bond fine-pitch BGA (1.00 mm pitch).
- FGG denotes Pb-free wire-bond fine-pitch BGA (1.00 mm pitch).
- BG denotes standard BGA (1.27 mm pitch).
- BGG denotes Pb-free standard BGA (1.27 mm pitch).
- FF denotes flip-chip fine-pitch BGA (1.00 mm pitch).
- BF denotes flip-chip BGA (1.27 mm pitch).

The number of I/Os per package include all user I/Os except the 15 control pins (CCLK, DONE, M0, M1, M2, PROG_B, PWRDWN_B, TCK, TDI, TDO, TMS, HSWAP_EN, DXN, DXP, AND RSVD).

Table 1: **Wire-Bond Packages Information**

Package[1]	CS144/ CSG144	FG256/ FGG256	FG456/ FGG456	FG676/ FGG676	BG575/ BGG575	BG728/ BGG728
Pitch (mm)	0.80	1.00	1.00	1.00	1.27	1.27
Size (mm)	12 x 12	17 x 17	23 x 23	27 x 27	31 x 31	35 x 35
I/Os	92	172	324	484	408	516

Notes:
1. Wire-bond packages include FGG*nnn* Pb-free versions. See Virtex-II Ordering Examples (Module 1).

Table 2: **Flip-Chip Packages Information**

Package	FF896	FF1152	FF1517	BF957
Pitch (mm)	1.00	1.00	1.00	1.27
Size (mm)	31 x 31	35 x 35	40 x 40	40 x 40
I/Os	624	824	1,108	684

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
NA	GND	M10		
NA	GND	M9		
NA	GND	L14		
NA	GND	L13		
NA	GND	L12		
NA	GND	L11		
NA	GND	L10		
NA	GND	L9		
NA	GND	K14		
NA	GND	K13		
NA	GND	K12		
NA	GND	K11		
NA	GND	K10		
NA	GND	K9		
NA	GND	J14		
NA	GND	J13		
NA	GND	J12		
NA	GND	J11		
NA	GND	J10		
NA	GND	J9		
NA	GND	D19		
NA	GND	D4		
NA	GND	C20		
NA	GND	C3		
NA	GND	B21		
NA	GND	B2		
NA	GND	A22		
NA	GND	A1		

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
7	IO_L21P_7/VREF_7	F3		
7	IO_L21N_7	F2		
7	IO_L19P_7	H6		
7	IO_L19N_7	H7		
7	IO_L06P_7	E1		
7	IO_L06N_7	E2		
7	IO_L04P_7	D1		
7	IO_L04N_7	D2		
7	IO_L03P_7/VREF_7	C1		
7	IO_L03N_7	C2		
7	IO_L02P_7/VRN_7	E3		
7	IO_L02N_7/VRP_7	E4		
7	IO_L01P_7	G5		
7	IO_L01N_7	F4		
0	VCCO_0	J13		
0	VCCO_0	J12		
0	VCCO_0	J11		
0	VCCO_0	H10		
0	VCCO_0	H9		
0	VCCO_0	B10		
0	VCCO_0	B7		
1	VCCO_1	B17		
1	VCCO_1	J16		
1	VCCO_1	J15		
1	VCCO_1	J14		
1	VCCO_1	H18		
1	VCCO_1	H17		
1	VCCO_1	B20		
2	VCCO_2	N18		
2	VCCO_2	M18		
2	VCCO_2	L18		
2	VCCO_2	K25		
2	VCCO_2	K19		
2	VCCO_2	J19		
2	VCCO_2	G25		
3	VCCO_3	Y25		

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
NA	VCCINT	H19		
NA	VCCINT	H8		
NA	GND	AF26		
NA	GND	AF1		
NA	GND	AE25		
NA	GND	AE14		
NA	GND	AE13		
NA	GND	AE2		
NA	GND	AD24		
NA	GND	AD3		
NA	GND	AC23		
NA	GND	AC4		
NA	GND	AB22		
NA	GND	AB5		
NA	GND	AA21		
NA	GND	AA6		
NA	GND	U17		
NA	GND	U16		
NA	GND	U15		
NA	GND	U14		
NA	GND	U13		
NA	GND	U12		
NA	GND	U11		
NA	GND	U10		
NA	GND	T17		
NA	GND	T16		
NA	GND	T15		
NA	GND	T14		
NA	GND	T13		
NA	GND	T12		
NA	GND	T11		
NA	GND	T10		
NA	GND	R17		
NA	GND	R16		
NA	GND	R15		
NA	GND	R14		
NA	GND	R13		

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
5	IO_L52N_5	AA9		
5	IO_L52P_5	Y9		
5	IO_L51N_5/VREF_5	W9		
5	IO_L51P_5	V9		
5	IO_L49N_5	AD8		
5	IO_L49P_5	AD6		
5	IO_L24N_5	AC8		
5	IO_L24P_5	AC7		
5	IO_L22N_5	AB8		
5	IO_L22P_5	AA8		
5	IO_L21N_5/VREF_5	W8		
5	IO_L21P_5	Y8		
5	IO_L19N_5	AD5		
5	IO_L19P_5	AD4		
5	IO_L06N_5	AC6		
5	IO_L06P_5	AC5		
5	IO_L05N_5/VRP_5	AB7		
5	IO_L05P_5/VRN_5	AA7		
5	IO_L04N_5	AB5		
5	IO_L04P_5/VREF_5	AA5		
5	IO_L03N_5/D4/ALT_VRP_5	AA6		
5	IO_L03P_5/D5/ALT_VRN_5	Y6		
5	IO_L02N_5/D6	Y7		
5	IO_L02P_5/D7	W7		
5	IO_L01N_5/RDWR_B	V8		
5	IO_L01P_5/CS_B	U9		
6	IO_L01P_6	AB2		
6	IO_L01N_6	AB1		
6	IO_L02P_6/VRN_6	AA3		
6	IO_L02N_6/VRP_6	AA2		
6	IO_L03P_6	Y4		
6	IO_L03N_6/VREF_6	Y3		
6	IO_L04P_6	W4		
6	IO_L04N_6	W5		
6	IO_L06P_6	V5		

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
1	VCCO_1	G16
1	VCCO_1	D21
1	VCCO_1	C16
2	VCCO_2	N18
2	VCCO_2	M25
2	VCCO_2	M21
2	VCCO_2	M18
2	VCCO_2	L19
2	VCCO_2	L18
2	VCCO_2	K19
2	VCCO_2	G24
3	VCCO_3	AA24
3	VCCO_3	V19
3	VCCO_3	U19
3	VCCO_3	U18
3	VCCO_3	T25
3	VCCO_3	T21
3	VCCO_3	T18
3	VCCO_3	R18
4	VCCO_4	AE16
4	VCCO_4	AD21
4	VCCO_4	AA16
4	VCCO_4	W18
4	VCCO_4	W17
4	VCCO_4	V17
4	VCCO_4	V16
4	VCCO_4	V15
5	VCCO_5	AE12
5	VCCO_5	AD7
5	VCCO_5	AA12
5	VCCO_5	W11
5	VCCO_5	W10
5	VCCO_5	V13
5	VCCO_5	V12
5	VCCO_5	V11
6	VCCO_6	AA4

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
4	IO_L73P_4	AJ12	NC	NC
4	IO_L74N_4	AE13	NC	NC
4	IO_L74P_4	AE14	NC	NC
4	IO_L75N_4	AF13	NC	NC
4	IO_L75P_4/VREF_4	AG13	NC	NC
4	IO_L76N_4	AK13	NC	NC
4	IO_L76P_4	AK12	NC	NC
4	IO_L77N_4	AB14	NC	NC
4	IO_L77P_4	AB15	NC	NC
4	IO_L78N_4	AF15	NC	NC
4	IO_L78P_4	AF14	NC	NC
4	IO_L91N_4/VREF_4	AJ14		
4	IO_L91P_4	AJ15		
4	IO_L92N_4	AC14		
4	IO_L92P_4	AC15		
4	IO_L93N_4	AG15		
4	IO_L93P_4	AG14		
4	IO_L94N_4/VREF_4	AK14		
4	IO_L94P_4	AK15		
4	IO_L95N_4/GCLK3S	AD15		
4	IO_L95P_4/GCLK2P	AE15		
4	IO_L96N_4/GCLK1S	AH14		
4	IO_L96P_4/GCLK0P	AH15		
5	IO_L96N_5/GCLK7S	AH16		
5	IO_L96P_5/GCLK6P	AH17		
5	IO_L95N_5/GCLK5S	AE16		
5	IO_L95P_5/GCLK4P	AD16		
5	IO_L94N_5	AJ16		
5	IO_L94P_5/VREF_5	AJ17		
5	IO_L93N_5	AG17		
5	IO_L93P_5	AG16		
5	IO_L92N_5	AC16		
5	IO_L92P_5	AC17		
5	IO_L91N_5	AK17		
5	IO_L91P_5/VREF_5	AK18		
5	IO_L78N_5	AF17	NC	NC

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
1	IO_L33N_1/VREF_1	D11	NC	
1	IO_L33P_1	D12	NC	
1	IO_L32N_1	H14	NC	
1	IO_L32P_1	H13	NC	
1	IO_L31N_1	A8	NC	
1	IO_L31P_1	A9	NC	
1	IO_L30N_1	F11		
1	IO_L30P_1	F12		
1	IO_L29N_1	K14		
1	IO_L29P_1	L14		
1	IO_L28N_1	C9		
1	IO_L28P_1	C10		
1	IO_L27N_1/VREF_1	G11		
1	IO_L27P_1	G12		
1	IO_L26N_1	M15		
1	IO_L26P_1	M14		
1	IO_L25N_1	B7		
1	IO_L25P_1	B8		
1	IO_L24N_1	D9		
1	IO_L24P_1	D10		
1	IO_L23N_1	J13		
1	IO_L23P_1	J12		
1	IO_L22N_1	A6		
1	IO_L22P_1	A7		
1	IO_L21N_1/VREF_1	E9		
1	IO_L21P_1	E10		
1	IO_L20N_1	D8		
1	IO_L20P_1	E7		
1	IO_L19N_1	C7		
1	IO_L19P_1	C8		
1	IO_L12N_1	F9	NC	
1	IO_L12P_1	F10	NC	
1	IO_L11N_1	H12	NC	
1	IO_L11P_1	H11	NC	
1	IO_L10N_1	B5	NC	
1	IO_L10P_1	B6	NC	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
1	IO_L09N_1/VREF_1	G9	NC	
1	IO_L09P_1	G10	NC	
1	IO_L08N_1	K13	NC	
1	IO_L08P_1	K12	NC	
1	IO_L07N_1	A4	NC	
1	IO_L07P_1	A5	NC	
1	IO_L06N_1	F8		
1	IO_L06P_1	E8		
1	IO_L05N_1	J11		
1	IO_L05P_1	K11		
1	IO_L04N_1	C5		
1	IO_L04P_1/VREF_1	C6		
1	IO_L03N_1/VRP_1	D6		
1	IO_L03P_1/VRN_1	D7		
1	IO_L02N_1	H10		
1	IO_L02P_1	J10		
1	IO_L01N_1	C4		
1	IO_L01P_1	B4		
2	IO_L01N_2	E3		
2	IO_L01P_2	D2		
2	IO_L02N_2/VRP_2	L13		
2	IO_L02P_2/VRN_2	M13		
2	IO_L03N_2	F4		
2	IO_L03P_2/VREF_2	E4		
2	IO_L04N_2	E1		
2	IO_L04P_2	D1		
2	IO_L05N_2	L12		
2	IO_L05P_2	M11		
2	IO_L06N_2	G6		
2	IO_L06P_2	F5		
2	IO_L07N_2	F2	NC	
2	IO_L07P_2	E2	NC	
2	IO_L08N_2	M12	NC	
2	IO_L08P_2	N12	NC	
2	IO_L09N_2	H6	NC	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
7	IO_L26P_7	M31		
7	IO_L26N_7	L31		
7	IO_L25P_7	G38		
7	IO_L25N_7	H38		
7	IO_L24P_7	J34		
7	IO_L24N_7	K34		
7	IO_L23P_7	K32		
7	IO_L23N_7	K31		
7	IO_L22P_7	F39		
7	IO_L22N_7	G39		
7	IO_L21P_7/VREF_7	G36		
7	IO_L21N_7	H36		
7	IO_L20P_7	N28		
7	IO_L20N_7	M28		
7	IO_L19P_7	G37		
7	IO_L19N_7	H37		
7	IO_L12P_7	J33	NC	
7	IO_L12N_7	K33	NC	
7	IO_L11P_7	M29	NC	
7	IO_L11N_7	L28	NC	
7	IO_L10P_7	E38	NC	
7	IO_L10N_7	F38	NC	
7	IO_L09P_7/VREF_7	G35	NC	
7	IO_L09N_7	H35	NC	
7	IO_L08P_7	L30	NC	
7	IO_L08N_7	K29	NC	
7	IO_L07P_7	D39	NC	
7	IO_L07N_7	E39	NC	
7	IO_L06P_7	G34		
7	IO_L06N_7	H34		
7	IO_L05P_7	J32		
7	IO_L05N_7	H33		
7	IO_L04P_7	F36		
7	IO_L04N_7	F37		
7	IO_L03P_7/VREF_7	E36		
7	IO_L03N_7	F35		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	GND	AR26		
NA	GND	AR14		
NA	GND	AR5		
NA	GND	AP34		
NA	GND	AP6		
NA	GND	AN33		
NA	GND	AN20		
NA	GND	AN7		
NA	GND	AM32		
NA	GND	AM23		
NA	GND	AM17		
NA	GND	AM8		
NA	GND	AL31		
NA	GND	AL9		
NA	GND	AK30		
NA	GND	AK20		
NA	GND	AK10		
NA	GND	AJ38		
NA	GND	AJ29		
NA	GND	AJ11		
NA	GND	AJ2		
NA	GND	AF35		
NA	GND	AF5		
NA	GND	AD23		
NA	GND	AD22		
NA	GND	AD21		
NA	GND	AD20		
NA	GND	AD19		
NA	GND	AD18		
NA	GND	AD17		
NA	GND	AC36		
NA	GND	AC32		
NA	GND	AC24		
NA	GND	AC23		
NA	GND	AC22		
NA	GND	AC21		

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
1	IO_L71P_1	B12	
1	IO_L70N_1	C13	
1	IO_L70P_1	C12	
1	IO_L69N_1/VREF_1	H13	
1	IO_L69P_1	H12	
1	IO_L68N_1	D12	
1	IO_L68P_1	D11	
1	IO_L67N_1	B11	
1	IO_L67P_1	B10	
1	IO_L54N_1	E12	
1	IO_L54P_1	E11	
1	IO_L53N_1	A11	
1	IO_L53P_1	A10	
1	IO_L52N_1	G12	
1	IO_L52P_1	G11	
1	IO_L51N_1/VREF_1	K13	
1	IO_L51P_1	K12	
1	IO_L50N_1	C11	
1	IO_L50P_1	C10	
1	IO_L49N_1	B9	
1	IO_L49P_1	B7	
1	IO_L30N_1	F11	NC
1	IO_L30P_1	F9	NC
1	IO_L29N_1	A9	NC
1	IO_L29P_1	A8	NC
1	IO_L27N_1/VREF_1	D9	NC
1	IO_L27P_1	D8	NC
1	IO_L26N_1	J12	NC
1	IO_L26P_1	J11	NC
1	IO_L25N_1	C9	NC
1	IO_L25P_1	C8	NC
1	IO_L24N_1	E10	
1	IO_L24P_1	E9	
1	IO_L23N_1	H11	
1	IO_L23P_1	H10	
1	IO_L22N_1	A7	
1	IO_L22P_1	A6	
1	IO_L21N_1/VREF_1	A5	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
4	IO_L78N_4	AJ13	
4	IO_L78P_4	AK13	
4	IO_L91N_4/VREF_4	AC15	
4	IO_L91P_4	AC16	
4	IO_L92N_4	AG14	
4	IO_L92P_4	AG15	
4	IO_L93N_4	AK14	
4	IO_L93P_4	AK15	
4	IO_L94N_4/VREF_4	AF16	
4	IO_L94P_4	AG16	
4	IO_L95N_4/GCLK3S	AL14	
4	IO_L95P_4/GCLK2P	AL15	
4	IO_L96N_4/GCLK1S	AH15	
4	IO_L96P_4/GCLK0P	AJ15	
5	IO_L96N_5/GCLK7S	AJ16	
5	IO_L96P_5/GCLK6P	AH17	
5	IO_L95N_5/GCLK5S	AD16	
5	IO_L95P_5/GCLK4P	AD17	
5	IO_L94N_5	AL17	
5	IO_L94P_5/VREF_5	AL18	
5	IO_L93N_5	AG17	
5	IO_L93P_5	AF17	
5	IO_L92N_5	AE17	
5	IO_L92P_5	AE18	
5	IO_L91N_5	AK17	
5	IO_L91P_5/VREF_5	AJ17	
5	IO_L78N_5	AK18	
5	IO_L78P_5	AK19	
5	IO_L77N_5	AC17	
5	IO_L77P_5	AB18	
5	IO_L76N_5	AH18	
5	IO_L76P_5	AH19	
5	IO_L75N_5/VREF_5	AL19	
5	IO_L75P_5	AL20	
5	IO_L74N_5	AC18	
5	IO_L74P_5	AC19	
5	IO_L73N_5	AJ19	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
5	IO_L73P_5	AJ20	
5	IO_L72N_5	AG18	
5	IO_L72P_5	AG19	
5	IO_L71N_5	AF18	
5	IO_L71P_5	AF19	
5	IO_L70N_5	AK20	
5	IO_L70P_5	AK21	
5	IO_L69N_5/VREF_5	AH20	
5	IO_L69P_5	AH21	
5	IO_L68N_5	AD19	
5	IO_L68P_5	AD20	
5	IO_L67N_5	AL21	
5	IO_L67P_5	AL22	
5	IO_L54N_5	AG20	
5	IO_L54P_5	AG21	
5	IO_L53N_5	AB19	
5	IO_L53P_5	AB20	
5	IO_L52N_5	AJ21	
5	IO_L52P_5	AJ22	
5	IO_L51N_5/VREF_5	AF20	
5	IO_L51P_5	AF21	
5	IO_L50N_5	AE20	
5	IO_L50P_5	AE21	
5	IO_L49N_5	AK22	
5	IO_L49P_5	AK23	
5	IO_L30N_5	AJ23	NC
5	IO_L30P_5	AJ24	NC
5	IO_L29N_5	AC20	NC
5	IO_L29P_5	AC21	NC
5	IO_L28N_5	AL23	NC
5	IO_L28P_5	AL24	NC
5	IO_L27N_5/VREF_5	AL25	NC
5	IO_L27P_5	AL26	NC
5	IO_L26N_5	AD21	NC
5	IO_L26P_5	AD22	NC
5	IO_L25N_5	AH23	NC
5	IO_L25P_5	AH24	NC
5	IO_L24N_5	AG22	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
NA	GND	T14	
NA	GND	T15	
NA	GND	T16	
NA	GND	T17	
NA	GND	T18	
NA	GND	T22	
NA	GND	T25	
NA	GND	T28	
NA	GND	T31	
NA	GND	U14	
NA	GND	U15	
NA	GND	U16	
NA	GND	U17	
NA	GND	U18	
NA	GND	V14	
NA	GND	V15	
NA	GND	V16	
NA	GND	V17	
NA	GND	V18	
NA	GND	W7	
NA	GND	W25	
NA	GND	AB4	
NA	GND	AB16	
NA	GND	AB28	
NA	GND	AC9	
NA	GND	AC23	
NA	GND	AD2	
NA	GND	AD8	
NA	GND	AD24	
NA	GND	AD30	
NA	GND	AE7	
NA	GND	AE13	
NA	GND	AE16	
NA	GND	AE19	
NA	GND	AE25	
NA	GND	AF6	
NA	GND	AF26	
NA	GND	AG5	

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
11/07/00	1.0	Early access draft.
11/22/00	1.1	Initial Xilinx release. Made the following corrections: CS144 package - Table 5, page 5: • Added missing pin D10 in Bank 1. • Changed dedicated pins A2 and B2 to RSVD (from DXN and DXP). FG256 package - Table 6, page 10: • Changed dedicated pins A3 and A4 to RSVD (from DXN and DXP). FG896 package - Table 11, page 94: • Corrected pin AG1 in Bank 4 to be AG12. FF1152 package - Table 12, page 120: • Corrected pin Y3 in Bank 6 to be Y32.
12/19/00	1.2	Reverse designations were fixed for pins in every package.
01/25/01	1.3	Data sheet divided into four modules (per current style standard). DXN and DXP pin information added for CS144 package (Table 5) and FG256 package (Table 6).
02/07/01	1.4	DXN and DXP pin information was changed back to RSVD for the CS144 package (Table 5) and the FG256 package (Table 6).
04/02/01	1.5	• ALT_VRN and ALT_VRP pin information was added for each package. • Table 8, page 34 – added No Connect designations for the XC2V1500 device in the FG676 package. • Reverted to traditional double-column format.
11/07/01	1.6	• Updated list of devices supported in the FF1152, FF1517, and BF957 packages.
09/26/02	1.7	• Updated Table 3 to reflect devices supported in the BG728 and BF957 packages. • Added mention of LVPECL to pin definition in Table 4.
10/07/02	1.8	• Corrected Table 10 heading to reflect supported devices in the BG728 package.
12/06/02	1.8.1	• Enhanced the description of the PWRDWN_B pin in Table 4.
05/07/03	1.8.2	• Added clarification to Table 4 and all device pinout tables regarding the dual-use nature of pins D0/DIN and BUSY/DOUT during configuration.
06/19/03	1.8.3	• The final GND pin in each of five pinout tables was inadvertently deleted in v1.8.2. This revision restores the deleted GND pins as follows: - Pin C5, Table 5, page 5 (CS144) - Pin A1, Table 6, page 10 (FG256) - Pin A2, Table 10, page 72 (BG728) - Pin A2, Table 12, page 120 (FF1152) - Pin AL30, Table 14, page 198 (BF957)
08/01/03	2.0	All Virtex-II devices and speed grades now Production. See Table 13, Module 3.
03/29/04	2.0.1	Recompiled for backward compatibility with Acrobat 4 and above.
06/24/04	3.3	Added references to, and new package drawings for, Pb-free wire-bond packages CSG, FGG, and BGG. (Revision number advanced to level of complete data sheet.)
03/01/05	3.4	Table 4: Changed Direction for User I/O pins (IO_LXXY_#) from “Input/Output” to “Input/Output/Bidirectional”. Added requirement to V_{BATT} to connect pin to V_{CCAUX} or GND if battery is not used.
11/05/07	3.5	Updated copyright notice and legal disclaimer.