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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 11648 |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 3096576 |
| Number of I/O | 1108 |
| Number of Gates | 8000000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 1517-BBGA, FCBGA |
| Supplier Device Package | 1517-FCBGA (40x40) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc2v8000-4ffg1517i |

The Virtex-II implementation process is comprised of Synthesis, translation, mapping, place and route, and configuration file generation. While the tools can be run individually, many designers choose to run the entire implementation process with the click of a button. To assist those who prefer to script their design flows, Xilinx provides Xflow, an automated single command line process.

### *Design Verification*

In addition to conventional design verification using static timing analysis or simulation techniques, Xilinx offers powerful in-circuit debugging techniques using ChipScope ILA (Integrated Logic Analysis). The reconfigurable nature of Xilinx FPGAs means that designs can be verified in real time without the need for extensive sets of software simulation vectors.

For simulation, the system extracts post-layout timing information from the design database, and back-annotates this information into the netlist for use by the simulator. The back annotation features a variety of patented Xilinx techniques, resulting in the industry's most powerful simulation flows. Alternatively, timing-critical portions of a design can be verified using the Xilinx static timing analyzer or a third party static timing analysis tool like Synopsys Prime Time™, by exporting timing data in the STAMP data format.

For in-circuit debugging, ChipScope ILA enables designers to analyze the real-time behavior of a device while operating at full system speeds. Logic analysis commands and captured data are transferred between the ChipScope software and ILA cores within the Virtex-II FPGA, using industry standard JTAG protocols. These JTAG transactions are driven over an optional download cable (MultiLINX or JTAG), connecting the Virtex device in the target system to a PC or workstation.

ChipScope ILA was designed to look and feel like a logic analyzer, making it easy to begin debugging a design immediately. Modifications to the desired logic analysis can be downloaded directly into the system in a matter of minutes.

## Other Unique Features of Virtex-II Design Flow

Xilinx design flows feature a number of unique capabilities. Among these are efficient incremental HDL design flows; a robust capability that is enabled by Xilinx exclusive hierarchical floorplanning capabilities. Another powerful design capability only available in the Xilinx design flow is "Modular Design", part of the Xilinx suite of team design tools, which enables autonomous design, implementation, and verification of design modules.

### *Incremental Synthesis*

Xilinx unique hierarchical floorplanning capabilities enable designers to create a programmable logic design by isolating design changes within one hierarchical "logic block", and perform synthesis, verification and implementation processes on that specific logic block. By preserving the logic in unchanged portions of a design, Xilinx incremental design makes the high-density design process more efficient.

Xilinx hierarchical floorplanning capabilities can be specified using the high-level floorplanner or a preferred RTL floorplanner (see the Xilinx web site for a list of supported EDA partners). When used in conjunction with one of the EDA partners' floorplanners, higher performance results can be achieved, as many synthesis tools use this more predictable detailed physical implementation information to establish more aggressive and accurate timing estimates when performing their logic optimizations.

### *Modular Design*

Xilinx innovative modular design capabilities take the incremental design process one step further by enabling the designer to delegate responsibility for completing the design, synthesis, verification, and implementation of a hierarchical "logic block" to an arbitrary number of designers - assigning a specific region within the target FPGA for exclusive use by each of the team members.

This team design capability enables an autonomous approach to design modules, changing the hand-off point to the lead designer or integrator from "my module works in simulation" to "my module works in the FPGA". This unique design methodology also leverages the Xilinx hierarchical floorplanning capabilities and enables the Xilinx (or EDA partner) floorplanner to manage the efficient implementation of very high-density FPGAs.

# Virtex-II Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex-II devices. The numbers reported here are worst-case values; they have all been fully characterized. Note that these values are subject to the same guidelines as Virtex-II Switching Characteristics, page 9 (speed files).

Table 11 provides pin-to-pin values (in nanoseconds) including IOB delays; that is, delay through the device from input pin to output pin. In the case of multiple inputs and outputs, the worst delay is reported.

*Table 11:* **Pin-to-Pin Performance**

| Description | Device Used & Speed Grade | Pin-to-Pin (with I/O delays) | Units |
|---|---|---|---|
| **Basic Functions** | | | |
| 16-bit Address Decoder | XC2V1000 -5 | 6.3 | ns |
| 32-bit Address Decoder | XC2V1000 -5 | 7.7 | ns |
| 64-bit Address Decoder | XC2V1000 -5 | 9.3 | ns |
| 4:1 MUX | XC2V1000 -5 | 5.7 | ns |
| 8:1 MUX | XC2V1000 -5 | 6.5 | ns |
| 16:1 MUX | XC2V1000 -5 | 6.7 | ns |
| 32:1 MUX | XC2V1000 -5 | 8.7 | ns |
| Combinatorial (pad to LUT to pad) | XC2V1000 -5 | 5.0 | ns |
| **Memory** | | | |
| **Block RAM** | | | |
| Pad to setup | | 1.6 | ns |
| Clock to Pad | | 9.5 | ns |
| **Distributed RAM** | | | |
| Pad to setup | XC2V1000 -5 | 2.7 | ns |
| Clock to Pad | XC2V1000 -5 | 5.1 (no clk skew) | ns |

Table 12 shows internal (register-to-register) performance. Values are reported in MHz.

*Table 12:* **Register-to-Register Performance**

| Description | Device Used & Speed Grade | Register-to-Register Performance | Units |
|---|---|---|---|
| **Basic Functions** | | | |
| 16-bit Address Decoder | XC2V1000 -5 | 398 | MHz |
| 32-bit Address Decoder | XC2V1000 -5 | 291 | MHz |
| 64-bit Address Decoder | XC2V1000 -5 | 274 | MHz |
| 4:1 MUX | XC2V1000 -5 | 563 | MHz |
| 8:1 MUX | XC2V1000 -5 | 454 | MHz |
| 16:1 MUX | XC2V1000 -5 | 414 | MHz |
| 32:1 MUX | XC2V1000 -5 | 323 | MHz |
| Register to LUT to Register | XC2V1000 -5 | 613 | MHz |

## IOB Output Switching Characteristics Standard Adjustments

Table 17 gives all standard-specific adjustments for output delays terminating at pads, based on standard capacitive load, $C_{REF}$. Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

*Table 17:* **IOB Output Switching Characteristics Standard Adjustments**

| Description | IOSTANDARD Attribute | Timing Parameter | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -6 | -5 | -4 | |
| LVTTL (Low-Voltage Transistor-Transistor Logic), Slow, 2 mA | LVTTL_S2 | $T_{OLVTTL\_S2}$ | 9.42 | 9.71 | 10.68 | ns |
| LVTTL, Slow, 4 mA | LVTTL_S4 | $T_{OLVTTL\_S4}$ | 5.77 | 5.95 | 6.55 | ns |
| LVTTL, Slow, 6 mA | LVTTL_S6 | $T_{OLVTTL\_S6}$ | 4.11 | 4.24 | 4.66 | ns |
| LVTTL, Slow, 8 mA | LVTTL_S8 | $T_{OLVTTL\_S8}$ | 2.87 | 2.96 | 3.26 | ns |
| LVTTL, Slow, 12 mA | LVTTL_S12 | $T_{OLVTTL\_S12}$ | 2.32 | 2.39 | 2.63 | ns |
| LVTTL, Slow, 16 mA | LVTTL_S16 | $T_{OLVTTL\_S16}$ | 1.70 | 1.75 | 1.93 | ns |
| LVTTL, Slow, 24 mA | LVTTL_S24 | $T_{OLVTTL\_S24}$ | 1.26 | 1.30 | 1.43 | ns |
| LVTTL, Fast, 2 mA | LVTTL_F2 | $T_{OLVTTL\_F2}$ | 6.52 | 6.72 | 7.39 | ns |
| LVTTL, Fast, 4 mA | LVTTL_F4 | $T_{OLVTTL\_F4}$ | 2.80 | 2.88 | 3.17 | ns |
| LVTTL, Fast, 6 mA | LVTTL_F6 | $T_{OLVTTL\_F6}$ | 1.57 | 1.62 | 1.78 | ns |
| LVTTL, Fast, 8 mA | LVTTL_F8 | $T_{OLVTTL\_F8}$ | 0.46 | 0.48 | 0.52 | ns |
| LVTTL, Fast, 12 mA | LVTTL_F12 | $T_{OLVTTL\_F12}$ | 0.00 | 0.00 | 0.00 | ns |
| LVTTL, Fast, 16 mA | LVTTL_F16 | $T_{OLVTTL\_F16}$ | –0.13 | –0.14 | –0.15 | ns |
| LVTTL, Fast, 24 mA | LVTTL_F24 | $T_{OLVTTL\_F24}$ | –0.22 | –0.23 | –0.26 | ns |
| LVCMOS (Low-Voltage CMOS), 3.3V, Slow, 2 mA | LVCMOS33_S2 | $T_{OLVCMOS33\_S2}$ | 7.67 | 7.91 | 8.70 | ns |
| LVCMOS, 3.3V, Slow, 4 mA | LVCMOS33_S4 | $T_{OLVCMOS33\_S4}$ | 4.37 | 4.50 | 4.95 | ns |
| LVCMOS, 3.3V, Slow, 6 mA | LVCMOS33_S6 | $T_{OLVCMOS33\_S6}$ | 3.34 | 3.44 | 3.78 | ns |
| LVCMOS, 3.3V, Slow, 8 mA | LVCMOS33_S8 | $T_{OLVCMOS33\_S8}$ | 2.29 | 2.36 | 2.60 | ns |
| LVCMOS, 3.3V, Slow, 12 mA | LVCMOS33_S12 | $T_{OLVCMOS33\_S12}$ | 1.91 | 1.97 | 2.16 | ns |
| LVCMOS, 3.3V, Slow, 16 mA | LVCMOS33_S16 | $T_{OLVCMOS33\_S16}$ | 1.24 | 1.27 | 1.40 | ns |
| LVCMOS, 3.3V, Slow, 24 mA | LVCMOS33_S24 | $T_{OLVCMOS33\_S24}$ | 1.18 | 1.22 | 1.34 | ns |
| LVCMOS, 3.3V, Fast, 2 mA | LVCMOS33_F2 | $T_{OLVCMOS33\_F2}$ | 5.82 | 6.00 | 6.60 | ns |
| LVCMOS, 3.3V, Fast, 4 mA | LVCMOS33_F4 | $T_{OLVCMOS33\_F4}$ | 2.48 | 2.55 | 2.81 | ns |
| LVCMOS, 3.3V, Fast, 6 mA | LVCMOS33_F6 | $T_{OLVCMOS33\_F6}$ | 1.28 | 1.31 | 1.45 | ns |
| LVCMOS, 3.3V, Fast, 8 mA | LVCMOS33_F8 | $T_{OLVCMOS33\_F8}$ | 0.48 | 0.49 | 0.54 | ns |
| LVCMOS, 3.3V, Fast, 12 mA | LVCMOS33_F12 | $T_{OLVCMOS33\_F12}$ | 0.27 | 0.28 | 0.31 | ns |
| LVCMOS, 3.3V, Fast, 16 mA | LVCMOS33_F16 | $T_{OLVCMOS33\_F16}$ | –0.14 | –0.14 | –0.15 | ns |
| LVCMOS, 3.3V, Fast, 24 mA | LVCMOS33_F24 | $T_{OLVCMOS33\_F24}$ | –0.21 | –0.21 | –0.23 | ns |
| LVCMOS, 2.5V, Slow, 2 mA | LVCMOS25_S2 | $T_{OLVCMOS25\_S2}$ | 9.11 | 9.39 | 10.33 | ns |
| LVCMOS, 2.5V, Slow, 4 mA | LVCMOS25_S4 | $T_{OLVCMOS25\_S4}$ | 5.00 | 5.16 | 5.67 | ns |
| LVCMOS, 2.5V, Slow, 6 mA | LVCMOS25_S6 | $T_{OLVCMOS25\_S6}$ | 4.53 | 4.67 | 5.13 | ns |
| LVCMOS, 2.5V, Slow, 8 mA | LVCMOS25_S8 | $T_{OLVCMOS25\_S8}$ | 3.86 | 3.98 | 4.38 | ns |
| LVCMOS, 2.5V, Slow, 12 mA | LVCMOS25_S12 | $T_{OLVCMOS25\_S12}$ | 2.84 | 2.93 | 3.22 | ns |
| LVCMOS, 2.5V, Slow, 16 mA | LVCMOS25_S16 | $T_{OLVCMOS25\_S16}$ | 2.36 | 2.43 | 2.67 | ns |
| LVCMOS, 2.5V, Slow, 24 mA | LVCMOS25_S24 | $T_{OLVCMOS25\_S24}$ | 2.00 | 2.06 | 2.27 | ns |
| LVCMOS, 2.5V, Fast, 2 mA | LVCMOS25_F2 | $T_{OLVCMOS25\_F2}$ | 4.06 | 4.18 | 4.60 | ns |
| LVCMOS, 2.5V, Fast, 4 mA | LVCMOS25_F4 | $T_{OLVCMOS25\_F4}$ | 1.15 | 1.18 | 1.30 | ns |
| LVCMOS, 2.5V, Fast, 6 mA | LVCMOS25_F6 | $T_{OLVCMOS25\_F6}$ | 0.72 | 0.74 | 0.81 | ns |
| LVCMOS, 2.5V, Fast, 8 mA | LVCMOS25_F8 | $T_{OLVCMOS25\_F8}$ | 0.33 | 0.34 | 0.37 | ns |
| LVCMOS, 2.5V, Fast, 12 mA | LVCMOS25_F12 | $T_{OLVCMOS25\_F12}$ | 0.02 | 0.02 | 0.03 | ns |

*Table 17:* **IOB Output Switching Characteristics Standard Adjustments *(Continued)***

| Description | IOSTANDARD Attribute | Timing Parameter | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -6 | -5 | -4 | |
| LVCMOS, 2.5V, Fast, 16 mA | LVCMOS25_F16 | $T_{OLVCMOS25\_F16}$ | –0.18 | –0.19 | –0.21 | ns |
| LVCMOS, 2.5V, Fast, 24 mA | LVCMOS25_F24 | $T_{OLVCMOS25\_F24}$ | –0.35 | –0.36 | –0.40 | ns |
| LVCMOS, 1.8V, Slow, 2 mA | LVCMOS18_S2 | $T_{OLVCMOS18\_S2}$ | 15.62 | 16.10 | 17.71 | ns |
| LVCMOS, 1.8V, Slow, 4 mA | LVCMOS18_S4 | $T_{OLVCMOS18\_S4}$ | 10.20 | 10.51 | 11.57 | ns |
| LVCMOS, 1.8V, Slow, 6 mA | LVCMOS18_S6 | $T_{OLVCMOS18\_S6}$ | 7.52 | 7.75 | 8.53 | ns |
| LVCMOS, 1.8V, Slow, 8 mA | LVCMOS18_S8 | $T_{OLVCMOS18\_S8}$ | 6.87 | 7.08 | 7.78 | ns |
| LVCMOS, 1.8V, Slow, 12 mA | LVCMOS18_S12 | $T_{OLVCMOS18\_S12}$ | 5.54 | 5.71 | 6.28 | ns |
| LVCMOS, 1.8V, Slow, 16 mA | LVCMOS18_S16 | $T_{OLVCMOS18\_S16}$ | 5.31 | 5.47 | 6.02 | ns |
| LVCMOS, 1.8V, Fast, 2 mA | LVCMOS18_F2 | $T_{OLVCMOS18\_F2}$ | 5.55 | 5.72 | 6.30 | ns |
| LVCMOS, 1.8V, Fast, 4 mA | LVCMOS18_F4 | $T_{OLVCMOS18\_F4}$ | 1.89 | 1.95 | 2.15 | ns |
| LVCMOS, 1.8V, Fast, 6 mA | LVCMOS18_F6 | $T_{OLVCMOS18\_F6}$ | 0.83 | 0.85 | 0.94 | ns |
| LVCMOS, 1.8V, Fast, 8 mA | LVCMOS18_F8 | $T_{OLVCMOS18\_F8}$ | 0.70 | 0.72 | 0.80 | ns |
| LVCMOS, 1.8V, Fast, 12 mA | LVCMOS18_F12 | $T_{OLVCMOS18\_F12}$ | 0.26 | 0.27 | 0.30 | ns |
| LVCMOS, 1.8V, Fast, 16 mA | LVCMOS18_F16 | $T_{OLVCMOS18\_F16}$ | 0.23 | 0.23 | 0.26 | ns |
| LVCMOS, 1.5V, Slow, 2 mA | LVCMOS15_S2 | $T_{OLVCMOS15\_S2}$ | 18.96 | 19.55 | 21.50 | ns |
| LVCMOS, 1.5V, Slow, 4 mA | LVCMOS15_S4 | $T_{OLVCMOS15\_S4}$ | 12.77 | 13.17 | 14.48 | ns |
| LVCMOS, 1.5V, Slow, 6 mA | LVCMOS15_S6 | $T_{OLVCMOS15\_S6}$ | 12.05 | 12.42 | 13.66 | ns |
| LVCMOS, 1.5V, Slow, 8 mA | LVCMOS15_S8 | $T_{OLVCMOS15\_S8}$ | 9.75 | 10.06 | 11.06 | ns |
| LVCMOS, 1.5V, Slow, 12 mA | LVCMOS15_S12 | $T_{OLVCMOS15\_S12}$ | 9.04 | 9.32 | 10.25 | ns |
| LVCMOS, 1.5V, Slow, 16 mA | LVCMOS15_S16 | $T_{OLVCMOS15\_S16}$ | 8.21 | 8.46 | 9.31 | ns |
| LVCMOS, 1.5V, Fast, 2 mA | LVCMOS15_F2 | $T_{OLVCMOS15\_F2}$ | 5.09 | 5.25 | 5.78 | ns |
| LVCMOS, 1.5V, Fast, 4 mA | LVCMOS15_F4 | $T_{OLVCMOS15\_F4}$ | 2.01 | 2.07 | 2.27 | ns |
| LVCMOS, 1.5V, Fast, 6 mA | LVCMOS15_F6 | $T_{OLVCMOS15\_F6}$ | 1.46 | 1.51 | 1.66 | ns |
| LVCMOS, 1.5V, Fast, 8 mA | LVCMOS15_F8 | $T_{OLVCMOS15\_F8}$ | 0.93 | 0.96 | 1.05 | ns |
| LVCMOS, 1.5V, Fast, 12 mA | LVCMOS15_F12 | $T_{OLVCMOS15\_F12}$ | 0.74 | 0.77 | 0.84 | ns |
| LVCMOS, 1.5V, Fast, 16 mA | LVCMOS15_F16 | $T_{OLVCMOS15\_F16}$ | 0.67 | 0.69 | 0.75 | ns |
| LVDS (Low-Voltage Differential Signaling), 2.5V | LVDS_25 | $T_{OLVDS\_25}$ | –0.31 | –0.32 | –0.36 | ns |
| LVDS, 3.3V | LVDS_33 | $T_{OLVDS\_33}$ | –0.25 | –0.26 | –0.29 | ns |
| LVDSEXT (LVDS Extended Mode), 2.5V | LVDSEXT_25 | $T_{OLVDSEXT\_25}$ | –0.18 | –0.19 | –0.21 | ns |
| LVDSEXT, 3.3V | LVDSEXT_33 | $T_{OLVDSEXT\_33}$ | –0.17 | –0.18 | –0.19 | ns |
| ULVDS (Ultra LVDS), 2.5V | ULVDS_25 | $T_{OULVDS\_25}$ | –0.20 | –0.21 | –0.23 | ns |
| BLVDS (Bus LVDS), 2.5V | BLVDS_25 | $T_{OBLVDS\_25}$ | 0.67 | 0.69 | 0.76 | ns |
| LDT (HyperTransport), 2.5V | LDT_25 | $T_{OLDT\_25}$ | –0.20 | –0.21 | –0.23 | ns |
| LVPECL (Low-Voltage Positive Electron-Coupled Logic), 3.3V | LVPECL_33 | $T_{OLVPECL\_33}$ | 0.29 | 0.30 | 0.33 | ns |
| PCI (Peripheral Component Interface), 33 MHz, 3.3V | PCI33_3 | $T_{OPCI33\_3}$ | 1.15 | 1.19 | 1.31 | ns |
| PCI, 66 MHz, 3.3V | PCI66_3 | $T_{OPCI66\_3}$ | –0.01 | –0.01 | –0.01 | ns |
| PCI-X, 133 MHz, 3.3V | PCIX | $T_{OPCIX}$ | –0.01 | –0.01 | –0.01 | ns |
| GTL (Gunning Transceiver Logic) | GTL | $T_{OGTL}$ | –0.31 | –0.32 | –0.36 | ns |
| GTL Plus | GTLP | $T_{OGTLP}$ | –0.17 | –0.18 | –0.20 | ns |
| HSTL (High-Speed Transceiver Logic), Class I | HSTL_I | $T_{OHSTL\_I}$ | 0.26 | 0.27 | 0.29 | ns |
| HSTL, Class II | HSTL_II | $T_{OHSTL\_II}$ | –0.15 | –0.16 | –0.17 | ns |
| HSTL, Class III | HSTL_III | $T_{OHSTL\_III}$ | –0.17 | –0.17 | –0.19 | ns |
| HSTL, Class IV | HSTL_IV | $T_{OHSTL\_IV}$ | –0.40 | –0.41 | –0.45 | ns |
| HSTL, Class I, 1.8V | HSTL_I_18 | $T_{OHSTL\_I\_18}$ | 0.03 | 0.03 | 0.04 | ns |

*Table 17:* **IOB Output Switching Characteristics Standard Adjustments *(Continued)***

| Description | IOSTANDARD Attribute | Timing Parameter | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -6 | -5 | -4 | |
| HSTL, Class II, 1.8V | HSTL_II_18 | $T_{OHSTL\_II\_18}$ | –0.17 | –0.18 | –0.20 | ns |
| HSTL, Class III, 1.8V | HSTL_III_18 | $T_{OHSTL\_III\_18}$ | –0.16 | –0.16 | –0.18 | ns |
| HSTL, Class IV, 1.8V | HSTL_IV_18 | $T_{OHSTL\_IV\_18}$ | –0.39 | –0.40 | –0.44 | ns |
| SSTL (Stub Series Terminated Logic), Class I, 1.8V | SSTL18_I | $T_{OSSTL18\_I}$ | 0.20 | 0.20 | 0.22 | ns |
| SSTL, Class II, 1.8V | SSTL18_II | $T_{OSSTL18\_II}$ | –0.05 | –0.05 | –0.06 | ns |
| SSTL, Class I, 2.5V | SSTL2_I | $T_{OSSTL2\_I}$ | 0.21 | 0.22 | 0.24 | ns |
| SSTL, Class II, 2.5V | SSTL2_II | $T_{OSSTL2\_II}$ | –0.15 | –0.16 | –0.18 | ns |
| SSTL, Class I, 3.3V | SSTL3_I | $T_{OSSTL3\_I}$ | 0.29 | 0.30 | 0.33 | ns |
| SSTL, Class II, 3.3V | SSTL3_II | $T_{OSSTL3\_II}$ | –0.05 | –0.05 | –0.05 | ns |
| AGP-2X/AGP (Accelerated Graphics Port) | AGP | $T_{OAGP}$ | –0.27 | –0.28 | –0.31 | ns |
| LVDCI (Low-Voltage Digitally Controlled Impedance), 3.3V | LVDCI_33 | $T_{OLVDCI\_33}$ | 0.74 | 0.77 | 0.84 | ns |
| LVDCI, 2.5V | LVDCI_25 | $T_{OLVDCI\_25}$ | 0.78 | 0.80 | 0.88 | ns |
| LVDCI, 1.8V | LVDCI_18 | $T_{OLVDCI\_18}$ | 0.84 | 0.87 | 0.95 | ns |
| LVDCI, 1.5V | LVDCI_15 | $T_{OLVDCI\_15}$ | 1.82 | 1.88 | 2.06 | ns |
| LVDCI, 3.3V, Half-Impedance | LVDCI_DV2_33 | $T_{OLVDCI\_DV2\_33}$ | 0.12 | 0.12 | 0.13 | ns |
| LVDCI, 2.5V, Half-Impedance | LVDCI_DV2_25 | $T_{OLVDCI\_DV2\_25}$ | 0.03 | 0.03 | 0.03 | ns |
| LVDCI, 1.8V, Half-Impedance | LVDCI_DV2_18 | $T_{OLVDCI\_DV2\_18}$ | 0.42 | 0.43 | 0.48 | ns |
| LVDCI, 1.5V, Half-Impedance | LVDCI_DV2_15 | $T_{OLVDCI\_DV2\_15}$ | 1.20 | 1.23 | 1.36 | ns |
| HSLVDCI (High-Speed Low-Voltage DCI), 1.5V | HSLVDCI_15 | $T_{OHSLVDCI\_15}$ | 1.82 | 1.88 | 2.06 | ns |
| HSLVDCI, 1.8V | HSLVDCI_18 | $T_{OHSLVDCI\_18}$ | 1.05 | 1.08 | 1.24 | ns |
| HSLVDCI, 2.5V | HSLVDCI_25 | $T_{OHSLVDCI\_25}$ | 0.78 | 0.80 | 0.88 | ns |
| HSLVDCI, 3.3V | HSLVDCI_33 | $T_{OHSLVDCI\_33}$ | 0.74 | 0.77 | 0.84 | ns |
| GTL (Gunning Transceiver Logic) with DCI | GTL_DCI | $T_{OGTL\_DCI}$ | –0.31 | –0.32 | –0.35 | ns |
| GTL Plus with DCI | GTLP_DCI | $T_{OGTLP\_DCI}$ | –0.15 | –0.16 | –0.17 | ns |
| HSTL (High-Speed Transceiver Logic), Class I, with DCI | HSTL_I_DCI | $T_{OHSTL\_I\_DCI}$ | 0.23 | 0.23 | 0.26 | ns |
| HSTL, Class II, with DCI | HSTL_II_DCI | $T_{OHSTL\_II\_DCI}$ | 0.06 | 0.06 | 0.07 | ns |
| HSTL, Class III, with DCI | HSTL_III_DCI | $T_{OHSTL\_III\_DCI}$ | –0.17 | –0.18 | –0.20 | ns |
| HSTL, Class IV, with DCI | HSTL_IV_DCI | $T_{OHSTL\_IV\_DCI}$ | –0.46 | –0.47 | –0.52 | ns |
| HSTL, Class I, 1.8V, with DCI | HSTL_I_DCI_18 | $T_{OHSTL\_I\_DCI\_18}$ | 0.05 | 0.05 | 0.06 | ns |
| HSTL, Class II, 1.8V, with DCI | HSTL_II_DCI_18 | $T_{OHSTL\_II\_DCI\_18}$ | –0.03 | –0.03 | –0.03 | ns |
| HSTL, Class III, 1.8V, with DCI | HSTL_III_DCI_18 | $T_{OHSTL\_III\_DCI\_18}$ | –0.14 | –0.14 | –0.16 | ns |
| HSTL, Class IV, 1.8V, with DCI | HSTL_IV_DCI_18 | $T_{OHSTL\_IV\_DCI\_18}$ | –0.41 | –0.42 | –0.47 | ns |
| SSTL (Stub Series Terminated Logic), Class I, 1.8V, with DCI | SSTL18_I_DCI | $T_{OSSTL18\_I\_DCI}$ | 0.36 | 0.37 | 0.40 | ns |
| SSTL, Class II, 1.8V, with DCI | SSTL18_II_DCI | $T_{OSSTL18\_II\_DCI}$ | 0.06 | 0.06 | 0.07 | ns |
| SSTL, Class I, 2.5V, with DCI | SSTL2_I_DCI | $T_{OSSTL2\_I\_DCI}$ | 0.12 | 0.13 | 0.14 | ns |
| SSTL, Class II, 2.5V, with DCI | SSTL2_II_DCI | $T_{OSSTL2\_II\_DCI}$ | –0.10 | –0.10 | –0.11 | ns |
| SSTL, Class I, 3.3V, with DCI | SSTL3_I_DCI | $T_{OSSTL3\_I\_DCI}$ | 0.15 | 0.16 | 0.17 | ns |
| SSTL, Class II, 3.3V, with DCI | SSTL3_II_DCI | $T_{OSSTL3\_II\_DCI}$ | 0.08 | 0.08 | 0.09 | ns |

## Output Clock Jitter

*Table 40:* **Output Clock Jitter**

| Description | Symbol | Constraints | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -6 | -5 | -4 | |
| **Clock Synthesis Period Jitter** | | | | | | |
| CLK0 | CLKOUT_PER_JITT_0 | | ±100 | ±100 | ±100 | ps |
| CLK90 | CLKOUT_PER_JITT_90 | | ±150 | ±150 | ±150 | ps |
| CLK180 | CLKOUT_PER_JITT_180 | | ±150 | ±150 | ±150 | ps |
| CLK270 | CLKOUT_PER_JITT_270 | | ±150 | ±150 | ±150 | ps |
| CLK2X, CLK2X180 | CLKOUT_PER_JITT_2X | | ±200 | ±200 | ±200 | ps |
| CLKDV (integer division) | CLKOUT_PER_JITT_DV1 | | ±150 | ±150 | ±150 | ps |
| CLKDV (non-integer division) | CLKOUT_PER_JITT_DV2 | | ±300 | ±300 | ±300 | ps |
| CLKFX, CLKFX180 | CLKOUT_PER_JITT_FX | | Note 1 | Note 1 | Note 1 | ps |

**Notes:**
1. Values for this parameter are available at www.xilinx.com.

## Output Clock Phase Alignment

*Table 41:* **Output Clock Phase Alignment**

| Description | Symbol | Constraints | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -6 | -5 | -4 | |
| **Phase Offset Between CLKIN and CLKFB** | | | | | | |
| CLKIN/CLKFB | CLKIN_CLKFB_PHASE | | ±50 | ±50 | ±50 | ps |
| **Phase Offset Between Any DCM Outputs** | | | | | | |
| All CLK outputs | CLKOUT_PHASE | | ±140 | ±140 | ±140 | ps |
| **Duty Cycle Precision** | | | | | | |
| DLL outputs(1) | CLKOUT_DUTY_CYCLE_DLL(2) | | ±150 | ±150 | ±150 | ps |
| CLKFX outputs | CLKOUT_DUTY_CYCLE_FX | | ±100 | ±100 | ±100 | ps |

**Notes:**
1. "DLL outputs" is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. CLKOUT_DUTY_CYCLE_DLL applies to the 1X clock outputs (CLK0, CLK90, CLK180, and CLK270) only if DUTY_CYCLE_CORRECTION = TRUE.
3. Specification also applies to PSCLK.

## FG256/FGG256 Fine-Pitch BGA Package

As shown in Table 6, XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000 Virtex-II devices are available in the FG256/FGG256 fine-pitch BGA package. The pins in the XC2V250, XC2V500, and XC2V1000 devices are same. The No Connect columns show pin differences for the XC2V40 and XC2V80 devices. Following this table are the FG256/FGG256 Fine-Pitch BGA Package Specifications (1.00mm pitch).

*Table 6:* **FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

| Bank | Pin Description | Pin Number | No Connect in XC2V40 | No Connect in XC2V80 |
|---|---|---|---|---|
| 0 | IO_L01N_0 | C4 | | |
| 0 | IO_L01P_0 | B4 | | |
| 0 | IO_L02N_0 | D5 | | |
| 0 | IO_L02P_0 | C5 | | |
| 0 | IO_L03N_0/VRP_0 | B5 | | |
| 0 | IO_L03P_0/VRN_0 | A5 | | |
| 0 | IO_L04N_0/VREF_0 | D6 | NC | NC |
| 0 | IO_L04P_0 | C6 | NC | NC |
| 0 | IO_L05N_0 | B6 | NC | NC |
| 0 | IO_L05P_0 | A6 | NC | NC |
| 0 | IO_L92N_0 | E6 | NC | NC |
| 0 | IO_L92P_0 | E7 | NC | NC |
| 0 | IO_L93N_0 | D7 | NC | NC |
| 0 | IO_L93P_0 | C7 | NC | NC |
| 0 | IO_L94N_0/VREF_0 | B7 | | |
| 0 | IO_L94P_0 | A7 | | |
| 0 | IO_L95N_0/GCLK7P | D8 | | |
| 0 | IO_L95P_0/GCLK6S | C8 | | |
| 0 | IO_L96N_0/GCLK5P | B8 | | |
| 0 | IO_L96P_0/GCLK4S | A8 | | |
| | | | | |
| 1 | IO_L96N_1/GCLK3P | A9 | | |
| 1 | IO_L96P_1/GCLK2S | B9 | | |
| 1 | IO_L95N_1/GCLK1P | C9 | | |
| 1 | IO_L95P_1/GCLK0S | D9 | | |
| 1 | IO_L94N_1 | A10 | | |
| 1 | IO_L94P_1/VREF_1 | B10 | | |
| 1 | IO_L93N_1 | C10 | NC | NC |
| 1 | IO_L93P_1 | D10 | NC | NC |
| 1 | IO_L92N_1 | E10 | NC | NC |

*Table 7:* **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

| Bank | Pin Description | Pin Number | No Connect in XC2V250 | No Connect in XC2V500 |
|---|---|---|---|---|
| 2 | IO_L45N_2 | H19 | | |
| 2 | IO_L45P_2/VREF_2 | H20 | | |
| 2 | IO_L46N_2 | H21 | | |
| 2 | IO_L46P_2 | H22 | | |
| 2 | IO_L48N_2 | J17 | | |
| 2 | IO_L48P_2 | J18 | | |
| 2 | IO_L49N_2 | J19 | NC | |
| 2 | IO_L49P_2 | J20 | NC | |
| 2 | IO_L51N_2 | J21 | NC | |
| 2 | IO_L51P_2/VREF_2 | J22 | NC | |
| 2 | IO_L52N_2 | K17 | NC | |
| 2 | IO_L52P_2 | K18 | NC | |
| 2 | IO_L54N_2 | K19 | NC | |
| 2 | IO_L54P_2 | K20 | NC | |
| 2 | IO_L91N_2 | K21 | | |
| 2 | IO_L91P_2 | K22 | | |
| 2 | IO_L93N_2 | L17 | | |
| 2 | IO_L93P_2/VREF_2 | L18 | | |
| 2 | IO_L94N_2 | L19 | | |
| 2 | IO_L94P_2 | L20 | | |
| 2 | IO_L96N_2 | L21 | | |
| 2 | IO_L96P_2 | L22 | | |
| | | | | |
| 3 | IO_L96N_3 | M21 | | |
| 3 | IO_L96P_3 | M20 | | |
| 3 | IO_L94N_3 | M19 | | |
| 3 | IO_L94P_3 | M18 | | |
| 3 | IO_L93N_3/VREF_3 | M17 | | |
| 3 | IO_L93P_3 | N17 | | |
| 3 | IO_L91N_3 | N22 | | |
| 3 | IO_L91P_3 | N21 | | |
| 3 | IO_L54N_3 | N20 | NC | |
| 3 | IO_L54P_3 | N19 | NC | |
| 3 | IO_L52N_3 | N18 | NC | |

*Table 8:* **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

| Bank | Pin Description | Pin Number | No Connect in XC2V1500 | No Connect in XC2V2000 |
|---|---|---|---|---|
| 7 | IO_L78N_7 | M2 | NC | |
| 7 | IO_L76P_7 | M5 | NC | |
| 7 | IO_L76N_7 | M6 | NC | |
| 7 | IO_L75P_7/VREF_7 | M3 | NC | |
| 7 | IO_L75N_7 | M4 | NC | |
| 7 | IO_L73P_7 | M7 | NC | |
| 7 | IO_L73N_7 | M8 | NC | |
| 7 | IO_L72P_7 | L1 | | |
| 7 | IO_L72N_7 | L2 | | |
| 7 | IO_L70P_7 | L5 | | |
| 7 | IO_L70N_7 | L6 | | |
| 7 | IO_L69P_7/VREF_7 | L3 | | |
| 7 | IO_L69N_7 | L4 | | |
| 7 | IO_L67P_7 | K1 | | |
| 7 | IO_L67N_7 | J1 | | |
| 7 | IO_L54P_7 | K3 | | |
| 7 | IO_L54N_7 | K4 | | |
| 7 | IO_L52P_7 | K5 | | |
| 7 | IO_L52N_7 | K6 | | |
| 7 | IO_L51P_7/VREF_7 | L8 | | |
| 7 | IO_L51N_7 | L7 | | |
| 7 | IO_L49P_7 | J2 | | |
| 7 | IO_L49N_7 | H1 | | |
| 7 | IO_L48P_7 | J3 | | |
| 7 | IO_L48N_7 | J4 | | |
| 7 | IO_L46P_7 | J5 | | |
| 7 | IO_L46N_7 | J6 | | |
| 7 | IO_L45P_7/VREF_7 | H5 | | |
| 7 | IO_L45N_7 | H4 | | |
| 7 | IO_L43P_7 | K7 | | |
| 7 | IO_L43N_7 | J7 | | |
| 7 | IO_L25P_7 | H2 | NC | NC |
| 7 | IO_L25N_7 | H3 | NC | NC |
| 7 | IO_L24P_7 | G1 | | |
| 7 | IO_L24N_7 | F1 | | |
| 7 | IO_L22P_7 | G3 | | |
| 7 | IO_L22N_7 | G4 | | |

*Table 10:* **BG728 BGA — XC2V3000**

| Bank | Pin Description | Pin Number |
|---|---|---|
| 7 | IO_L27P_7/VREF_7 | H5 |
| 7 | IO_L27N_7 | H6 |
| 7 | IO_L25P_7 | J7 |
| 7 | IO_L25N_7 | J8 |
| 7 | IO_L24P_7 | G1 |
| 7 | IO_L24N_7 | F1 |
| 7 | IO_L22P_7 | G2 |
| 7 | IO_L22N_7 | G3 |
| 7 | IO_L21P_7/VREF_7 | F2 |
| 7 | IO_L21N_7 | F3 |
| 7 | IO_L19P_7 | G5 |
| 7 | IO_L19N_7 | G6 |
| 7 | IO_L06P_7 | F4 |
| 7 | IO_L06N_7 | F5 |
| 7 | IO_L04P_7 | E1 |
| 7 | IO_L04N_7 | E2 |
| 7 | IO_L03P_7/VREF_7 | D1 |
| 7 | IO_L03N_7 | C1 |
| 7 | IO_L02P_7/VRN_7 | E3 |
| 7 | IO_L02N_7/VRP_7 | E4 |
| 7 | IO_L01P_7 | D2 |
| 7 | IO_L01N_7 | D3 |
| | | |
| 0 | VCCO_0 | K13 |
| 0 | VCCO_0 | K12 |
| 0 | VCCO_0 | K11 |
| 0 | VCCO_0 | J11 |
| 0 | VCCO_0 | J10 |
| 0 | VCCO_0 | G12 |
| 0 | VCCO_0 | D7 |
| 0 | VCCO_0 | C12 |
| 1 | VCCO_1 | K17 |
| 1 | VCCO_1 | K16 |
| 1 | VCCO_1 | K15 |
| 1 | VCCO_1 | J18 |
| 1 | VCCO_1 | J17 |

*Table 10:* **BG728 BGA — XC2V3000**

| Bank | Pin Description | Pin Number |
|---|---|---|
| NA | GND | F22 |
| NA | GND | F6 |
| NA | GND | E23 |
| NA | GND | E17 |
| NA | GND | E11 |
| NA | GND | E5 |
| NA | GND | D24 |
| NA | GND | D14 |
| NA | GND | D4 |
| NA | GND | C25 |
| NA | GND | C3 |
| NA | GND | B27 |
| NA | GND | B26 |
| NA | GND | B20 |
| NA | GND | B8 |
| NA | GND | B2 |
| NA | GND | B1 |
| NA | GND | A27 |
| NA | GND | A26 |
| NA | GND | A14 |
| NA | GND | A2 |

**Notes:**
1. See Table 4 for an explanation of the signals available on this pin.

*Table 12:* **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

| Bank | Pin Description | Pin Number | No Connect in the XC2V3000 |
|---|---|---|---|
| 2 | IO_L81N_2 | R7 | NC |
| 2 | IO_L81P_2/VREF_2 | R6 | NC |
| 2 | IO_L82N_2 | U5 | NC |
| 2 | IO_L82P_2 | T5 | NC |
| 2 | IO_L83N_2 | T10 | NC |
| 2 | IO_L83P_2 | U10 | NC |
| 2 | IO_L84N_2 | U4 | NC |
| 2 | IO_L84P_2 | T4 | NC |
| 2 | IO_L91N_2 | T2 | |
| 2 | IO_L91P_2 | R1 | |
| 2 | IO_L92N_2 | U7 | |
| 2 | IO_L92P_2 | T7 | |
| 2 | IO_L93N_2 | T6 | |
| 2 | IO_L93P_2/VREF_2 | U6 | |
| 2 | IO_L94N_2 | U1 | |
| 2 | IO_L94P_2 | U2 | |
| 2 | IO_L95N_2 | U9 | |
| 2 | IO_L95P_2 | U8 | |
| 2 | IO_L96N_2 | U3 | |
| 2 | IO_L96P_2 | V4 | |
| | | | |
| 3 | IO_L96N_3 | V6 | |
| 3 | IO_L96P_3 | W6 | |
| 3 | IO_L95N_3 | V5 | |
| 3 | IO_L95P_3 | W5 | |
| 3 | IO_L94N_3 | V7 | |
| 3 | IO_L94P_3 | W7 | |
| 3 | IO_L93N_3/VREF_3 | V10 | |
| 3 | IO_L93P_3 | W10 | |
| 3 | IO_L92N_3 | V1 | |
| 3 | IO_L92P_3 | V2 | |
| 3 | IO_L91N_3 | W3 | |
| 3 | IO_L91P_3 | Y3 | |
| 3 | IO_L84N_3 | V9 | NC |
| 3 | IO_L84P_3 | V8 | NC |
| 3 | IO_L83N_3 | W4 | NC |

*Table 12:* **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

| Bank | Pin Description | Pin Number | No Connect in the XC2V3000 |
|---|---|---|---|
| 3 | IO_L53P_3 | AD2 | |
| 3 | IO_L52N_3 | AC8 | |
| 3 | IO_L52P_3 | AB8 | |
| 3 | IO_L51N_3/VREF_3 | AB10 | |
| 3 | IO_L51P_3 | AC10 | |
| 3 | IO_L50N_3 | AD5 | |
| 3 | IO_L50P_3 | AE5 | |
| 3 | IO_L49N_3 | AE4 | |
| 3 | IO_L49P_3 | AF4 | |
| 3 | IO_L48N_3 | AB9 | |
| 3 | IO_L48P_3 | AC9 | |
| 3 | IO_L47N_3 | AE2 | |
| 3 | IO_L47P_3 | AF1 | |
| 3 | IO_L46N_3 | AD6 | |
| 3 | IO_L46P_3 | AE6 | |
| 3 | IO_L45N_3/VREF_3 | AD9 | |
| 3 | IO_L45P_3 | AE9 | |
| 3 | IO_L44N_3 | AF2 | |
| 3 | IO_L44P_3 | AG2 | |
| 3 | IO_L43N_3 | AF3 | |
| 3 | IO_L43P_3 | AG3 | |
| 3 | IO_L30N_3 | AD7 | |
| 3 | IO_L30P_3 | AE7 | |
| 3 | IO_L29N_3 | AF5 | |
| 3 | IO_L29P_3 | AG5 | |
| 3 | IO_L28N_3 | AE8 | |
| 3 | IO_L28P_3 | AD8 | |
| 3 | IO_L27N_3/VREF_3 | AF8 | |
| 3 | IO_L27P_3 | AF9 | |
| 3 | IO_L26N_3 | AH1 | |
| 3 | IO_L26P_3 | AJ1 | |
| 3 | IO_L25N_3 | AG4 | |
| 3 | IO_L25P_3 | AH5 | |
| 3 | IO_L24N_3 | AF6 | |
| 3 | IO_L24P_3 | AG6 | |
| 3 | IO_L23N_3 | AH3 | |

*Table 12:* **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

| Bank | Pin Description | Pin Number | No Connect in the XC2V3000 |
|---|---|---|---|
| 7 | IO_L03N_7 | F30 | |
| 7 | IO_L02P_7/VRN_7 | K25 | |
| 7 | IO_L02N_7/VRP_7 | J25 | |
| 7 | IO_L01P_7 | D33 | |
| 7 | IO_L01N_7 | E33 | |
| | | | |
| 0 | VCCO_0 | M22 | |
| 0 | VCCO_0 | M21 | |
| 0 | VCCO_0 | M20 | |
| 0 | VCCO_0 | M19 | |
| 0 | VCCO_0 | M18 | |
| 0 | VCCO_0 | L23 | |
| 0 | VCCO_0 | L22 | |
| 0 | VCCO_0 | L21 | |
| 0 | VCCO_0 | L20 | |
| 0 | VCCO_0 | E20 | |
| 0 | VCCO_0 | D28 | |
| 0 | VCCO_0 | A25 | |
| 0 | VCCO_0 | A19 | |
| 1 | VCCO_1 | M17 | |
| 1 | VCCO_1 | M16 | |
| 1 | VCCO_1 | M15 | |
| 1 | VCCO_1 | M14 | |
| 1 | VCCO_1 | M13 | |
| 1 | VCCO_1 | L15 | |
| 1 | VCCO_1 | L14 | |
| 1 | VCCO_1 | L13 | |
| 1 | VCCO_1 | L12 | |
| 1 | VCCO_1 | E15 | |
| 1 | VCCO_1 | D7 | |
| 1 | VCCO_1 | A16 | |
| 1 | VCCO_1 | A10 | |
| 2 | VCCO_2 | U12 | |
| 2 | VCCO_2 | T12 | |
| 2 | VCCO_2 | T1 | |
| 2 | VCCO_2 | R12 | |

*Table 13:* **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

| Bank | Pin Description | Pin Number | No Connect in the XC2V4000 | No Connect in the XC2V6000 |
|---|---|---|---|---|
| 0 | IO_L76P_0 | C24 | | |
| 0 | IO_L77N_0 | K22 | | |
| 0 | IO_L77P_0 | K21 | | |
| 0 | IO_L78N_0 | E22 | | |
| 0 | IO_L78P_0 | E23 | | |
| 0 | IO_L79N_0 | B23 | | |
| 0 | IO_L79P_0 | B24 | | |
| 0 | IO_L80N_0 | J22 | | |
| 0 | IO_L80P_0 | J21 | | |
| 0 | IO_L81N_0 | G21 | | |
| 0 | IO_L81P_0/VREF_0 | G22 | | |
| 0 | IO_L82N_0 | A23 | | |
| 0 | IO_L82P_0 | A24 | | |
| 0 | IO_L83N_0 | H22 | | |
| 0 | IO_L83P_0 | H21 | | |
| 0 | IO_L84N_0 | F21 | | |
| 0 | IO_L84P_0 | F22 | | |
| 0 | IO_L91N_0/VREF_0 | B21 | | |
| 0 | IO_L91P_0 | B22 | | |
| 0 | IO_L92N_0 | L20 | | |
| 0 | IO_L92P_0 | M20 | | |
| 0 | IO_L93N_0 | E21 | | |
| 0 | IO_L93P_0 | D22 | | |
| 0 | IO_L94N_0/VREF_0 | A21 | | |
| 0 | IO_L94P_0 | A22 | | |
| 0 | IO_L95N_0/GCLK7P | H20 | | |
| 0 | IO_L95P_0/GCLK6S | J20 | | |
| 0 | IO_L96N_0/GCLK5P | C21 | | |
| 0 | IO_L96P_0/GCLK4S | D21 | | |
| | | | | |
| 1 | IO_L96N_1/GCLK3P | F19 | | |
| 1 | IO_L96P_1/GCLK2S | F20 | | |
| 1 | IO_L95N_1/GCLK1P | H19 | | |
| 1 | IO_L95P_1/GCLK0S | H18 | | |
| 1 | IO_L94N_1 | C19 | | |
| 1 | IO_L94P_1/VREF_1 | C20 | | |

*Table 13:* **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

| Bank | Pin Description | Pin Number | No Connect in the XC2V4000 | No Connect in the XC2V6000 |
|---|---|---|---|---|
| 1 | IO_L33N_1/VREF_1 | D11 | NC | |
| 1 | IO_L33P_1 | D12 | NC | |
| 1 | IO_L32N_1 | H14 | NC | |
| 1 | IO_L32P_1 | H13 | NC | |
| 1 | IO_L31N_1 | A8 | NC | |
| 1 | IO_L31P_1 | A9 | NC | |
| 1 | IO_L30N_1 | F11 | | |
| 1 | IO_L30P_1 | F12 | | |
| 1 | IO_L29N_1 | K14 | | |
| 1 | IO_L29P_1 | L14 | | |
| 1 | IO_L28N_1 | C9 | | |
| 1 | IO_L28P_1 | C10 | | |
| 1 | IO_L27N_1/VREF_1 | G11 | | |
| 1 | IO_L27P_1 | G12 | | |
| 1 | IO_L26N_1 | M15 | | |
| 1 | IO_L26P_1 | M14 | | |
| 1 | IO_L25N_1 | B7 | | |
| 1 | IO_L25P_1 | B8 | | |
| 1 | IO_L24N_1 | D9 | | |
| 1 | IO_L24P_1 | D10 | | |
| 1 | IO_L23N_1 | J13 | | |
| 1 | IO_L23P_1 | J12 | | |
| 1 | IO_L22N_1 | A6 | | |
| 1 | IO_L22P_1 | A7 | | |
| 1 | IO_L21N_1/VREF_1 | E9 | | |
| 1 | IO_L21P_1 | E10 | | |
| 1 | IO_L20N_1 | D8 | | |
| 1 | IO_L20P_1 | E7 | | |
| 1 | IO_L19N_1 | C7 | | |
| 1 | IO_L19P_1 | C8 | | |
| 1 | IO_L12N_1 | F9 | NC | |
| 1 | IO_L12P_1 | F10 | NC | |
| 1 | IO_L11N_1 | H12 | NC | |
| 1 | IO_L11P_1 | H11 | NC | |
| 1 | IO_L10N_1 | B5 | NC | |
| 1 | IO_L10P_1 | B6 | NC | |

*Table 13:* **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

| Bank | Pin Description | Pin Number | No Connect in the XC2V4000 | No Connect in the XC2V6000 |
|---|---|---|---|---|
| 6 | IO_L71N_6 | AE39 | | |
| 6 | IO_L72P_6 | AD36 | | |
| 6 | IO_L72N_6 | AE36 | | |
| 6 | IO_L73P_6 | AB29 | | |
| 6 | IO_L73N_6 | AA29 | | |
| 6 | IO_L74P_6 | AE38 | | |
| 6 | IO_L74N_6 | AD38 | | |
| 6 | IO_L75P_6 | AC33 | | |
| 6 | IO_L75N_6/VREF_6 | AD33 | | |
| 6 | IO_L76P_6 | AB30 | | |
| 6 | IO_L76N_6 | AA30 | | |
| 6 | IO_L77P_6 | AD37 | | |
| 6 | IO_L77N_6 | AC37 | | |
| 6 | IO_L78P_6 | AB34 | | |
| 6 | IO_L78N_6 | AC34 | | |
| 6 | IO_L79P_6 | AB31 | | |
| 6 | IO_L79N_6 | AA31 | | |
| 6 | IO_L80P_6 | AD39 | | |
| 6 | IO_L80N_6 | AC39 | | |
| 6 | IO_L81P_6 | AB35 | | |
| 6 | IO_L81N_6/VREF_6 | AC35 | | |
| 6 | IO_L82P_6 | AB32 | | |
| 6 | IO_L82N_6 | AA32 | | |
| 6 | IO_L83P_6 | AC38 | | |
| 6 | IO_L83N_6 | AB38 | | |
| 6 | IO_L84P_6 | AA33 | | |
| 6 | IO_L84N_6 | AB33 | | |
| 6 | IO_L91P_6 | Y28 | | |
| 6 | IO_L91N_6 | Y29 | | |
| 6 | IO_L92P_6 | AB39 | | |
| 6 | IO_L92N_6 | AA39 | | |
| 6 | IO_L93P_6 | AA36 | | |
| 6 | IO_L93N_6/VREF_6 | AB36 | | |
| 6 | IO_L94P_6 | Y31 | | |
| 6 | IO_L94N_6 | Y32 | | |
| 6 | IO_L95P_6 | AA37 | | |

*Table 13:* **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

| Bank | Pin Description | Pin Number | No Connect in the XC2V4000 | No Connect in the XC2V6000 |
|---|---|---|---|---|
| 7 | IO_L26P_7 | M31 | | |
| 7 | IO_L26N_7 | L31 | | |
| 7 | IO_L25P_7 | G38 | | |
| 7 | IO_L25N_7 | H38 | | |
| 7 | IO_L24P_7 | J34 | | |
| 7 | IO_L24N_7 | K34 | | |
| 7 | IO_L23P_7 | K32 | | |
| 7 | IO_L23N_7 | K31 | | |
| 7 | IO_L22P_7 | F39 | | |
| 7 | IO_L22N_7 | G39 | | |
| 7 | IO_L21P_7/VREF_7 | G36 | | |
| 7 | IO_L21N_7 | H36 | | |
| 7 | IO_L20P_7 | N28 | | |
| 7 | IO_L20N_7 | M28 | | |
| 7 | IO_L19P_7 | G37 | | |
| 7 | IO_L19N_7 | H37 | | |
| 7 | IO_L12P_7 | J33 | NC | |
| 7 | IO_L12N_7 | K33 | NC | |
| 7 | IO_L11P_7 | M29 | NC | |
| 7 | IO_L11N_7 | L28 | NC | |
| 7 | IO_L10P_7 | E38 | NC | |
| 7 | IO_L10N_7 | F38 | NC | |
| 7 | IO_L09P_7/VREF_7 | G35 | NC | |
| 7 | IO_L09N_7 | H35 | NC | |
| 7 | IO_L08P_7 | L30 | NC | |
| 7 | IO_L08N_7 | K29 | NC | |
| 7 | IO_L07P_7 | D39 | NC | |
| 7 | IO_L07N_7 | E39 | NC | |
| 7 | IO_L06P_7 | G34 | | |
| 7 | IO_L06N_7 | H34 | | |
| 7 | IO_L05P_7 | J32 | | |
| 7 | IO_L05N_7 | H33 | | |
| 7 | IO_L04P_7 | F36 | | |
| 7 | IO_L04N_7 | F37 | | |
| 7 | IO_L03P_7/VREF_7 | E36 | | |
| 7 | IO_L03N_7 | F35 | | |

*Table 13:* **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

| Bank | Pin Description | Pin Number | No Connect in the XC2V4000 | No Connect in the XC2V6000 |
|---|---|---|---|---|
| 7 | IO_L02P_7/VRN_7 | M27 | | |
| 7 | IO_L02N_7/VRP_7 | L27 | | |
| 7 | IO_L01P_7 | D38 | | |
| 7 | IO_L01N_7 | E37 | | |
| | | | | |
| 0 | VCCO_0 | P25 | | |
| 0 | VCCO_0 | P24 | | |
| 0 | VCCO_0 | P23 | | |
| 0 | VCCO_0 | P22 | | |
| 0 | VCCO_0 | P21 | | |
| 0 | VCCO_0 | N26 | | |
| 0 | VCCO_0 | N25 | | |
| 0 | VCCO_0 | N24 | | |
| 0 | VCCO_0 | N23 | | |
| 0 | VCCO_0 | N22 | | |
| 0 | VCCO_0 | N21 | | |
| 0 | VCCO_0 | L23 | | |
| 0 | VCCO_0 | J25 | | |
| 0 | VCCO_0 | G27 | | |
| 0 | VCCO_0 | E29 | | |
| 0 | VCCO_0 | C22 | | |
| 0 | VCCO_0 | B26 | | |
| 1 | VCCO_1 | P19 | | |
| 1 | VCCO_1 | P18 | | |
| 1 | VCCO_1 | P17 | | |
| 1 | VCCO_1 | P16 | | |
| 1 | VCCO_1 | P15 | | |
| 1 | VCCO_1 | N19 | | |
| 1 | VCCO_1 | N18 | | |
| 1 | VCCO_1 | N17 | | |
| 1 | VCCO_1 | N16 | | |
| 1 | VCCO_1 | N15 | | |
| 1 | VCCO_1 | N14 | | |
| 1 | VCCO_1 | L17 | | |
| 1 | VCCO_1 | J15 | | |
| 1 | VCCO_1 | G13 | | |

*Table 13:* **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

| Bank | Pin Description | Pin Number | No Connect in the XC2V4000 | No Connect in the XC2V6000 |
|---|---|---|---|---|
| NA | GND | D4 | | |
| NA | GND | C39 | | |
| NA | GND | C38 | | |
| NA | GND | C37 | | |
| NA | GND | C3 | | |
| NA | GND | C2 | | |
| NA | GND | C1 | | |
| NA | GND | B39 | | |
| NA | GND | B38 | | |
| NA | GND | B37 | | |
| NA | GND | B29 | | |
| NA | GND | B11 | | |
| NA | GND | B3 | | |
| NA | GND | B2 | | |
| NA | GND | B1 | | |
| NA | GND | A38 | | |
| NA | GND | A37 | | |
| NA | GND | A20 | | |
| NA | GND | A3 | | |
| NA | GND | A2 | | |

**Notes:**
1. See Table 4 for an explanation of the signals available on this pin.