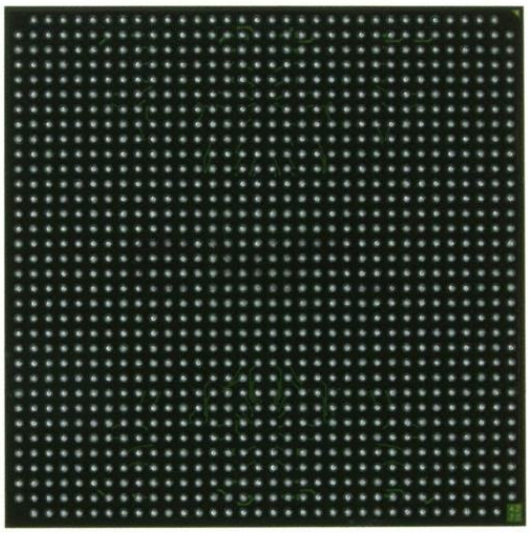

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	11648
Number of Logic Elements/Cells	-
Total RAM Bits	3096576
Number of I/O	824
Number of Gates	8000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v8000-5ff1152i

Virtex-II Platform FPGAs: Introduction and Overview

DS031-1 (v3.5) November 5, 2007 **Product Specification**

Summary of Virtex-II™ Features

- Industry First Platform FPGA Solution
- IP-Immersion Architecture
  - Densities from 40K to 8M system gates
  - 420 MHz internal clock speed (Advance Data)
  - 840+ Mb/s I/O (Advance Data)
- SelectRAM™ Memory Hierarchy
  - 3 Mb of dual-port RAM in 18 Kbit block SelectRAM resources
  - Up to 1.5 Mb of distributed SelectRAM resources
- High-Performance Interfaces to External Memory
  - DRAM interfaces
    - SDR / DDR SDRAM
    - Network FCRAM
    - Reduced Latency DRAM
  - SRAM interfaces
    - SDR / DDR SRAM
    - QDR™ SRAM
  - CAM interfaces
- Arithmetic Functions
  - Dedicated 18-bit x 18-bit multiplier blocks
  - Fast look-ahead carry logic chains
- Flexible Logic Resources
  - Up to 93,184 internal registers / latches with Clock Enable
  - Up to 93,184 look-up tables (LUTs) or cascadable 16-bit shift registers
  - Wide multiplexers and wide-input function support
  - Horizontal cascade chain and sum-of-products support
  - Internal 3-state bussing
- High-Performance Clock Management Circuitry
  - Up to 12 DCM (Digital Clock Manager) modules
    - Precise clock de-skew
    - Flexible frequency synthesis
    - High-resolution phase shifting
  - 16 global clock multiplexer buffers
- Active Interconnect Technology
  - Fourth generation segmented routing structure
  - Predictable, fast routing delay, independent of fanout
- SelectIO™-Ultra Technology
  - Up to 1,108 user I/Os
  - 19 single-ended and six differential standards
  - Programmable sink current (2 mA to 24 mA) per I/O
  - Digitally Controlled Impedance (DCI) I/O: on-chip termination resistors for single-ended I/O standards
  - PCI-X compatible (133 MHz and 66 MHz) at 3.3V
  - PCI compliant (66 MHz and 33 MHz) at 3.3V
  - CardBus compliant (33 MHz) at 3.3V
  - Differential Signaling
    - 840 Mb/s Low-Voltage Differential Signaling I/O (LVDS) with current mode drivers
    - Bus LVDS I/O
    - Lightning Data Transport (LDT) I/O with current driver buffers
    - Low-Voltage Positive Emitter-Coupled Logic (LVPECL) I/O
    - Built-in DDR input and output registers
  - Proprietary high-performance SelectLink Technology
    - High-bandwidth data path
    - Double Data Rate (DDR) link
    - Web-based HDL generation methodology
- Supported by Xilinx Foundation™ and Alliance Series™ Development Systems
  - Integrated VHDL and Verilog design flows
  - Compilation of 10M system gates designs
  - Internet Team Design (ITD) tool
- SRAM-Based In-System Configuration
  - Fast SelectMAP configuration
  - Triple Data Encryption Standard (DES) security option (Bitstream Encryption)
  - IEEE 1532 support
  - Partial reconfiguration
  - Unlimited reprogrammability
  - Readback capability
- 0.15 µm 8-Layer Metal Process with 0.12 µm High-Speed Transistors
- 1.5V (V_{CCINT}) Core Power Supply, Dedicated 3.3V V_{CCAUX} Auxiliary and V_{CCO} I/O Power Supplies
- IEEE 1149.1 Compatible Boundary-Scan Logic Support
- Flip-Chip and Wire-Bond Ball Grid Array (BGA) Packages in Three Standard Fine Pitches (0.80 mm, 1.00 mm, and 1.27 mm)
- Wire-Bond BGA Devices Available in Pb-Free Packaging (www.xilinx.com/pbfree)
- 100% Factory Tested

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Architecture

Virtex-II Array Overview

Virtex-II devices are user-programmable gate arrays with various configurable elements. The Virtex-II architecture is optimized for high-density and high-performance logic designs. As shown in Figure 1, the programmable device is comprised of input/output blocks (IOBs) and internal configurable logic blocks (CLBs).

Programmable I/O blocks provide the interface between package pins and the internal configurable logic. Most popular and leading-edge I/O standards are supported by the programmable IOBs.

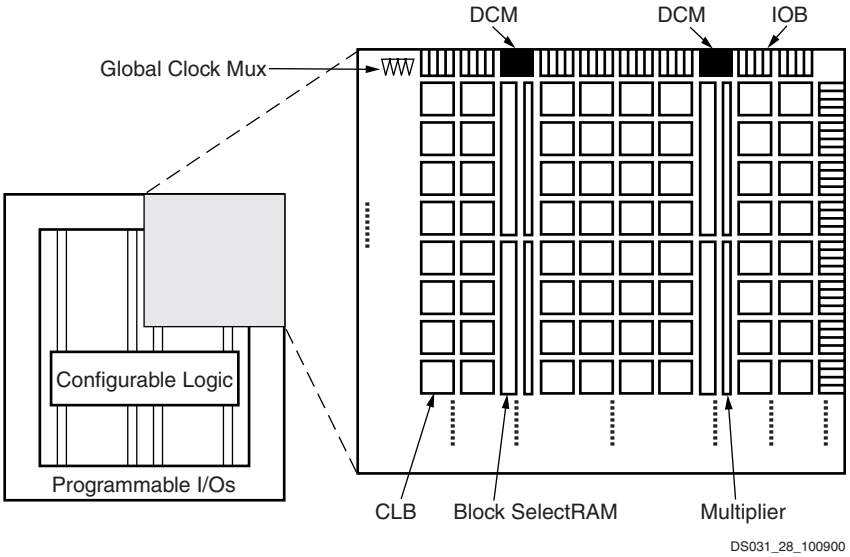

Figure 1: **Virtex-II Architecture Overview**

The internal configurable logic includes four major elements organized in a regular array.

- Configurable Logic Blocks (CLBs) provide functional elements for combinatorial and synchronous logic, including basic storage elements. BUFTs (3-state buffers) associated with each CLB element drive dedicated segmentable horizontal routing resources.
- Block SelectRAM memory modules provide large 18 Kbit storage elements of dual-port RAM.
- Multiplier blocks are 18-bit x 18-bit dedicated multipliers.
- DCM (Digital Clock Manager) blocks provide self-calibrating, fully digital solutions for clock distribution delay compensation, clock multiplication and division, coarse- and fine-grained clock phase shifting.

A new generation of programmable routing resources called Active Interconnect Technology interconnects all of these elements. The general routing matrix (GRM) is an array of routing switches. Each programmable element is tied to a switch matrix, allowing multiple connections to the general routing matrix. The overall programmable interconnection is hierarchical and designed to support high-speed designs.

All programmable elements, including the routing resources, are controlled by values stored in static memory cells. These values are loaded in the memory cells during configuration and can be reloaded to change the functions of the programmable elements.

Virtex-II Features

This section briefly describes Virtex-II features.

Input/Output Blocks (IOBs)

IOBs are programmable and can be categorized as follows:

- Input block with an optional single-data-rate or double-data-rate (DDR) register
- Output block with an optional single-data-rate or DDR register, and an optional 3-state buffer, to be driven directly or through a single or DDR register
- Bidirectional block (any combination of input and output configurations)

These registers are either edge-triggered D-type flip-flops or level-sensitive latches.

IOBs support the following single-ended I/O standards:

- LVTTL, LVCMOS (3.3V, 2.5V, 1.8V, and 1.5V)
- PCI-X compatible (133 MHz and 66 MHz) at 3.3V
- PCI compliant (66 MHz and 33 MHz) at 3.3V
- CardBus compliant (33 MHz) at 3.3V
- GTL and GTLP

Table 4: **LVTTL and LVCMOS Programmable Currents (Sink and Source)**

SelectI/O-Ultra	Programmable Current (Worst-Case Guaranteed Minimum)						
LVTTL	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA
LVCMOS33	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA
LVCMOS25	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA
LVCMOS18	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	n/a
LVCMOS15	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	n/a

Figure 6 shows the SSTL2, SSTL3, and HSTL configurations. HSTL can sink current up to 48 mA. (HSTL IV)

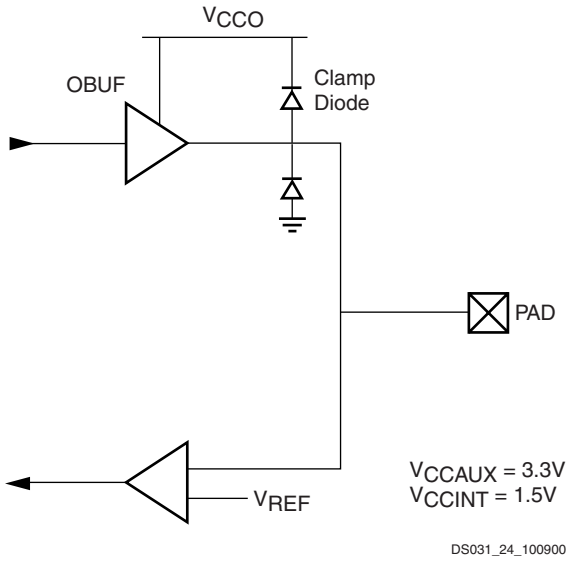

Figure 6: **SSTL or HSTL SelectI/O-Ultra Standards**

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. Virtex-II uses two memory cells to control the configuration of an I/O as an input. This is to reduce the probability of an I/O configured as an input from flipping to an output when subjected to a single event upset (SEU) in space applications.

Prior to configuration, all outputs not involved in configuration are forced into their high-impedance state. The pull-down resistors and the weak-keeper circuits are inactive. The dedicated pin HSWAP_EN controls the pull-up resistors prior to configuration. By default, HSWAP_EN is set high, which disables the pull-up resistors on user I/O pins. When HSWAP_EN is set low, the pull-up resistors are activated on user I/O pins.

All Virtex-II IOBs support IEEE 1149.1 compatible Boundary-Scan testing.

Input Path

The Virtex-II IOB input path routes input signals directly to internal logic and / or through an optional input flip-flop or latch, or through the DDR input registers. An optional delay element at the D-input of the storage element eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the Virtex-II device, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signaling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, V_{REF}. The need to supply V_{REF} imposes constraints on which standards can be used in the same bank. See I/O banking description.

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output and / or the 3-state signal can be routed to the buffer directly from the internal logic or through an output / 3-state flip-flop or latch, or through the DDR output / 3-state registers.

Each output driver can be individually programmed for a wide range of low-voltage signaling standards. In most signaling standards, the output High voltage depends on an externally supplied V_{CCO} voltage. The need to supply V_{CCO} imposes constraints on which standards can be used in the same bank. See I/O banking description.

I/O Banking

Some of the I/O standards described above require V_{CCO} and V_{REF} voltages. These voltages are externally supplied and connected to device pins that serve groups of IOB blocks, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from dividing each edge of the FPGA into two banks, as shown in Figure 7 and Figure 8. Each bank has multiple V_{CCO} pins, all of which must be connected to the same voltage. This voltage is determined by the output standards in use.

Digitally Controlled Impedance (DCI)

Today's chip output signals with fast edge rates require termination to prevent reflections and maintain signal integrity. High pin count packages (especially ball grid arrays) can not accommodate external termination resistors.

Virtex-II XCITE DCI provides controlled impedance drivers and on-chip termination for single-ended and differential I/Os. This eliminates the need for external resistors, and improves signal integrity. The DCI feature can be used on any IOB by selecting one of the DCI I/O standards.

When applied to inputs, DCI provides input parallel termination. When applied to outputs, DCI provides controlled impedance drivers (series termination) or output parallel termination.

DCI operates independently on each I/O bank. When a DCI I/O standard is used in a particular I/O bank, external reference resistors must be connected to two dual-function pins on the bank. These resistors, voltage reference of N transistor (VRN) and the voltage reference of P transistor (VRP) are shown in Figure 9.

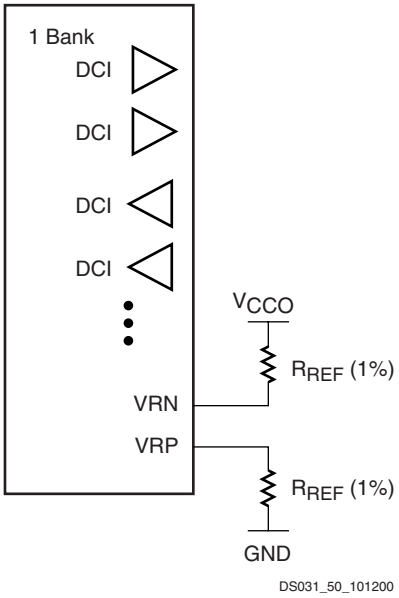

Figure 9: **DCI in a Virtex-II Bank**

When used with a terminated I/O standard, the value of resistors are specified by the standard (typically 50Ω). When used with a controlled impedance driver, the resistors set the output impedance of the driver within the specified range (25Ω to 100Ω). For all series and parallel terminations listed in Table 6 and Table 7, the reference resistors must have the same value for any given bank. One percent resistors are recommended.

The DCI system adjusts the I/O impedance to match the two external reference resistors, or half of the reference resistors, and compensates for impedance changes due to voltage and/or temperature fluctuations. The adjustment is done by turning parallel transistors in the IOB on or off.

Controlled Impedance Drivers (Series Term.)

DCI can be used to provide a buffer with a controlled output impedance. It is desirable for this output impedance to match the transmission line impedance (Z_0). Virtex-II input buffers also support LVDCI and LVDCI_DV2 I/O standards.

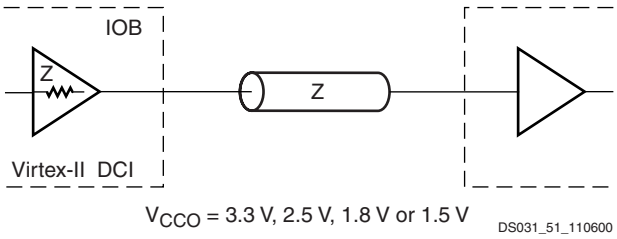

Figure 10: **Internal Series Termination**

Table 6: **SelectI/O-Ultra Controlled Impedance Buffers**

V_{CCO}	DCI	DCI Half Impedance
3.3 V	LVDCI_33	LVDCI_DV2_33
2.5 V	LVDCI_25	LVDCI_DV2_25
1.8 V	LVDCI_18	LVDCI_DV2_18
1.5 V	LVDCI_15	LVDCI_DV2_15

Controlled Impedance Drivers (Parallel)

DCI also provides on-chip termination for SSTL3, SSTL2, HSTL (Class I, II, III, or IV), and GTL/GTLP receivers or transmitters on bidirectional lines.

Table 7 and Table 8 list the on-chip parallel terminations available in Virtex-II devices. V_{CCO} must be set according to Table 3. Note that there is a V_{CCO} requirement for GTL_DCI and GTLP_DCI, due to the on-chip termination resistor.

Table 7: **SelectI/O-Ultra Buffers With On-Chip Parallel Termination**

I/O Standard Description	IOSTANDARD Attribute	
	External Termination	On-Chip Termination
SSTL3 Class I	SSTL3_I	SSTL3_I_DCI(1)
SSTL3 Class II	SSTL3_II	SSTL3_II_DCI(1)
SSTL2 Class I	SSTL2_I	SSTL2_I_DCI(1)
SSTL2 Class II	SSTL2_II	SSTL2_II_DCI(1)
HSTL Class I	HSTL_I	HSTL_I_DCI
HSTL Class II	HSTL_II	HSTL_II_DCI
HSTL Class III	HSTL_III	HSTL_III_DCI
HSTL Class IV	HSTL_IV	HSTL_IV_DCI
GTL	GTL	GTL_DCI
GTLP	GTLP	GTLP_DCI

Notes:
1. SSTL-compatible

Clock Distribution Switching Characteristics

Table 20: **Clock Distribution Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Global Clock Buffer I input to O output	T_{GIO}	0.47	0.52	0.59	ns, Max
Global Clock Buffer S input Setup/Hold to I1 an I2 inputs	T_{GSI}/T_{GIS}	0.55/ 0	0.61/ 0	0.70/ 0	ns, Max

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used (see Figure 16 in Module 2). The values listed below are worst-case. Precise values are provided by the timing analyzer.

Table 21: **CLB Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Combinatorial Delays					
4-input function: F/G inputs to X/Y outputs	T_{ILO}	0.35	0.39	0.44	ns, Max
5-input function: F/G inputs to F5 output	T_{IF5}	0.57	0.63	0.72	ns, Max
5-input function: F/G inputs to X output	T_{IF5X}	0.76	0.83	0.95	ns, Max
FXINA or FXINB inputs to Y output via MUXFX	T_{IFXY}	0.36	0.39	0.45	ns, Max
FXINA input to FX output via MUXFX	T_{INAFX}	0.26	0.28	0.32	ns, Max
FXINB input to FX output via MUXFX	T_{INBFX}	0.26	0.28	0.32	ns, Max
SOPIN input to SOPOUT output via ORCY	T_{SOPSOP}	0.35	0.38	0.44	ns, Max
Incremental delay routing through transparent latch to XQ/YQ outputs	T_{IFNCTL}	0.41	0.45	0.51	ns, Max
Sequential Delays					
FF Clock CLK to XQ/YQ outputs	T_{CKO}	0.45	0.50	0.57	ns, Max
Latch Clock CLK to XQ/YQ outputs	T_{CKLO}	0.54	0.59	0.68	ns, Max
Setup and Hold Times Before/After Clock CLK					
BX/BY inputs	T_{DICK}/T_{CKDI}	0.30/–0.07	0.33/–0.08	0.37/–0.09	ns, Min
DY inputs	T_{DYCK}/T_{CKDY}	0.30/–0.07	0.33/–0.08	0.37/–0.09	ns, Min
DX inputs	T_{DXCK}/T_{CKDX}	0.30/–0.07	0.33/–0.08	0.37/–0.09	ns, Min
CE input	T_{CECK}/T_{CKCE}	0.19/–0.06	0.21/–0.07	0.24/–0.08	ns, Min
SR/BY inputs (synchronous)	T_{SRCK}/T_{SCKR}	0.21/–0.02	0.23/–0.03	0.26/–0.03	ns, Min
Clock CLK					
Minimum Pulse Width, High	T_{CH}	0.61	0.67	0.77	ns, Min
Minimum Pulse Width, Low	T_{CL}	0.61	0.67	0.77	ns, Min
Set/Reset					
Minimum Pulse Width, SR/BY inputs (asynchronous)	T_{RPW}	0.61	0.67	0.77	ns, Min
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	T_{RQ}	1.06	1.17	1.34	ns, Max
Toggle Frequency (MHz) (for export control)	F_{TOG}	820	750	650	MHz

Virtex-II Platform FPGAs: Pinout Information

DS031-4 (v3.5) November 5, 2007

Product Specification

This document provides Virtex-II™ Device/Package Combinations, Maximum I/Os Available, and Virtex-II Pin Definitions, followed by pinout tables for the following packages:

- CS144/CSG144 Chip-Scale BGA Package
- FG256/FGG256 Fine-Pitch BGA Package
- FG456/FGG456 Fine-Pitch BGA Package
- FG676/FGG676 Fine-Pitch BGA Package
- BG575/BGG575 Standard BGA Package
- BG728/BGG728 Standard BGA Package
- FF896 Flip-Chip Fine-Pitch BGA Package
- FF1152 Flip-Chip Fine-Pitch BGA Package
- FF1517 Flip-Chip Fine-Pitch BGA Package
- BF957 Flip-Chip BGA Package

For device pinout diagrams and layout guidelines, refer to the ***Virtex-II Platform FPGA User Guide***. ASCII package pinout files are also available for download from the Xilinx website (**www.xilinx.com**).

Virtex-II Device/Package Combinations and Maximum I/Os Available

Wire-bond and flip-chip packages are available. Table 1 and Table 2 show the maximum number of user I/Os possible in wire-bond and flip-chip packages, respectively.

Table 3 shows the number of user I/Os available for all device/package combinations.

- CS denotes wire-bond chip-scale ball grid array (BGA) (0.80 mm pitch).
- CSG denotes Pb-free wire-bond chip-scale ball grid array (BGA) (0.80 mm pitch).
- FG denotes wire-bond fine-pitch BGA (1.00 mm pitch).
- FGG denotes Pb-free wire-bond fine-pitch BGA (1.00 mm pitch).
- BG denotes standard BGA (1.27 mm pitch).
- BGG denotes Pb-free standard BGA (1.27 mm pitch).
- FF denotes flip-chip fine-pitch BGA (1.00 mm pitch).
- BF denotes flip-chip BGA (1.27 mm pitch).

The number of I/Os per package include all user I/Os except the 15 control pins (CCLK, DONE, M0, M1, M2, PROG_B, PWRDWN_B, TCK, TDI, TDO, TMS, HSWAP_EN, DXN, DXP, AND RSVD).

Table 1: **Wire-Bond Packages Information**

Package[1]	CS144/ CSG144	FG256/ FGG256	FG456/ FGG456	FG676/ FGG676	BG575/ BGG575	BG728/ BGG728
Pitch (mm)	0.80	1.00	1.00	1.00	1.27	1.27
Size (mm)	12 x 12	17 x 17	23 x 23	27 x 27	31 x 31	35 x 35
I/Os	92	172	324	484	408	516

Notes:
1. Wire-bond packages include FGG*nnn* Pb-free versions. See Virtex-II Ordering Examples (Module 1).

Table 2: **Flip-Chip Packages Information**

Package	FF896	FF1152	FF1517	BF957
Pitch (mm)	1.00	1.00	1.00	1.27
Size (mm)	31 x 31	35 x 35	40 x 40	40 x 40
I/Os	624	824	1,108	684

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Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
NA	VCCINT	R16		
NA	VCCINT	R7		
NA	VCCINT	H16		
NA	VCCINT	H7		
NA	VCCINT	G16		
NA	VCCINT	G15		
NA	VCCINT	G8		
NA	VCCINT	G7		
NA	VCCINT	F17		
NA	VCCINT	F6		
NA	GND	AB22		
NA	GND	AB1		
NA	GND	AA21		
NA	GND	AA2		
NA	GND	Y20		
NA	GND	Y3		
NA	GND	W19		
NA	GND	W4		
NA	GND	P14		
NA	GND	P13		
NA	GND	P12		
NA	GND	P11		
NA	GND	P10		
NA	GND	P9		
NA	GND	N14		
NA	GND	N13		
NA	GND	N12		
NA	GND	N11		
NA	GND	N10		
NA	GND	N9		
NA	GND	M14		
NA	GND	M13		
NA	GND	M12		
NA	GND	M11		

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
NA	VCCINT	H19		
NA	VCCINT	H8		
NA	GND	AF26		
NA	GND	AF1		
NA	GND	AE25		
NA	GND	AE14		
NA	GND	AE13		
NA	GND	AE2		
NA	GND	AD24		
NA	GND	AD3		
NA	GND	AC23		
NA	GND	AC4		
NA	GND	AB22		
NA	GND	AB5		
NA	GND	AA21		
NA	GND	AA6		
NA	GND	U17		
NA	GND	U16		
NA	GND	U15		
NA	GND	U14		
NA	GND	U13		
NA	GND	U12		
NA	GND	U11		
NA	GND	U10		
NA	GND	T17		
NA	GND	T16		
NA	GND	T15		
NA	GND	T14		
NA	GND	T13		
NA	GND	T12		
NA	GND	T11		
NA	GND	T10		
NA	GND	R17		
NA	GND	R16		
NA	GND	R15		
NA	GND	R14		
NA	GND	R13		

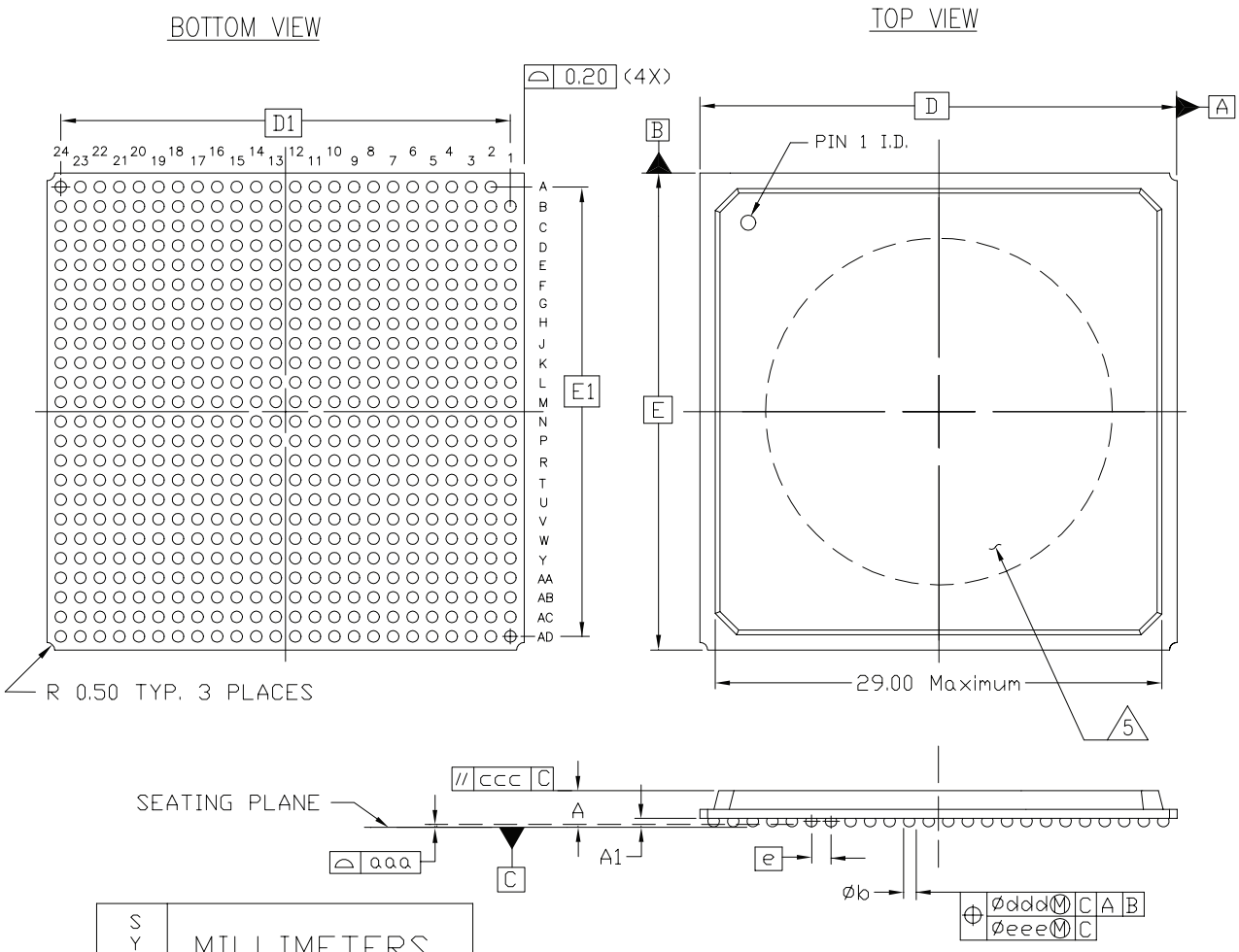
Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
6	IO_L06N_6	V6		
6	IO_L19P_6	U7		
6	IO_L19N_6	T8		
6	IO_L21P_6	AA1		
6	IO_L21N_6/VREF_6	Y2		
6	IO_L22P_6	Y1		
6	IO_L22N_6	W1		
6	IO_L24P_6	W2		
6	IO_L24N_6	V2		
6	IO_L43P_6	V4		
6	IO_L43N_6	V3		
6	IO_L45P_6	U6		
6	IO_L45N_6/VREF_6	U5		
6	IO_L46P_6	T7		
6	IO_L46N_6	T6		
6	IO_L48P_6	R8		
6	IO_L48N_6	R7		
6	IO_L49P_6	U2		
6	IO_L49N_6	U1		
6	IO_L51P_6	U4		
6	IO_L51N_6/VREF_6	U3		
6	IO_L52P_6	T1		
6	IO_L52N_6	R1		
6	IO_L54P_6	T3		
6	IO_L54N_6	T2		
6	IO_L67P_6	T5	NC	
6	IO_L67N_6	T4	NC	
6	IO_L69P_6	R6	NC	
6	IO_L69N_6/VREF_6	R5	NC	
6	IO_L70P_6	P8	NC	
6	IO_L70N_6	P7	NC	
6	IO_L72P_6	R2	NC	
6	IO_L72N_6	P1	NC	
6	IO_L73P_6	R3	NC	NC
6	IO_L73N_6	P3	NC	NC
6	IO_L91P_6	P5		

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
NA	GND	Y5		
NA	GND	W19		
NA	GND	W6		
NA	GND	V24		
NA	GND	V18		
NA	GND	V7		
NA	GND	V1		
NA	GND	R21		
NA	GND	R4		
NA	GND	P14		
NA	GND	P13		
NA	GND	P12		
NA	GND	P11		
NA	GND	N14		
NA	GND	N13		
NA	GND	N12		
NA	GND	N11		
NA	GND	M14		
NA	GND	M13		
NA	GND	M12		
NA	GND	M11		
NA	GND	L14		
NA	GND	L13		
NA	GND	L12		
NA	GND	L11		
NA	GND	K21		
NA	GND	K4		
NA	GND	G24		
NA	GND	G18		
NA	GND	G7		
NA	GND	G1		
NA	GND	F19		
NA	GND	F6		
NA	GND	E20		
NA	GND	E5		
NA	GND	D21		

BG575/BGG575 Standard BGA Package Specifications (1.27mm pitch)



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A		2.33	2.60
A_1	0.50	0.60	0.70
D/E	31.00 BSC		
D_1/E_1	29.21 REF		
e	1.27BSC		
Øb	0.60	0.75	0.90
aaa			0.20
ccc			0.35
ddd			0.30
eee			0.15
M	24		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-BAN-1 (DEPOPULATED)
4. NO SOLDER BALL AND LAND ON A1.

5 HEAT SINK OPTION

575-BALL MOLDED BGA (BG575/BGG575)

Figure 5: **BG575/BGG575 Standard BGA Package Specifications**

BG728/BGG728 Standard BGA Package

As shown in Table 10, XC2V3000 Virtex-II devices are available in the BG728/BGG728 BGA package. Following this table are the BG728/BGG728 Standard BGA Package Specifications (1.27mm pitch).

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
0	IO_L01N_0	B3
0	IO_L01P_0	A3
0	IO_L02N_0	B4
0	IO_L02P_0	A4
0	IO_L03N_0/VRP_0	C5
0	IO_L03P_0/VRN_0	C6
0	IO_L04N_0/VREF_0	B5
0	IO_L04P_0	A5
0	IO_L05N_0	E6
0	IO_L05P_0	D6
0	IO_L06N_0	B6
0	IO_L06P_0	A6
0	IO_L19N_0	E7
0	IO_L19P_0	D8
0	IO_L21N_0	F8
0	IO_L21P_0/VREF_0	E8
0	IO_L22N_0	C7
0	IO_L22P_0	C8
0	IO_L24N_0	B7
0	IO_L24P_0	A7
0	IO_L25N_0	H9
0	IO_L25P_0	J9
0	IO_L27N_0	F9
0	IO_L27P_0/VREF_0	G9
0	IO_L28N_0	E9
0	IO_L28P_0	D9
0	IO_L30N_0	C9
0	IO_L30P_0	B9
0	IO_L49N_0	A8
0	IO_L49P_0	A9
0	IO_L51N_0	G10
0	IO_L51P_0/VREF_0	H10
0	IO_L52N_0	F10

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
3	IO_L24N_3	AC8		
3	IO_L24P_3	AB8		
3	IO_L23N_3	AE2		
3	IO_L23P_3	AF3		
3	IO_L22N_3	AD3		
3	IO_L22P_3	AE3		
3	IO_L21N_3/VREF_3	AD6		
3	IO_L21P_3	AD7		
3	IO_L20N_3	AF1		
3	IO_L20P_3	AG1		
3	IO_L19N_3	AD4		
3	IO_L19P_3	AE4		
3	IO_L06N_3	AD8		
3	IO_L06P_3	AE7		
3	IO_L05N_3	AG2		
3	IO_L05P_3	AH2		
3	IO_L04N_3	AD5		
3	IO_L04P_3	AE5		
3	IO_L03N_3/VREF_3	AC9		
3	IO_L03P_3	AD9		
3	IO_L02N_3/VRP_3	AH1		
3	IO_L02P_3/VRN_3	AJ1		
3	IO_L01N_3	AF4		
3	IO_L01P_3	AG3		
4	IO_L01N_4/BUSY/DOUT(1)	AK2		
4	IO_L01P_4/INIT_B	AJ3		
4	IO_L02N_4/D0/DIN(1)	AE8		
4	IO_L02P_4/D1	AF9		
4	IO_L03N_4/D2/ALT_VRP_4	AH5		
4	IO_L03P_4/D3/ALT_VRN_4	AH6		
4	IO_L04N_4/VREF_4	AJ4		
4	IO_L04P_4	AK4		
4	IO_L05N_4/VRP_4	AC10		
4	IO_L05P_4/VRN_4	AC11		
4	IO_L06N_4	AH7		
4	IO_L06P_4	AG6		

FF1517 Flip-Chip Fine-Pitch BGA Package

As shown in Table 13, XC2V4000, XC2V6000, and XC2V8000 Virtex-II devices are available in the FF1517 flip-chip fine-pitch BGA package. Pins in each of these devices are the same, except for the pin differences in the XC2V4000 and XC2V6000 devices shown in the No Connect columns. Following this table are the FF1517 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
0	IO_L01N_0	B36		
0	IO_L01P_0	C36		
0	IO_L02N_0	J30		
0	IO_L02P_0	J29		
0	IO_L03N_0/VRP_0	D33		
0	IO_L03P_0/VRN_0	D34		
0	IO_L04N_0/VREF_0	C34		
0	IO_L04P_0	C35		
0	IO_L05N_0	H30		
0	IO_L05P_0	G30		
0	IO_L06N_0	D32		
0	IO_L06P_0	E33		
0	IO_L07N_0	A35	NC	
0	IO_L07P_0	A36	NC	
0	IO_L08N_0	K28	NC	
0	IO_L08P_0	J28	NC	
0	IO_L09N_0	E32	NC	
0	IO_L09P_0/VREF_0	F32	NC	
0	IO_L10N_0	B34	NC	
0	IO_L10P_0	B35	NC	
0	IO_L11N_0	H29	NC	
0	IO_L11P_0	H28	NC	
0	IO_L12N_0	F31	NC	
0	IO_L12P_0	G31	NC	
0	IO_L19N_0	C32		
0	IO_L19P_0	C33		
0	IO_L20N_0	M26		
0	IO_L20P_0	M25		
0	IO_L21N_0	E30		
0	IO_L21P_0/VREF_0	E31		
0	IO_L22N_0	A33		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
1	IO_L33N_1/VREF_1	D11	NC	
1	IO_L33P_1	D12	NC	
1	IO_L32N_1	H14	NC	
1	IO_L32P_1	H13	NC	
1	IO_L31N_1	A8	NC	
1	IO_L31P_1	A9	NC	
1	IO_L30N_1	F11		
1	IO_L30P_1	F12		
1	IO_L29N_1	K14		
1	IO_L29P_1	L14		
1	IO_L28N_1	C9		
1	IO_L28P_1	C10		
1	IO_L27N_1/VREF_1	G11		
1	IO_L27P_1	G12		
1	IO_L26N_1	M15		
1	IO_L26P_1	M14		
1	IO_L25N_1	B7		
1	IO_L25P_1	B8		
1	IO_L24N_1	D9		
1	IO_L24P_1	D10		
1	IO_L23N_1	J13		
1	IO_L23P_1	J12		
1	IO_L22N_1	A6		
1	IO_L22P_1	A7		
1	IO_L21N_1/VREF_1	E9		
1	IO_L21P_1	E10		
1	IO_L20N_1	D8		
1	IO_L20P_1	E7		
1	IO_L19N_1	C7		
1	IO_L19P_1	C8		
1	IO_L12N_1	F9	NC	
1	IO_L12P_1	F10	NC	
1	IO_L11N_1	H12	NC	
1	IO_L11P_1	H11	NC	
1	IO_L10N_1	B5	NC	
1	IO_L10P_1	B6	NC	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
3	IO_L82N_3	AA4		
3	IO_L82P_3	AB4		
3	IO_L81N_3/VREF_3	AB11		
3	IO_L81P_3	AA11		
3	IO_L80N_3	AC1		
3	IO_L80P_3	AD1		
3	IO_L79N_3	AA7		
3	IO_L79P_3	AB7		
3	IO_L78N_3	AB12		
3	IO_L78P_3	AA12		
3	IO_L77N_3	AC2		
3	IO_L77P_3	AC3		
3	IO_L76N_3	AB5		
3	IO_L76P_3	AC5		
3	IO_L75N_3/VREF_3	AD9		
3	IO_L75P_3	AC9		
3	IO_L74N_3	AD2		
3	IO_L74P_3	AE2		
3	IO_L73N_3	AB6		
3	IO_L73P_3	AC6		
3	IO_L72N_3	AD10		
3	IO_L72P_3	AC10		
3	IO_L71N_3	AD3		
3	IO_L71P_3	AE3		
3	IO_L70N_3	AC7		
3	IO_L70P_3	AD7		
3	IO_L69N_3/VREF_3	AE8		
3	IO_L69P_3	AD8		
3	IO_L68N_3	AE1		
3	IO_L68P_3	AF1		
3	IO_L67N_3	AD4		
3	IO_L67P_3	AE4		
3	IO_L60N_3	AD12		
3	IO_L60P_3	AC12		
3	IO_L59N_3	AF3		
3	IO_L59P_3	AG3		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
6	VCCO_6	AG33		
6	VCCO_6	AF38		
6	VCCO_6	AF27		
6	VCCO_6	AE31		
6	VCCO_6	AE27		
6	VCCO_6	AE26		
6	VCCO_6	AD27		
6	VCCO_6	AD26		
6	VCCO_6	AC29		
6	VCCO_6	AC27		
6	VCCO_6	AC26		
6	VCCO_6	AB37		
6	VCCO_6	AB27		
6	VCCO_6	AB26		
6	VCCO_6	AA27		
6	VCCO_6	AA26		
7	VCCO_7	W27		
7	VCCO_7	W26		
7	VCCO_7	V37		
7	VCCO_7	V27		
7	VCCO_7	V26		
7	VCCO_7	U29		
7	VCCO_7	U27		
7	VCCO_7	U26		
7	VCCO_7	T27		
7	VCCO_7	T26		
7	VCCO_7	R31		
7	VCCO_7	R27		
7	VCCO_7	R26		
7	VCCO_7	P38		
7	VCCO_7	P27		
7	VCCO_7	N33		
7	VCCO_7	L35		
NA	CCLK	AT5		
NA	PROG_B	H31		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	VCCINT	R19		
NA	VCCINT	R18		
NA	VCCINT	R17		
NA	VCCINT	R16		
NA	VCCINT	R15		
NA	VCCINT	P26		
NA	VCCINT	P20		
NA	VCCINT	P14		
NA	VCCINT	N27		
NA	VCCINT	N20		
NA	VCCINT	N13		
NA	GND	AW38		
NA	GND	AW37		
NA	GND	AW20		
NA	GND	AW3		
NA	GND	AW2		
NA	GND	AV39		
NA	GND	AV38		
NA	GND	AV37		
NA	GND	AV29		
NA	GND	AV11		
NA	GND	AV3		
NA	GND	AV2		
NA	GND	AV1		
NA	GND	AU39		
NA	GND	AU38		
NA	GND	AU37		
NA	GND	AU3		
NA	GND	AU2		
NA	GND	AU1		
NA	GND	AT36		
NA	GND	AT23		
NA	GND	AT20		
NA	GND	AT17		
NA	GND	AT4		
NA	GND	AR35		

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
6	IO_L67P_6	AB30	
6	IO_L67N_6	AA30	
6	IO_L68P_6	W26	
6	IO_L68N_6	V26	
6	IO_L69P_6	AB31	
6	IO_L69N_6/VREF_6	AA31	
6	IO_L70P_6	AA29	
6	IO_L70N_6	Y29	
6	IO_L71P_6	Y24	
6	IO_L71N_6	W24	
6	IO_L72P_6	V25	
6	IO_L72N_6	U25	
6	IO_L73P_6	Y28	
6	IO_L73N_6	W28	
6	IO_L74P_6	W23	
6	IO_L74N_6	V23	
6	IO_L75P_6	Y30	
6	IO_L75N_6/VREF_6	W30	
6	IO_L76P_6	Y31	
6	IO_L76N_6	W31	
6	IO_L77P_6	V27	
6	IO_L77N_6	U27	
6	IO_L78P_6	W29	
6	IO_L78N_6	U29	
6	IO_L91P_6	U23	
6	IO_L91N_6	T23	
6	IO_L92P_6	U26	
6	IO_L92N_6	T26	
6	IO_L93P_6	V28	
6	IO_L93N_6/VREF_6	U28	
6	IO_L94P_6	U24	
6	IO_L94N_6	T24	
6	IO_L95P_6	V30	
6	IO_L95N_6	U30	
6	IO_L96P_6	V31	
6	IO_L96N_6	U31	
7	IO_L96P_7	T27	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
NA	GND	T14	
NA	GND	T15	
NA	GND	T16	
NA	GND	T17	
NA	GND	T18	
NA	GND	T22	
NA	GND	T25	
NA	GND	T28	
NA	GND	T31	
NA	GND	U14	
NA	GND	U15	
NA	GND	U16	
NA	GND	U17	
NA	GND	U18	
NA	GND	V14	
NA	GND	V15	
NA	GND	V16	
NA	GND	V17	
NA	GND	V18	
NA	GND	W7	
NA	GND	W25	
NA	GND	AB4	
NA	GND	AB16	
NA	GND	AB28	
NA	GND	AC9	
NA	GND	AC23	
NA	GND	AD2	
NA	GND	AD8	
NA	GND	AD24	
NA	GND	AD30	
NA	GND	AE7	
NA	GND	AE13	
NA	GND	AE16	
NA	GND	AE19	
NA	GND	AE25	
NA	GND	AF6	
NA	GND	AF26	
NA	GND	AG5	